

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICROSOFT CORPORATION,
Petitioner,

v.

THROUGHPUTER, INC.,
Patent Owner.

IPR2022-01566
Patent 11,036,556 B1

Before MICHAEL R. ZECHER, MATTHEW S. MEYERS, and
JULIET MITCHELL DIRBA, *Administrative Patent Judges*.

DIRBA, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

IPR2022-01566
Patent 11,036,556 B1

On November 7, 2022, Microsoft Corporation (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–8 of U.S. Patent No. 11,036,556 B1 (Ex. 1001, “the ’556 patent”). Paper 2 (“Pet.”). ThroughPuter, Inc. (“Patent Owner”) timely filed a Preliminary Response. Paper 8 (“Prelim. Resp.”). With our authorization (Paper 10), Petitioner filed a Preliminary Reply (Paper 11, “Prelim. Reply”), and Patent Owner filed a Preliminary Sur-Reply (Paper 12, “Prelim. Sur-Reply”).

An *inter partes* review may not be instituted unless “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

For the reasons given below, on this record, Petitioner has not established a reasonable likelihood that it would prevail in showing the unpatentability of at least one challenged claim. Accordingly, we do not institute an *inter partes* review of the ’556 patent.

I. BACKGROUND

A. Related Matters

The parties indicate that the ’556 patent has been asserted in *ThroughPuter, Inc. v. Microsoft Corp.*, No. 2:22-cv-00492-BJR (W.D. Wash.), which was consolidated with *ThroughPuter, Inc. v. Microsoft Corp.*, No. 2:22-cv-00344-BJR (W.D. Wash.). Pet. 76; Paper 4 (Patent Owner’s Mandatory Notices), 2. The parties also state that Petitioner has challenged other patents from that litigation in IPR2022-00527, IPR2022-00528, IPR2022-00574, IPR2022-00757, and IPR2022-00758. *Id.*

B. The Petitioner's Asserted Grounds

Petitioner asserts the following grounds of unpatentability (Pet. 2):

| Claim(s) Challenged | 35 U.S.C. § | Reference(s)/Basis |
|--------------------------------|--------------------|---|
| 1, 2, 4–8 | 103 ¹ | Kupferschmidt ² , Tuan ³ |
| 1–8 | 103 | Kupferschmidt, Tuan, Brent ⁴ |
| 4 | 103 | Kupferschmidt, Tuan, Sandstrom-501 ⁵ |
| 4 | 103 | Kupferschmidt, Tuan, Brent, Sandstrom-501 |

In support of its contentions, Petitioner relies on the testimony of Jeffrey S. Chase, Ph.D. (Ex. 1003) and June Ann Munford (Ex. 1007).

C. Summary of the '556 Patent

The '556 patent is titled “Concurrent Program Execution Optimization.” Ex. 1001, code (54). The application that led to the '556

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011), revised 35 U.S.C. § 103 effective March 16, 2013. The challenged patent was filed after March 16, 2013 and claims priority to applications filed after that date. As a consequence, we refer to the current version of the statute. *Accord* Pet. 2.

² US 2010/0333099 A1, published Dec. 30, 2010 (Ex. 1004).

³ Vu Manh Tuan, “A Study on a Multitasking Environment for Dynamically Reconfigurable Processors,” Doctoral Dissertation, School of Science for Open and Environmental Systems Graduate School of Science and Technology, Keio University (2009) (Ex. 1005).

⁴ US 2010/0131955 A1, published May 27, 2010 (Ex. 1006).

⁵ US 2012/0079501 A1, published Mar. 29, 2012 (Ex. 1010).

patent was filed on March 8, 2021, claiming priority to applications filed as early as August 23, 2013. *Id.* at (22), (60), (63).

The Specification is directed to “managing execution of multiple concurrent, multi-task software programs on parallel processing hardware.” Ex. 1001, 1:45–48. Figure 2 of the ’556 patent is reproduced below.

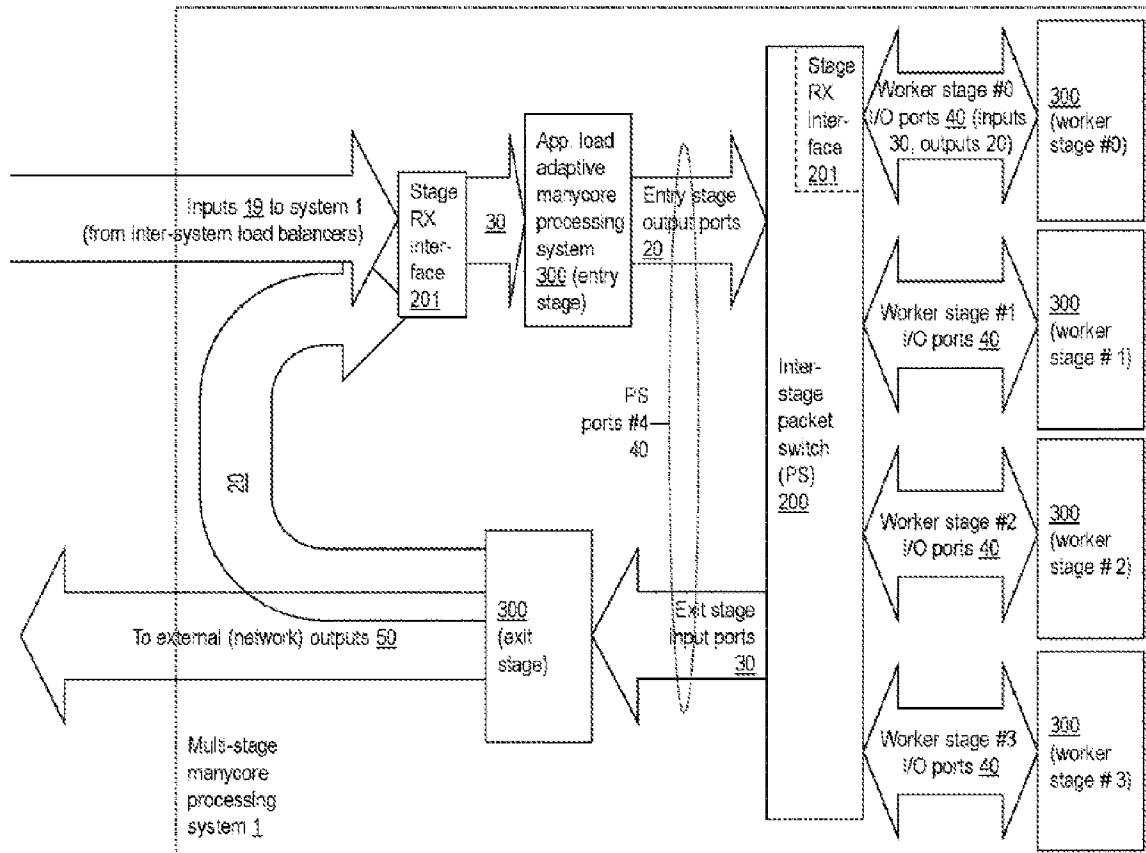


FIG. 2

Figure 2 is a functional block diagram of multi-stage manycore processing system 1, which is shared dynamically among tasks of multiple application programs (apps) and instances (insts) thereof. *Id.* at 5:18–21, 10:29–32. For each of the apps, each task is located at one of the processing stages 300. *Id.* at 10:32–33. Nevertheless, for any given app-inst, copies of same task

software can be located at more than one of the processing stages 300 of a given system 1, thus supporting any combination of pipelined and/or parallelized processing. *Id.* at 10:34–41. Hardware logic is implemented for scheduling tasks of application program instances and prioritizing inter-task communications (ITC) among tasks of a given app instance. *Id.* at 10:10–13.

D. Challenged Claims

Petitioner challenges all eight claims of the '556 patent. Of these, only claim 1 is independent. It recites:

1. A method performed in a data processing system, the method comprising:

receiving, by hardware logic and/or software logic, requests to perform different tasks on behalf of instances of a plurality of programs managed by a data processing system;

identifying, by the hardware logic and/or software logic for each of the instances, communication interdependencies between different processing stages of a set of processing stages of the respective instance;

based on conditions in the data processing system, dynamically varying, by the hardware logic and/or software logic, structures of field-programmable gate arrays used to process different tasks of the instances of the plurality of programs, the structures being dynamically varied by

identifying available field-programmable gate arrays of the data processing system that are available to process different processing stages of requesting instances of respective programs,

based at least on the conditions in the data processing system, identifying selected field-programmable gate arrays from the available field-programmable gate arrays to execute the different

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