AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space;

at least one MLC nonvolatile memory element;

at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements; ~~and~~

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein;

the controller performing a data integrity test on stored data in a given one of the MLC and SLC nonvolatile memory elements after any access operation is performed thereon;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

2. (Currently Amended) The system of Claim 1, wherein the memory elements are a software module, a hardware module, a standalone device, or multi-chip package.

3. (Currently Amended) The system of Claim 1, wherein at least one of the volatile or nonvolatile memory elements ~~memories~~ are embedded in the at least one controller.

4. (Currently Amended) The system of Claim 1, wherein the MLC and SLC nonvolatile memory elements comprise [[is]] flash memory.

5. (Currently Amended) The system of Claim 1, wherein the memory in the SLC and MLC nonvolatile memory elements is phase-change memory.

6. (Currently Amended) The system of Claim 1, wherein the memory in the SLC and MLC nonvolatile memory elements is magnetic random access memory.

7. (Currently Amended) The system of Claim 1, wherein the random access volatile memory element is dynamic random access memory.

8. (Currently Amended) The system of Claim 1, wherein the random access volatile memory element is static random access memory.

9. (Original) The system of Claim 1, wherein the at least one SLC nonvolatile memory element includes a hard disk drive (HDD).

10. (New) The system of Claim 1, wherein the controller, upon detection of a failure of the data integrity test, remaps the data to the other of the MLC and SLC nonvolatile memory elements.

11. (New) The system of Claim 10, wherein the given one of the MLC and SLC nonvolatile memory elements is the MLC nonvolatile memory element.

12. (New) The system of Claim 10, wherein the SLC memory element has a higher endurance than the MLC memory element.

13. (New) The system of Claim 1, wherein the access operation is a Read operation.

14. (New) The system of Claim 1, wherein the access operation is a Write operation.

15. (New) The system of Claim 1, wherein the MLC is a 1 bit cell.

16. (New) The system of Claim 1, wherein the MLC is a multilevel cell, wherein the multilevel cell stores n bits per cell, wherein n is any integer greater than 1.

17. (New) The system of Claim 16, wherein the multilevel cell is a 3 bit cell.

18. (New) The system of Claim 16, wherein the multilevel cell is a 4 bit cell.

19. (New) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space;

at least one MLC nonvolatile memory element;

at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

at least one controller to maintain an address table in one or more of the memory elements;

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein;

the controller performing a data integrity test on stored data in a given one of the MLC and SLC nonvolatile memory elements after any access operation is performed thereon;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

20. (Currently Amended) The system of Claim 19, wherein the memory elements are a software module, a hardware module, a standalone device, or multi-chip package.

21. (Currently Amended) The system of Claim 19, wherein at least one of the volatile or nonvolatile memory elements are embedded in the at least one controller.