IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR UNITED STATES PATENT

LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation of U.S. Patent Application No. U.S. Application No. 14/950,553 filed on November 24, 2015, entitled LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM (Atty. Dkt. No. GRTD-32800), which published on June 2, 2016, as U.S. Application Publication No. 2016-0155496, now U.S. Patent No. 9,997,240 issued June 12, 2018, which is incorporated by reference in its entirety. U.S. Application No. 14/950,553 is a Continuation of U.S. Patent Application No. 14/525,411, filed October 28, 2014, entitled LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM, which published on October 1, 2015, as U.S. Publication No. 2015-0278013, now U.S. Patent No. 9,196,385, issued on November 24, 2015, (Atty. Dkt. No. GRTD-32620). Application No. 14/525,411 is a Division of U.S. Patent Application No. 13/455,267, filed April 25, 2012, published on January 24, 2013, as U.S. Publication No. 2013-0021846, now U.S. Patent No. 8,891,298, issued on November 18, 2014, entitled LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM (Atty. Dkt. No. GRTD-32619). Application No. 13/455,267 claims the benefit of U.S. Provisional Application No. 61/509,257, filed July 19, 2011, entitled LIFETIME MIXED LEVEL NAND FLASH SYSTEM (Atty. Dkt. No. GRTD-32624). Patent Nos. 9,997,240; 9,196,385; and 8,891,298 and Patent Application Publication Nos. 2015-0278013 and 2013-0021846 are hereby incorporated by reference in their entirety. This application also incorporates by reference the complete disclosure of U.S. Patent Application No. 12/256,362, filed October 22, 2008, published on April 30, 2009, as U.S. Publication No. 2009-0109787, now U.S. Patent No. 7,855,916, issued on December 21, 2010, entitled NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES (Atty. Dkt. No.

GRTD-32614). This application also incorporates by reference the complete disclosure of U.S. Patent Application No. 12/915,177, filed October 29, 2010, published on March 10, 2011, as U.S. Publication No. 2011-0060870, now U.S. Patent No. 8,194,452, issued on June 5, 2012, entitled NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES (Atty. Dkt. No. 32615).

TECHNICAL FIELD

[0002] This application relates to a system and method for providing reliable storage through the use of non-volatile memories and, more particularly, to a system and method of increasing the reliability and lifetime of a NAND flash storage system, module, or chip through the use of a combination of single-level cell (SLC) and multi-level cell (MLC) NAND flash storage without substantially raising the cost of the NAND flash storage system. The memory in a total non-volatile memory system may contain some SRAM (static random-access memory), DRAM (dynamic RAM), RRAM (resistive RAM), PCM (phase change memory), MAGRAM (magnetic random-access memory), NAND flash, and one or more HDDs (hard disk drives) when storage of the order of several terabytes is required. The SLC non-volatile memory can be flash, PCM, RRAM, MAGRAM or any other solid-state non-volatile memory as long as it has endurance that is superior to that of MLC flash, and it provides for data access speeds that are faster than that of MLC flash or rotating storage media (e.g., HDDs).

BACKGROUND

[0003] Non-volatile memories provide long-term storage of data. More particularly, non-volatile memories can retain the stored data even when not powered. Magnetic (rotating) hard disk drives (HDD) dominate this storage medium due to lower cost compared to solid state disks (SSD). Optical (rotating) disks, tape drives and others have a smaller role in long-term storage systems. SSDs are preferred for their superior performance (fast access time), mechanical reliability and ruggedness, and portability. Flash memory, more specifically NAND flash, is the dominant SSD medium today.

[0004] RRAM, PCM, MAGRAM and others, wi1llikely play a larger role in the future, each of them having their own advantages and disadvantages. They may ultimately replace flash memories, initially for use as a "write buffer" and later to replace "SLC flash" and "MLC flash." MLC NAND flash is a flash memory technology using multiple levels per cell to allow more bits to be stored using the same number of transistors. In SLC NAND flash technology, each cell can exist in one of two states, storing one bit of information per cell. Most MLC NAND flash memory has four possible states per cell, so it can store two bits of information per cell.

[0005] These semiconductor technology driven "flash alternatives," i.e., RRAM, PCM, MAGRAM and others, have several advantages over any (SLC or MLC) flash because they: 1) allow data to be written over existing data (without prior erase of existing data), 2) allow for an erase of individual bytes or pages (instead of having to erase an entire block), and 3) possess superior endurance (1,000,000 write-erase cycles compared to typical 100,000 cycles for SLC flash and less than 10,000 cycles for MLC flash).

[0006] HDDs have several platters. Each platter contains 250-5,000 tracks (concentric circles). Each track contains 64 to 256 sectors. Each sector contains 512 bytes of data and has a unique "physical (memory) address." A plurality of sectors is typically combined to form a "logical block" having a unique "logical address." This logical address is the address at which the logical block of physical sectors appears to reside from the perspective of an executing application program. The size of each logical block and its logical address (and/or address ranges/boundaries) is optimized for the particular operating system (OS) and software

applications executed by the host processor. A computer OS organizes data as "files." Each file may be located (stored) in either a single logical block or a plurality of logical blocks, and therefore, the location of files typically traverses the boundaries of individual (physical) sectors. Sometimes, a plurality of files has to be combined and/ or modified, which poses an enormous challenge for the memory controller device of a non-volatile memory system.

[0007] SSDs are slowly encroaching on the HDD space and the vast majority of NAND flash in enterprise servers utilizes a SLC architecture, which further comprises a NAND flash controller and a flash translation layer (FTL). NAND flash devices are generally fragmented into a number of identically sized blocks, each of which is further segmented into some number of pages. It should be noted that asymmetrical block sizes, as well as page sizes, are also acceptable within a device or a module containing devices. For example, a block may comprise 32 to 64 pages, each of which incorporates 2 - 4 Kbit of memory. In addition, the process of writing data to a NAND flash memory device is complicated by the fact that, during normal operation of, for example, single-level storage (SLC) , erased bits (usually all bits in a block with the value of '1') can only be changed to the opposite state (usually '0') once before the entire block must be erased. Blocks can only be erased in their entirety, and, when erased, are usually written to '1' bits. However, if an erased block is already there, and if the addresses (block, page, etc.) are allowed, data can be written immediately; if not, a block has to be erased before it can be written to.

[0008] FTL is the driver that works in conjunction with an existing operating system (or, in some embedded applications, as the operating system) to make linear flash memory appear to the system like a disk drive, i.e., it emulates a HDD. This is achieved by creating "virtual" small blocks of data, or sectors, out of flash's large erase blocks and managing data on the flash so that it appears to be "write in place" when in fact it is being stored in different locations in the flash. FTL further manages the flash so that there are clean/ erased places to store data.

[0009] Given the limited number of writes that individual blocks within flash devices can tolerate, wear leveling algorithms are used within the flash devices (as firmware commonly known as FTL or managed by a controller) to attempt to ensure that "hot" blocks, i.e., blocks that are frequently written, are not rendered unusable much faster than other blocks. This task is

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