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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/006,299	06/12/2018	G.R. MOHAN RAO	GRTD60-34138	6732
	7590 01/24/201 SON MANDALA L.L.I		EXAMINER	
P.O. Drawer 800889			REIDLINGER, RONALD LANCE	
DALLAS, TX	75380		ART UNIT	PAPER NUMBER
			2824	
			NOTIFICATION DATE	DELIVERY MODE
			01/24/2019	ELECTRONIC

## Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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	Application No. 16/006,299	Applicant(s) RAO, G.R. MOHAN				
Office Action Summary	Examiner	Art Unit	AIA Status			
	R LANCE REIDLINGER	2824	No			
The MAILING DATE of this communication appears on the cover sheet with the correspondence address						
Period for Reply		•				
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) ✓ Responsive to communication(s) filed on 12 Ju	<u>une 2018</u> .					
☐ A declaration(s)/affidavit(s) under <b>37 CFR 1.130(b)</b> was/were filed on						
2a) This action is <b>FINAL</b> . 2b) <b>☑</b>	This action is non-final.					
3) An election was made by the applicant in response to a restriction requirement set forth during the interview on ; the restriction requirement and election have been incorporated into this action.						
4) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims*						
5) ☑ Claims 5) ☑ Claim(s) 1-9 is/are pending in the applica	ation					
5a) Of the above claim(s) is/are withdrawn from consideration.						
6) Claim(s) is/are allowed.						
7) Claim(s) 1-9 is/are rejected.						
8) Claim(s) is/are objected to.						
9) Claim(s) are subject to restriction and/or election requirement * If any claims have been determined allowable, you may be eligible to benefit from the <b>Patent Prosecution Highway</b> program at a						
participating intellectual property office for the corresponding a	•	_	way program at a			
http://www.uspto.gov/patents/init_events/pph/index.jsp or send						
	, ,					
Application Papers  10) The specification is objected to by the Examine	<u>a</u> r					
11) The drawing(s) filed on 12 June 2018 is/are: a) accepted or b) objected to by the Examiner.						
, = 0 , ,	•	-				
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).					
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  Certified copies:						
a) ☐ All b) ☐ Some** c) ☐ None of the	ne:					
1. Certified copies of the priority docume	ents have been received.					
2. Certified copies of the priority docume	ents have been received in Applic	cation No				
** See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
1) Volice of References Cited (PTO-892)	3) Interview Summary					
Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/S Paper No(s)/Mail Date	SB/08b) Paper No(s)/Mail D 4) Other:	ate				



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#### **DETAILED ACTION**

Claims 1-9 are pending.

Claim 1 is independent.

### Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

### Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

- 1. Determining the scope and contents of the prior art.
- 2. Ascertaining the differences between the prior art and the claims at issue.
- 3. Resolving the level of ordinary skill in the pertinent art.



4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-4 and 7-9 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al. (U.S. Patent Application Publication No. 2010/0172179, on record in parent application 13/455,267) in view of Goodson et al. ("Design Tradeoffs in a Flash Translation Layer," on record in parent application 13/455,267).

Regarding claim 1, Gorobets et al. teach,

A system for storing data (e.g. Fig. 20) comprising:

memory space containing volatile memory space (Fig. 15 Cache (RAM)) and nonvolatile memory space (Fig. 15, MLC Memory, including Main Memory and Binary Cache), wherein the nonvolatile memory space includes both multilevel cell (MLC) (Figs. 15, 20 Main Memory of MLC Memory) space (Figs. 15, 20 Main Memory of MLC Memory) and single level cell (SLC) space (Figs. 15, 20 Binary Cache of MLC Memory);

at least one controller (Fig. 8 Memory Manager No. 300; see also Fig. 15 Controller) to operate memory elements and associated memory space (Flash Memory No. 200);

at least one MLC nonvolatile memory element (Fig. 20 Main Portion MLC No. 2003; this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]);

at least one SLC nonvolatile memory element (Fig. 20 Binary Portion No. 2001; again, this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]);

at least one random access volatile memory element (see Fig. 15 Cache (RAM));

wherein the at least one controller (Fig. 8 Memory Manager No. 300; see also Fig. 15 Controller)

of both maintain an address table in one or more of the memory elements (see ¶ [0096]); and

wherein the address table maps logical and physical addresses (memory manager in the controller maps logical addresses to physical addresses, see ¶ [0096]) adaptable to the system, wherein



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the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories (see ¶ [0152-154], explaining the use of spare block pool management to increase lifetime of the memory device; mapping would be necessary to remap any logical address pointing to a retired block so that it points to a replacement block, or new physical address).

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Gorobets et al. explain address translation layers for flash memory, but do not describe the specific term "an FTL flash translation layer."

Nevertheless, Goodson et al. document the purpose and motivation for using FTL for a flash memory device (see Title, "Design Tradeoffs in a Flash Translation Layer," and §§ 1-2, which explain the purpose of flash translation layers).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Goodson et al. to the teachings of Gorobets et al. such that an FTL (as explained by Goodson et al.) is used with the flash devide taught by Gorobets et al. for the purpose of allowing the files system of the flash memory device to maintain the block interface of the disk without sacrificing the tighter integration and control over how the flash is managed and because it hides the complexity of the flash by providing a logical block interface for the flash device.

Regarding claims 2 and 9, Gorobets et al. explain that flash memory is most commonly provided in the form of a memory card (i.e., module or standalone unit as claimed) or a flash drive (i.e., module or standalone unit or hard drive, as claimed) (see background ¶ [0015]). Because Gorobets et al. embodiments involve flash memory, the provisions of being a module, standalone device or hard drive, as claimed, are met.

Regarding claim 3, Gorobets et al. teach at least one of the volatile or nonvolatile memories are embedded in the at least one controller (see Fig. 15 volatile Cache (RAM) 102 is embedded within Controller).



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