Trials@uspto.gov
571-272-7822

Paper 11
Date: April 11, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

VERVAIN, LLC,
Patent Owner.

IPR2021-01550
Patent 10,950,300 B2

Before SALLY C. MEDLEY, STACEY G. WHITE, and ROBERT J. WEINSCHENK, *Administrative Patent Judges*.

WHITE, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Micron Technology, Inc. ("Petitioner") filed a Petition requesting an *inter partes* review of claims 1–12 ("the challenged claims") of U.S. Patent No. 10,950,300 B2 (Ex. 1007, "the '300 patent"). Paper 1 ("Pet."). Vervain, LLC ("Patent Owner") filed a Preliminary Response. Paper 9 ("Prelim. Resp.").

Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in the petition "shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." The following findings of fact and conclusions of law are not final, but are made for the sole purpose of determining whether Petitioner meets the threshold for initiating review. Any final decision shall be based on the full trial record, including any response timely filed by Patent Owner. Any arguments not raised by Patent Owner in a timely-filed response may be deemed waived, even if they were presented in the Preliminary Response.

For the reasons stated below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one claim. We hereby institute an *inter partes* review as to all of the challenged claims of the '300 patent on all of the asserted grounds of unpatentability.

A. Related Matters

The '300 patent is part of a family of related patents including US 8,891,298 B2 ("'298 patent"); US 9,196,385 B2 ("'385 patent"); US 9,997,240 B2 ("'240 patent"). Ex. 1007, code (60). The parties indicate that the '300 patent and the related '298 patent, '385 patent, and '240 patent are the subject of the following district court proceedings: *Vervain, LLC v.*

Micron Technology, Inc. et al., No. 6:21-cv-00487 (W.D. Tex.) and *Vervain, LLC v. Western Digital Corporation et al.*, No. 6:21-cv-00488 (W.D. Tex.). Pet. 4–5; Paper 6, 2. The parties further indicate that the '298 patent is the subject of IPR2021-01547; the '385 patent is the subject of IPR2021-01548, and the '210 patent is the subject of IPR2021-01549. Pet. 5; Paper 6, 2–3.

B. The '300 Patent

The '300 patent is titled "Lifetime Mixed Level Non-Volatile Memory System." Ex. 1007, code (54). Generally, the '300 patent describes a system that stores data in a second memory bank, in the case that data which was stored in a first memory bank fails a data integrity test. *Id.* at 5:10–17. Figure 1 of the '300 patent is reproduced below.

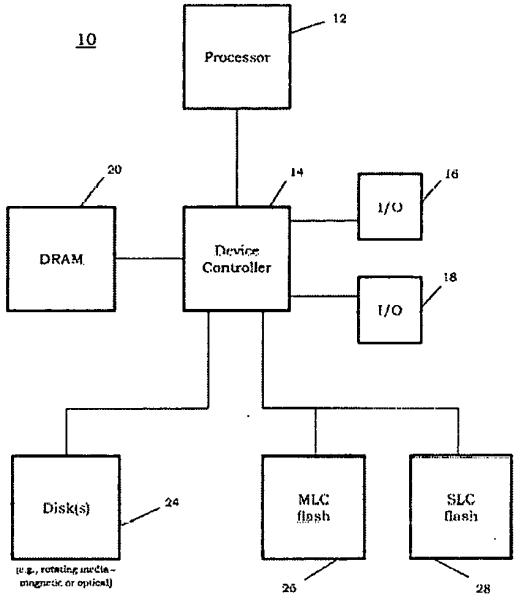

FIG. 1

Figure 1 shows a block diagram of a computer system 10 that stores, i.e., writes, data from dynamic random access memory ("DRAM") 20 onto non-volatile memory, e.g., multi-level cell ("MLC") NAND flash memory 26 or single-level cell ("SLC") NAND flash memory 28. Ex. 1007, 4:60–61, 6:17–20; *see id.* at 5:23–42. DRAM 20, MLC NAND flash

memory 26, and SLC NAND flash memory 28 are controlled by device controller 14. *Id.* at 5:34–42. Further, device controller 14 "acts as the memory controller" in a process which "write[s] a quantum of data stored in DRAM to a particular location in NAND flash memory." *Id.* at 6:17–22.

In the write process, "the quantum of data [to be written] is read from DRAM into memory within the device controller." *Id.* at 6:20–22. Then, the quantum of data is written to an identified physical address range in flash memory. *Id.* at 6:25–30; *see id.* Fig. 3A. In particular, the quantum of data initially is written to MLC NAND flash memory, rather than SLC NAND flash memory, because "MLC [NAND] flash memory is less expensive than SLC [NAND] flash memory." *Id.* at 5:51–60; *see id.* at 5:12–14.

Further, "[a]fter each write to an address within a particular address range," of the MLC NAND flash memory, "the device controller 14 will . . . perform a read on the address range to ensure the integrity of the written data." Ex. 1007, 5:61–64. In particular, the device controller compares "retained data representing" the quantum of data to be written with "newly stored data in the [MLC] NAND flash memory." *Id.* at 6:33–39; *see id.* Fig. 3B. If the data matches, "the write was a success." *Id.* at 6:38–40; *see id.* Fig. 3B. "However, if the retained data does not match the newly stored data in the [MLC] NAND flash memory," then a "quantum of available SLC NAND flash memory addresses" are identified, "the failed NAND flash physical address range is remapped to the next available quantum of SLC NAND flash memory," and the quantum of data is written to SLC NAND flash memory. *Id.* at 6:40–52, *see id.* Fig. 3B.

Additionally, in some embodiments, instead of device controller 15, "flash translation layer (FTL) 54 manages" the MLC and SLM NAND flash

memory banks and further conducts "control functions." *Id.* at 7:3–15 *see id.* Fig. 4.

C. Illustrative Claim

Of the challenged claims, claims 1 and 12 are independent. Claims 2–11 depend from claim 1. Claim 1 is illustrative.

1. A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space;

at least one controller to operate memory elements and associated memory space;

at least one MLC nonvolatile memory element that can be mapped into the MLC memory space;

at least one SLC nonvolatile memory element that can be mapped into the SLC memory space;

at least one random access volatile memory;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory;

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;

the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory;

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