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Paper 12
Date: September 15, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,
Petitioner,

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner.

IPR2023-00516
Patent 6,157,589

Before JEAN R. HOMERE, BARBARA A. PARVIS, and MINN CHUNG, *Administrative Patent Judges.*

CHUNG, *Administrative Patent Judge.*

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Xilinx, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1, 2, and 8–13 (the "challenged claims") of U.S. Patent No. 6,157,589 (Ex. 1001, "the '589 patent"). Polaris Innovations Limited ("Patent Owner") timely filed a Preliminary Response. Paper 11 ("Prelim. Resp.").

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). Under 35 U.S.C. § 314(a), institution of an *inter partes* review is authorized when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." Taking into account the arguments and evidence presented in Patent Owner's Preliminary Response, we determine that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail in showing the unpatentability of at least one challenged claim. Accordingly, we institute an *inter partes* review of all challenged claims of the '589 patent, based on all grounds raised in the Petition.

II. BACKGROUND

A. Related Matters

According to the parties, the '589 patent is involved in the following proceeding: *Polaris Innovations Ltd. v. Xilinx, Inc.*, No. 1:22-cv-00174-RGA (D. Del.). Pet. 1; Paper 3, 2. Patent Owner further states that the '589 patent is also the subject of *Polaris Innovations Limited v. Broadcom, Inc.*, No. 2:22-cv-00347 (E.D. Tex.). Paper 10, 2–3.

B. Real Parties-in-Interest

Petitioner identifies itself, Advanced Micro Devices, Inc., and ATI Technologies ULC as the real parties-in-interest. Pet. 1. Patent Owner identifies itself, Wi-LAN Inc., Owlpoint IP Opportunities JVF LP, and Quarterhill Inc. as the real parties-in-interest. Paper 10, 2.

C. The '589 Patent

The '589 patent issued December 5, 2000 from U.S. Patent Application No. 09/343,431, filed June 30, 1999. Ex. 1001, codes (21), (22), (45).

The '589 patent describes an initialization circuit for a dynamic semiconductor memory device ("DRAM"). *Id.* at 1:10–13, Abstract. As background, the '589 patent describes that for proper operation of a semiconductor memory device,

> it is necessary to ensure during the switch-on operation ("POWERUP") that the internal control circuits . . . are reliably held in a defined desired state, in order to prevent undesirable activation of output transistors that would cause, on the data lines, a short circuit (so-called "bus contention" or "data contention") or uncontrolled activation of internal current loads.

Id. at 1:23–30. According to the '589 patent, "[t]he solution to the problem turns out to be difficult" due to "a fundamental unpredictability of the time characteristic of the supply voltage and of the voltage level or levels at the external control inputs during the switch-on operation of the semiconductor memory." *Id.* at 1:30–35. The '589 patent describes that, to address this problem, the JEDEC standard for dynamic semiconductor memories specified that a predetermined initialization sequence of commands—e.g., a sequence comprising PRECHARGE, AUTOREFRESH, and

MODE-REGISTER-SET commands—must be applied in a defined chronological order before proper operation of the control circuits is allowed. *Id.* at 1:35–61. According to the '589 patent, "[a]fter the identification of such a defined initialization sequence, the memory module is normally in a so-called IDLE state . . . and prepared for proper operation"—i.e., "all the control circuits of the component have been unlatched." *Id.* at 1:62–67.

Against this backdrop, the '589 patent describes embodiments of a DRAM initialization circuit that contains a control circuit for controlling operations and an enable circuit that outputs an enable signal after identifying a predetermined proper initialization sequence of externally applied further command signals, the enable signal effecting an unlatching of the control circuit for proper operation of the semiconductor memory device. *Id.* at 2:15–37.

Figure 1 of the '589 patent is reproduced below.

Fig 1

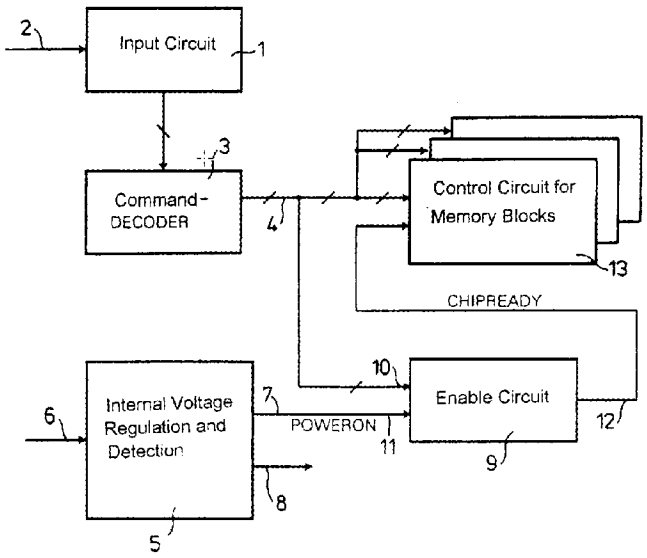

Figure 1 is a block diagram of components of the '589 patent's initialization circuit which controls a switching-on operation of a semiconductor memory operating according to the JEDEC standard. *Id.* at 3:28–31, 3:44–48.

With reference to Figure 1, the '589 patent describes:

> The initialization circuit has an input circuit 1, to whose input 2 command and clock signals that are externally applied in reference to the semiconductor memory are provided. The command and clock signals are amplified and conditioned before being received by a command decoder 3 connected downstream of the input circuit 1 and at whose output 4, inter alia, the command signals PRE or PRECHARGE (preparation command for word line activation), ARF or AUTOREFRESH (refresh command) and MRS or MODE-REGISTER-SET (loading configuration register command) are output.

Id. at 3:51–61. The initialization circuit further includes circuit 5 for internal voltage regulation and/or detection, which supplies an active POWERON signal if, after the POWERUP phase of the memory device, the internal supply voltages present at output 8 have reached the values necessary for proper operation of the component. *Id.* at 3:61–4:8.

According to the '589 patent,

> the initialization circuit furthermore has an enable circuit 9 connected downstream of the circuits 3 and 5. The command signals PRE, ARF and MRS are applied to an input 10 of the enable circuit 9 and the POWERON signal is applied to an input 11 of the enable circuit 9. An enable signal CHIPREADY is supplied at an output 12 of the enable circuit 9 after the identification of a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device is achieved. The enable signal effects unlatching of control circuits 13 provided for proper operation of the semiconductor memory device.

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