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UTILITY PATENT APPLICATION
UNDER 37 CFR 1.53(b)

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231
Sir:

Transmitted herewith for filing is the patent application of:

INVENTOR: Hideto HIDAKA
FOR: SEMICONDUCTOR MEMORY DEVICE WITH IMPROVED FLEXIBLE REDUNDANCY SCHEME

Enclosed are:

- ☒ 83 pages of specification, claims, abstract.
- ☒ Declaration and Power of Attorney.
- ☒ Priority Claimed.
- ☒ Certified copy of Japanese Patent Application No. 10-160466 and Japanese Patent Application No. 10-293421
- ☒ 31 sheets of formal drawing.
- ☒ An assignment of the invention to Mitsubishi Denki Kabushiki Kaisha and the assignment recordation fee.
- ☐ An associate power of attorney.
- ☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
- ☒ Information Disclosure Statement, Form PTO-1449 and reference.
- ☒ Return Receipt Postcard
- ☐

The filing fee has been calculated as shown below:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	20	-20	0	$18.00	$0.00
Independent Claims	4	-3	1	$78.00	$78.00
				Multiple Dependent Claim(s)	$0.00
				Basic Fee	$760.00
				Total of Above Calculations	$838.00
				Less ½ for Small Entity	$0.00
				Assignment & Recording Fee	$40.00
				Total Fee	$878.00

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Respectfully submitted,

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TITLE OF THE INVENTION

Semiconductor Memory Device with Improved Flexible Redundancy Scheme

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to semiconductor memory devices, and more particularly, to a semiconductor memory device having a memory array divided into a plurality of memory blocks. More specifically, the present invention relates to a redundancy circuit for repairing a defective memory cell in a semiconductor memory device having such an array-divided arrangement and a power supply circuit provided corresponding to each block.

Description of the Background Art

In the semiconductor memory device, a defective memory cell is replaced with a spare memory cell in order to equivalently repair the defective memory cell to raise the yield of the products. A flexible redundancy scheme has been proposed in order to improve the use efficiencies of spare lines (word lines or bit lines) and spare decoders for selecting spare lines in a redundancy circuit configuration including spare memory cells (spare word lines and bit lines) for repairing such defective memory cells (see, for example, "A Flexible Redundancy Technique for High-Density DRAM's", Horiguchi et al., IEEE Journal of Solid-State Circuits, Vol. 26, No. 1, January 1991, pp. 12 to 17).

Fig. 53 is a schematic diagram of the general configuration of a semiconductor memory device having a conventional flexible redundancy scheme. In Fig. 53, the semiconductor memory device includes four memory arrays MA0 to MA3. In each of memory arrays MA0 to MA3, a spare word line to repair a defective memory cell row is provided. In memory array MA0, spare word lines SW00 and SW01 are provided, and in memory array MA1, spare word lines SW10 and SW11 are provided. In memory array MA2, spare word line SW20 and SW21 are provided, and in memory array MA3, spare word lines SW30 and SW31 are provided.

Row decoders X0 to X3 each for decoding an address signal to drive a

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normal word line provided corresponding to an addressed row into a selected state are provided corresponding to memory arrays MA0 to MA3. A column decoder Y0 is provided between memory arrays MA0 and MA1 to decode a column address signal to select an addressed column, and also a column decoder Y1 is provided between memory arrays MA2 and MA3.

The semiconductor memory device further includes spare decoders SD0 to SD3 to store a row address at which a defective memory cell is present, maintain a word line (defective normal word line) corresponding to this defective row address in a non-selected state when the defective row is addressed and drive a corresponding spare word line into a selected state, an OR circuit G0 to receive output signals from spare decoders SD0 and SD1, and an OR circuit G1 to receive output signals from spare decoders SD2 and SD3.

The output signals of OR circuits G0 and G1 are provided in common to spare word line driving circuits included in row decoders X0 to X3. Spare decoders SD0 to SD3 are commonly provided with array address signal bits an-2 and an-1 to address one of memory arrays MA0 to MA3 and with intra-array address signals bits a0 to an-3 to address a row in the memory array. Row decoders X0 to X3 are provided with array address signal bits an-2 and an-1, and a row decoder is activated when a corresponding memory array is addressed. OR circuits G0 and G1 each correspond to two spare word lines provided for each of memory arrays MA0 to MA3.

Let us assume that normal word lines W0 and W1 are defective in memory array MA0, that a normal word line W2 in memory array MA1 is defective, and that a normal word line W3 in memory array MA2 is defective. In this state, the address of word line W0 is programmed in spare decoder SD0, while the address of word line W1 is programmed in spare decoder SD2. The address of normal word line W2 is programmed in spare decoder SD3, and the address of normal word line W3 is programmed in spare decoder SD1.

OR circuit G0 selects one of spare word lines SW00, SW10, SW20 and SW30, and the output signal of OR circuit G1 selects one of spare word

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lines SW1, SW11, SW21 and SW31.

When normal word line W0 is addressed, the output signal of spare decoder SD0 is driven into a selected state, and the output of OR circuit G0 is activated. In this state, array address signal bits an-2 and an-1 activate row decoder X0, and the remaining row decoders X1 to X3 are maintained in a non-active state. Thus, a word line driving circuit included in row decoder X0 drives spare word line SW00 into a selected state in response to the output signal of OR circuit G0. At this time, in row decoder X0, a decode circuit provided corresponding to normal word line W0 is maintained in a non-active state. As a result, defective normal word line W0 is replaced with spare word line SW00.

If defective normal word line W1 is addressed, the output signal of spare decoder SD2 attains an H level in a selected state, the output signal of OR circuit G1 attains an H level, and spare word line SW01 is selected. If defective normal word line W2 is addressed, the output signal of spare decoder SD3 attains an H level in a selected state, the output signal of OR circuit G1 attains an H level, and spare word line SW11 is selected. If defective normal word line W3 is addressed, the output signal of spare decoder SD1 attains an H level in a selected state, and spare word line SW20 is selected by OR circuit G0 accordingly. More specifically, defective normal word lines W0, W1, W2 and W3 are replaced with spare word lines SW00, SW01, SW11 and SW20, respectively.

In this flexible redundancy scheme shown in Fig. 53, a single spare word line can be activated by any of a plurality of spare decoders. For example, spare word line SW20 can be driven into a selected state by spare decoder SD0 or SD1. A single spare decoder can drive any of a plurality of spare word line into a selected state. For example, spare decoder SD0 can drive any of spare word lines SW00, SW10, SW20 and SW30 into a selected state. Thus, the spare word line and spare decoders do not correspond in one-to-one relation, and therefore the spare word lines and spare decoders can be more efficiently utilized. The number of spare word lines and the number of spare row decoders in a single memory array may be selected independently from each other as long as the numbers satisfy the following

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