EXHIBIT C

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Kim

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(54) **METHODS OF FORMING ETCH INHIBITING STRUCTURES ON FIELD ISOLATION REGIONS**

(75) Inventor: **Do-hyung Kim**, Seoul (KR)

(73) Assignee: **Samsung Electronics Co., Ltd.** (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/318,188**

(22) Filed: **May 25, 1999**

Related U.S. Application Data

(62) Division of application No. 08/748,148, filed on Nov. 12, 1996, now abandoned.

(30) **Foreign Application Priority Data**

Jun. 28, 1996 (KR) 96-25227

(51) **Int. Cl.**[7] **H01L 21/338**

(52) **U.S. Cl.** **438/183**; 438/926

(58) **Field of Search** 438/183, 926, 438/740, 233, 439

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Primary Examiner—Olik Chaudhuri
Assistant Examiner—Phat X. Cao
(74) *Attorney, Agent, or Firm*—Myers Bigel Sibley & Sajovec

(57) **ABSTRACT**

A microelectronic structure includes a substrate having adjacent active and field regions. A field isolation layer covers the field region, and an etch inhibiting layer is provided on the field isolation layer adjacent the active region of the substrate. An insulating layer covers the substrate, the field isolation layer, and the etch inhibiting layer, and the insulating layer defines a contact hole therein exposing a portion of the active region adjacent the etch inhibiting layer. Related methods are also discussed.

18 Claims, 2 Drawing Sheets

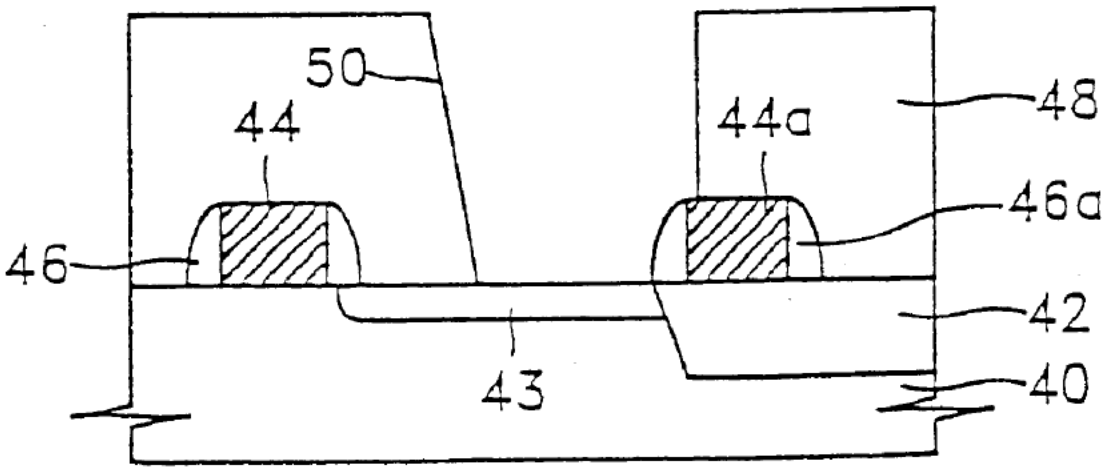


FIG. 1
(PRIOR ART)

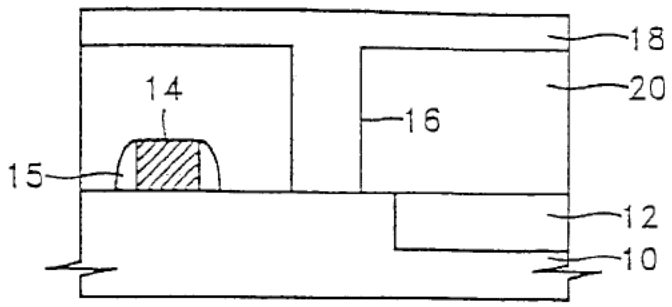


FIG. 2
(PRIOR ART)

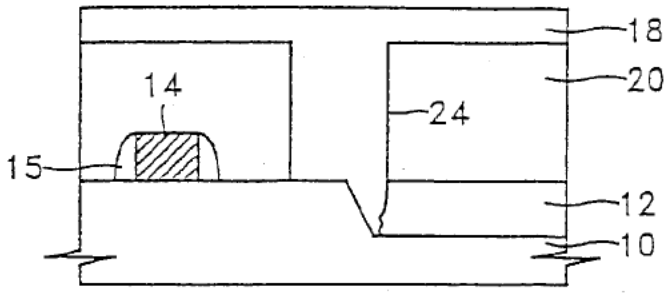


FIG. 3
(PRIOR ART)

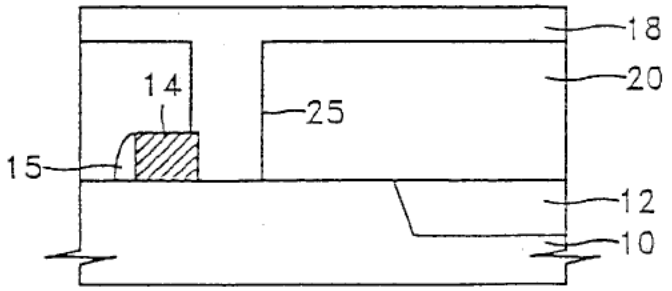


FIG. 4

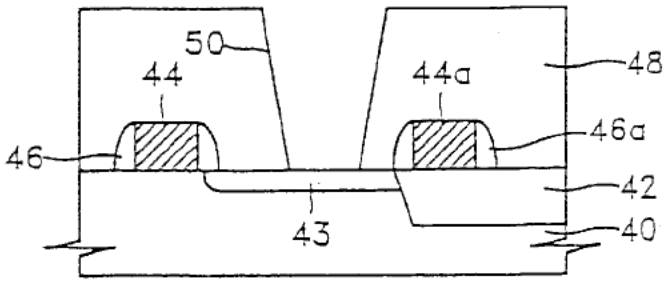


FIG. 5

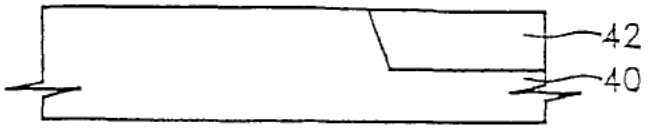


FIG. 6

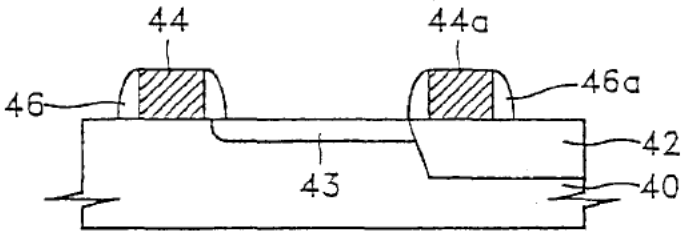


FIG. 7

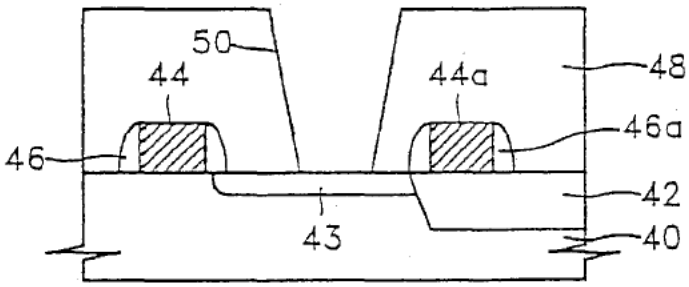
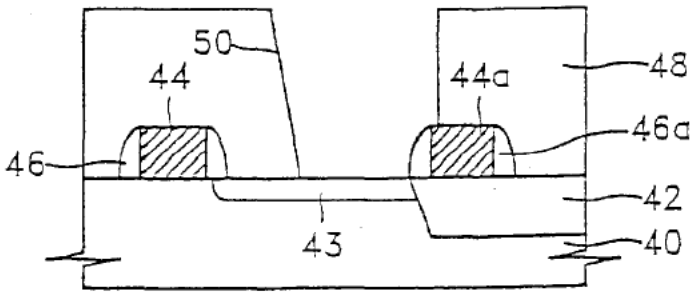


FIG. 8



METHODS OF FORMING ETCH INHIBITING STRUCTURES ON FIELD ISOLATION REGIONS

This application is a divisional application of U.S. patent application Ser. No. 08/748,148 filed Nov. 12, 1996, abandoned, and entitled ETCH INHIBITING STRUCTURES ON FIELD ISOLATION REGIONS AND RELATED METHODS.

FIELD OF THE INVENTION

The present invention relates to microelectronic structures and methods and more particularly to microelectronic structures and methods including isolation regions.

BACKGROUND OF THE INVENTION

As integrated circuit devices become more highly integrated, the space available for individual devices formed thereon is reduced. Accordingly, the sizes of patterns such as gates, bit lines, and metal lines formed on integrated circuits are generally reduced. Furthermore, space between these patterns is also generally reduced.

In particular, integrated circuit memory devices include a plurality of memory cells, and each memory cell is connected to other cells by conductive (metal) lines. The cells and conductive (metal) lines are connected to the substrate or other conductive layers by contact holes or via holes. The contact holes expose active regions of the substrate and the via holes expose the surface of other conductive layers. Patterned layers such as the gate electrodes should be isolated from the holes, and these patterned layers are generally arranged around the holes. Accordingly, the holes must be accurately placed in order to maintain electrical isolation with respect to the patterned layers such as the gate electrodes.

As the space between these patterned layers is reduced, however, the space available for forming the holes may also be reduced. Furthermore, there may be physical limits to the reductions which can be made to the size of the holes. Accordingly, the increased integration reduces the margin available in the placement of the holes. The margin available for the placement of the holes is also influenced by the process limitations of the steps for forming other adjacent patterns. For example, when a LOCOS field oxide layer is formed, the bird's beak phenomenon may reduce the active region. When a trench field oxide layer is formed, the inner wall of the trench may encroach into the active region also reducing the area available to the hole and further decreasing the margin for the formation of the hole.

FIG. **1** is a cross-sectional view of an integrated circuit device having a contact hole **16**. The field oxide layer **12** is formed on the semiconductor substrate **10**, and the gate electrode **14** is formed on an active region defined by the field oxide layer **12**. Spacers **15** are formed along the sidewalls of the gate electrode **14**. An insulating layer **20** is then formed on the surface of the substrate including the gate electrode **14** and the field oxide layer **12**, and the contact hole **16** is formed therein to expose a portion of the active region of the substrate. The conductive layer **18** is formed on the insulating layer **20** thus filling the contact hole **16**. The contact hole **16** is preferably formed over the active region between the gate electrode **14** and the field oxide film **12** so that neither the gate electrode **14** nor the field oxide film **12** is exposed.

While the contact hole **16** is shown centered between the gate electrode **14** and the field oxide layer **12** in FIG. **1**, it

may become more difficult to form the contact hole between these structures as the device integration increases. As the spaces become smaller, formation of the contact hole **16** may be limited by the physical characteristics of light and the ability to properly align the mask. Accordingly, the margin for error during the formation of the contact hole is reduced. As shown in FIGS. **2** and **3**, misalignment of the contact hole photomask may cause the contact hole to expose either the gate electrode **14** or the field oxide layer **12**.

As shown in FIG. **2**, the misaligned contact hole **24** exposes a portion of the active region as well as a portion of the field region. This misalignment may also result in the formation of a well through the field oxide layer **12** thus exposing a portion of a field region of the substrate when etching the insulating film **20**. In other words, a contact hole **24** may partially expose an active region of the substrate and a well in the field region of the substrate. Accordingly, when the contact hole **24** is filled with the conductive layer **18**, the conductive layer **18** is brought into contact with the well. Leakage current may thus flow through the conductive layer **18** into the well area. The integrated circuit device may thus overload leading to a delay in the operation of the device or even a malfunction. If a capacitor is formed, the life of the capacitor may also be reduced.

In FIG. **3**, a misaligned contact hole exposes a portion of the gate electrode **14**. Accordingly, the conductive layer **18** filling the contact hole **25** may contact the gate electrode **14** thus short circuiting the device. The reliability of the integrated circuit device may thus be reduced.

As discussed above, margins for forming contact holes are reduced as device integration increases. For example, the extension of a gate or a field region may reduce the area available for a contact hole, thus reducing the process margins. The reduction of process margins in turn causes a reduction in the alignment margin for the photomask used to form the contact hole. Accordingly, alignment of the photomask may become more difficult. The contact holes for integrated circuit devices may thus be more difficult to form and the alignment thereof may also be more difficult.

Accordingly, there continues to exist a need in the art for improved contact hole structures and related methods.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide improved contact hole structures and methods.

It is still another object of the present invention to provide increased alignment tolerances for the formation of contact holes.

These and other objects are provided according to the present invention by structures and methods wherein an etch inhibiting layer is provided on a field isolation layer adjacent the active region of the substrate. This etch inhibiting layer allows the misalignment of the contact hole without damaging the field isolation, layer. Accordingly, the yield and reliability of integrated circuit devices formed according to the present invention can be increased at a given level of integration.

In particular, a microelectronic structure includes a substrate having active and field regions and a field isolation layer which covers the field region, and first and second patterned conductive layers. The first patterned conductive layer is on the active region of the substrate spaced apart from the field region, and the second patterned conductive layer is on the field isolation layer adjacent the active region of the substrate. The second patterned conductive layer thus acts as the etch inhibiting layer protecting the field isolation layer.

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