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# EXHIBIT C

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## (12) United States Patent Rajappa et al.

# (10) Patent No.: US 6,378,082 B1

## (45) Date of Patent: Apr. 23, 2002

### (54) GENERATING STROBE SIGNALS AT DIFFERENT VOLTAGE LEVEL MODES FOR RECEIVING DATA AT GRAPHICS INTERFACE PORT

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- (73) Assignee: Intel Corporation, Santa Clara, CA (US)
- (\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.
- (21) Appl. No.: 09/345,711
- (22) Filed: Jun. 30, 1999
- (51) Int. Cl.<sup>7</sup> ..... G06F 1/06
- (52) U.S. Cl. ..... 713/501; 713/400; 713/600

### (56) **References Cited**

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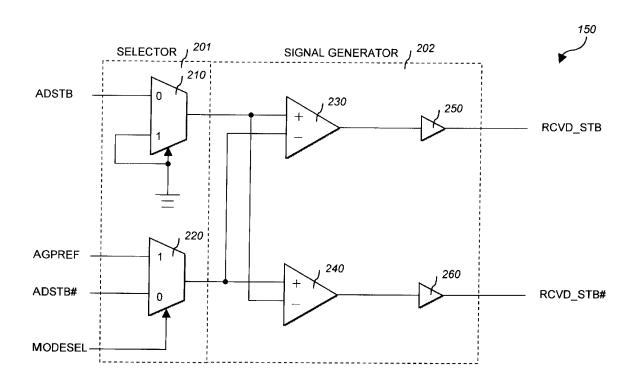
Primary Examiner-Kenneth S. Kim

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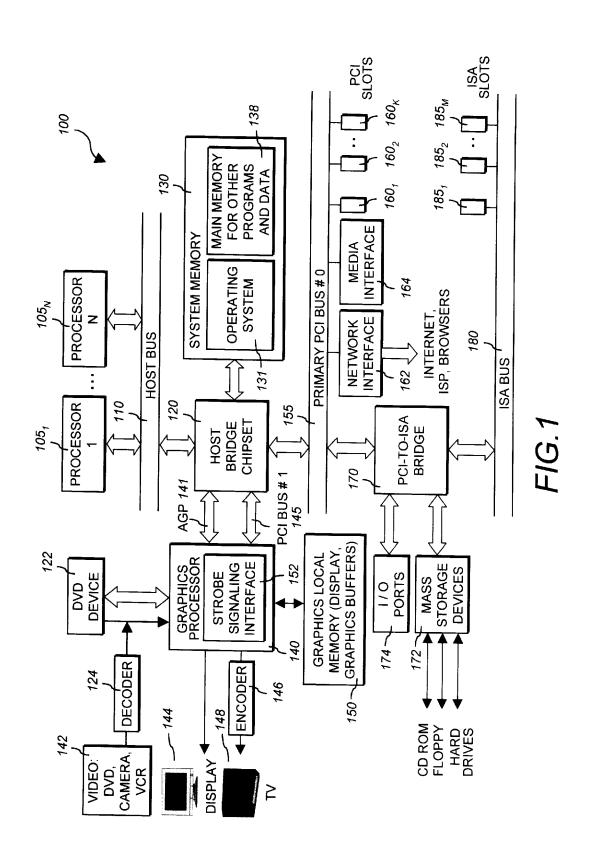
### (57) ABSTRACT

The present invention is a method and apparatus to generate first and second strobe signals to receive data on an interface port of a processor operating in first and second modes at first and second voltage levels, respectively. The second voltage level is higher than the first voltage level. A selector provides first and second selected signals from a plurality of signals which corresponds to the first and second modes. The selector operates at the second voltage level. A signal generator is coupled to the selector to generate the first and second strobe signals from the first and second selected signals.

### 30 Claims, 4 Drawing Sheets



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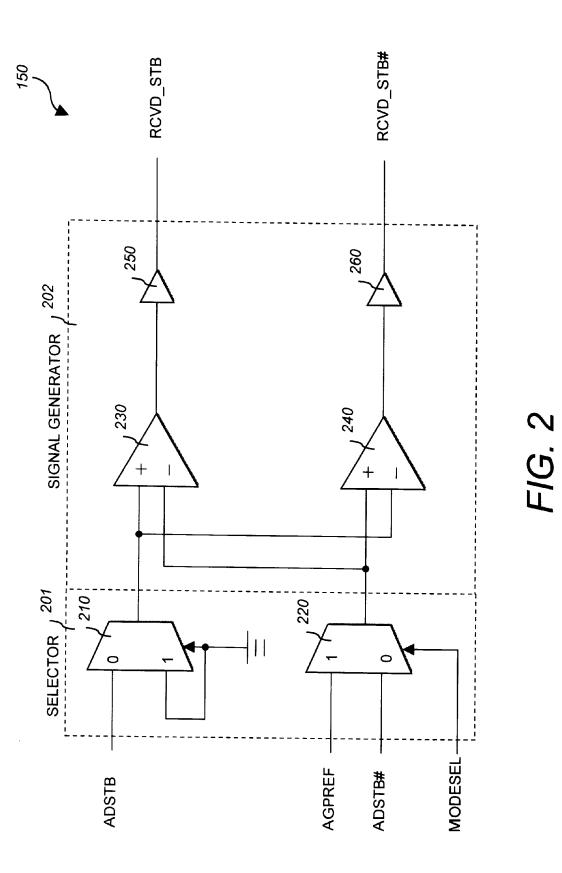
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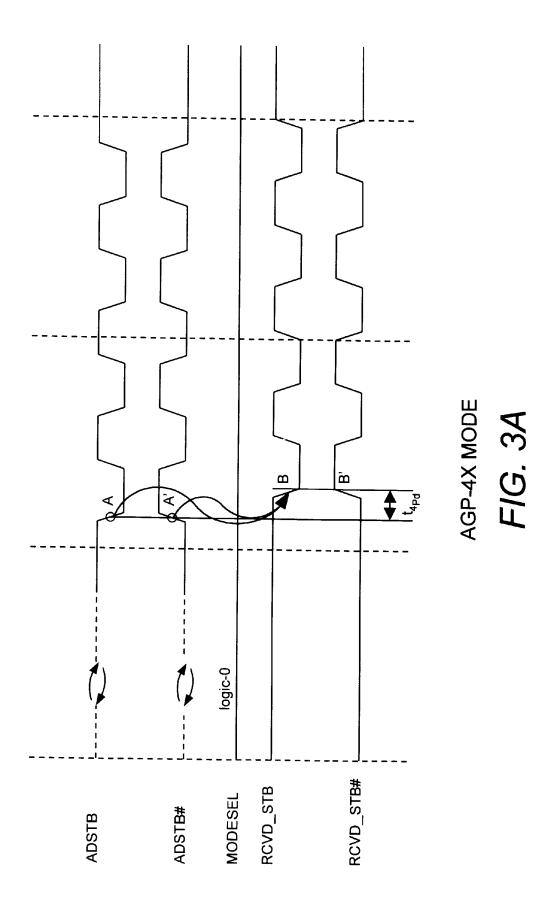
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