# EXHIBIT A

US005778434A

# United States Patent [19]

Nguyen et al.

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[45] Date of Patent: Jul. 7, 1998

[54] **SYSTEM AND METHOD FOR PROCESSING MULTIPLE REQUESTS AND OUT OF ORDER RETURNS**

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[21] Appl. No.: **479,035**

[22] Filed: **Jun. 7, 1995**

[51] **Int. Cl.**[6] ..... **G06F 12/00**

[52] **U.S. Cl.** ..... **711/137**; 711/146

[58] **Field of Search** ..... 395/464, 473; 711/137, 146

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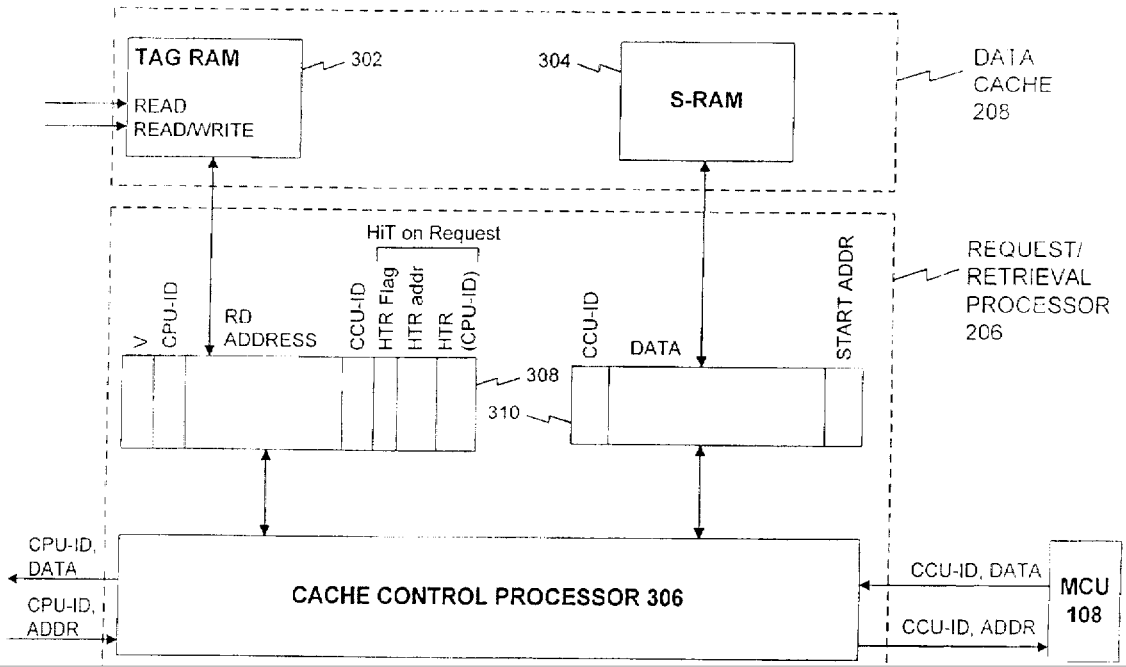
[57] **ABSTRACT**

A system and method for processing a sequence of requests for data by one or more central processing units (CPUs) after cache misses. Each CPU request includes a CPU-ID tag identifying the CPU issuing the request for data and an address identifying a location in lower-level memory where the data is stored. Cache-control ID tags are assigned to identify the locations in the request queue of the respective CPU-ID tags associated with each CPU request. Cache-control requests consisting of the cache-control ID tags and the respective address information are sent from the request queue to the lower-level memory or storage devices. Data is then returned along with the corresponding CCU-ID tags in the order in which it is returned by the storage devices. Finally, the sequence of CPU requests for data is fulfilled by returning the data and CPU-ID tag in the order in which the data was returned from lower-level memory. By issuing multiple requests for data and allowing out of order data return, data is retrieved from lower-level memory after cache misses more quickly and efficiently than processing data requests in sequence. By checking the request queue, pending CPU requests for the same data including requests for the same long word of data can be identified. Cache hits for multiple requests are determined by simultaneously checking sets in cache memory. Multiple instructions are then issued for multiple superset cache hits.

**19 Claims, 11 Drawing Sheets**



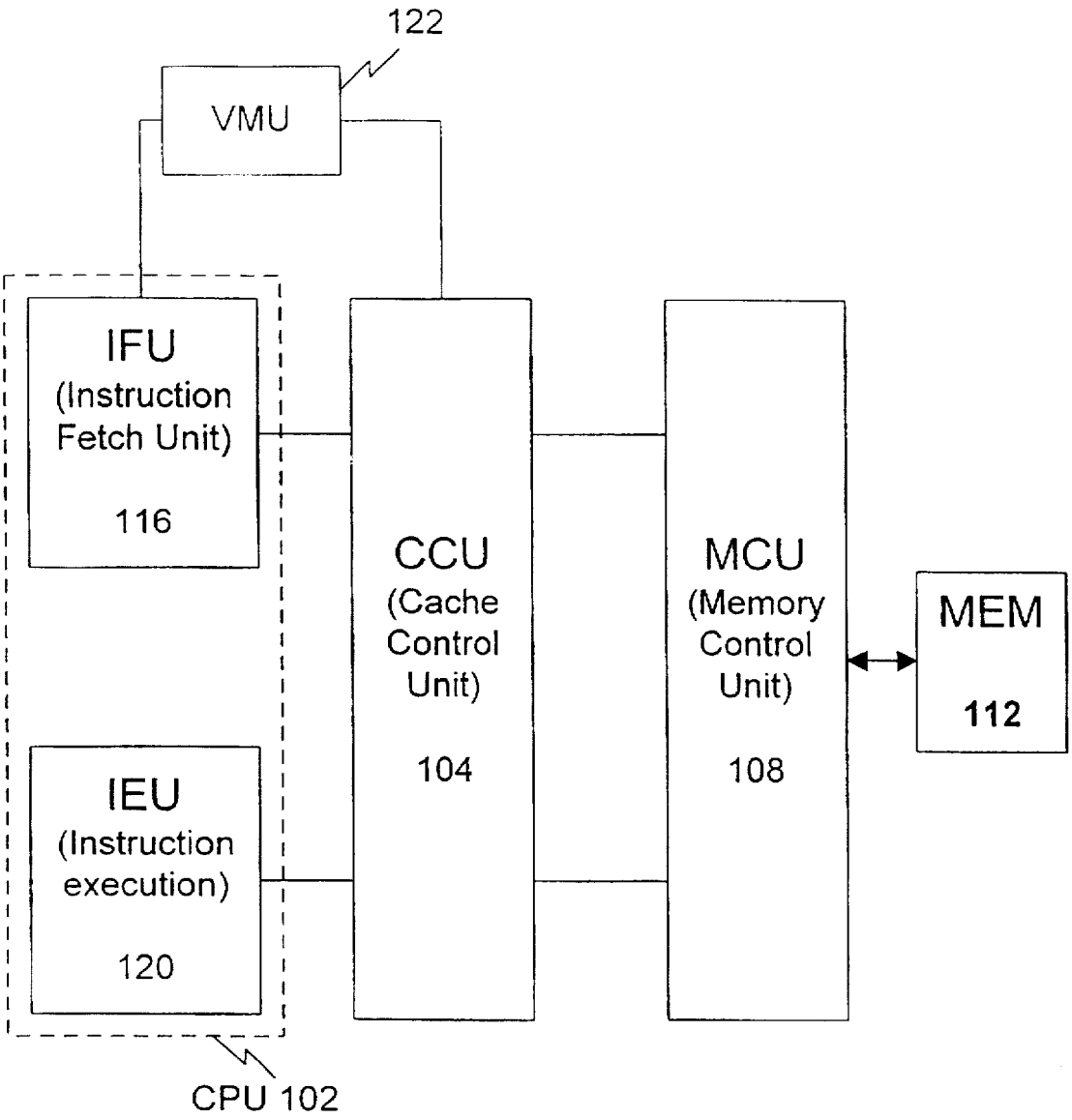



FIG. 1

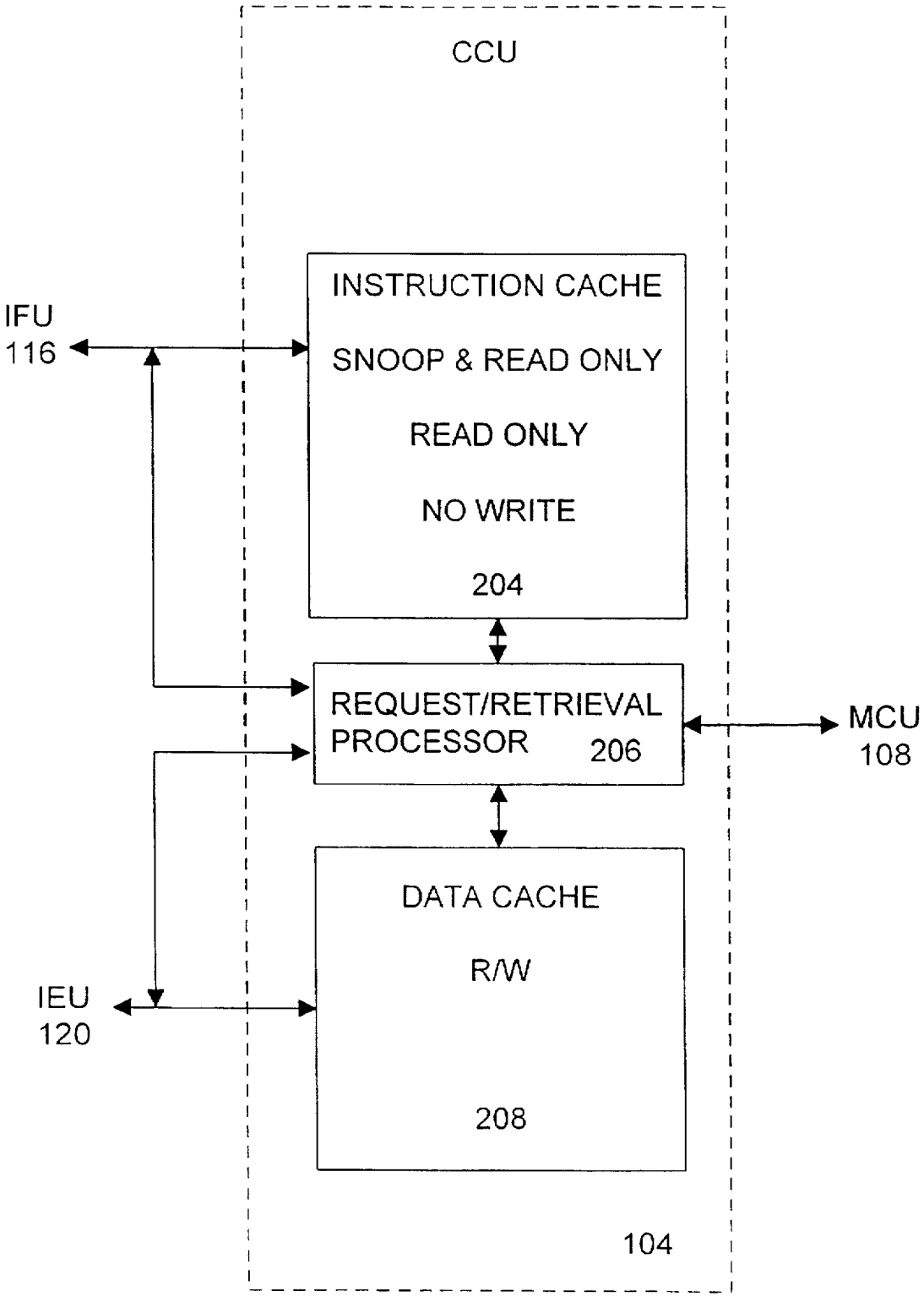



FIG. 2

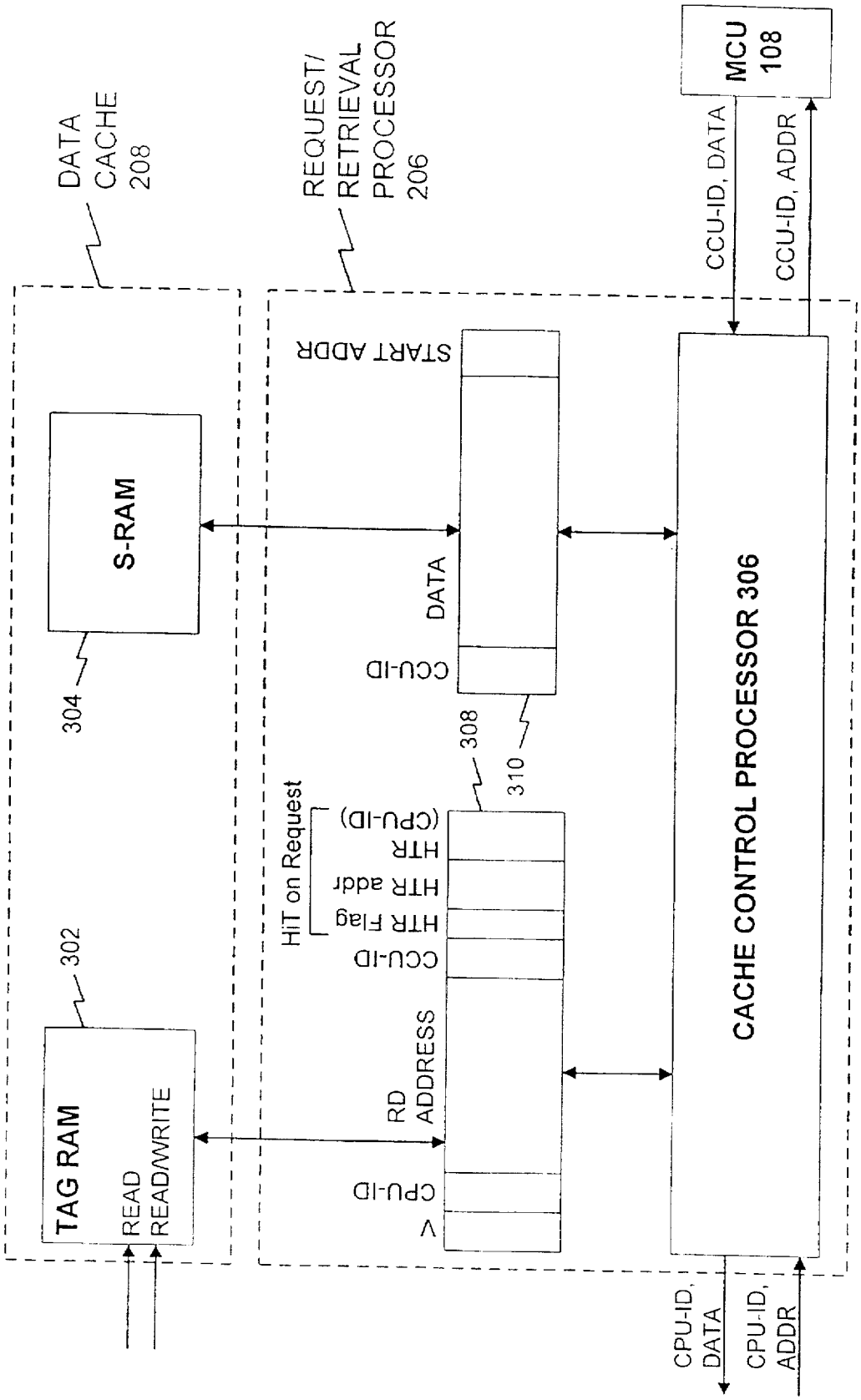



FIG. 3

DOCKET ALARM

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