EXHIBIT E

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Lee et al.

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(54) **METHODS OF FORMING CMOS TRANSISTORS WITH HIGH CONDUCTIVITY GATE ELECTRODES**

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(58) **Field of Classification Search** 438/296
See application file for complete search history.

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(57) **ABSTRACT**

Provided is a method for manufacturing a MOS transistor. The method comprises providing a substrate having a first active region and a second active region; forming a dummy gate stack on the first active region and the second active region, the dummy gate stack comprising a gate dielectric layer and a dummy gate electrode; forming source/drain regions in the first active region and the second active region disposed at both sides of the dummy gate stack; forming a mold insulating layer on the source/drain region; removing the dummy gate electrode on the first active region to form a first trench on the mold insulating layer; forming a first metal pattern to form a second trench at a lower portion of the first trench, and removing the dummy gate electrode on the second active region to from a third trench on the mold insulating layer; and forming a second metal layer in the second trench and the third trench to form a first gate electrode on the first active region and a second gate electrode on the second active region.

15 Claims, 19 Drawing Sheets

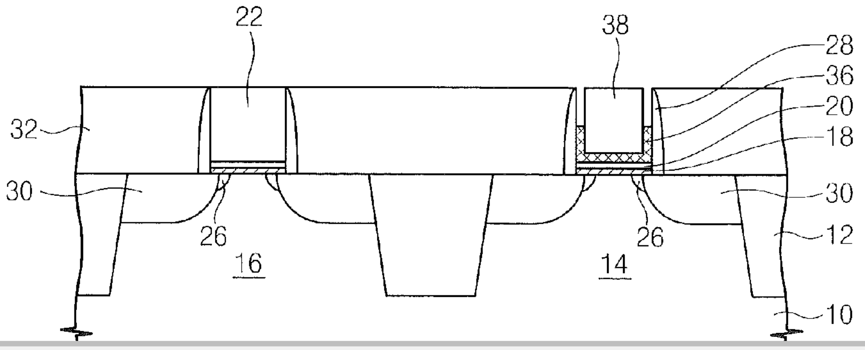

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Fig. 1

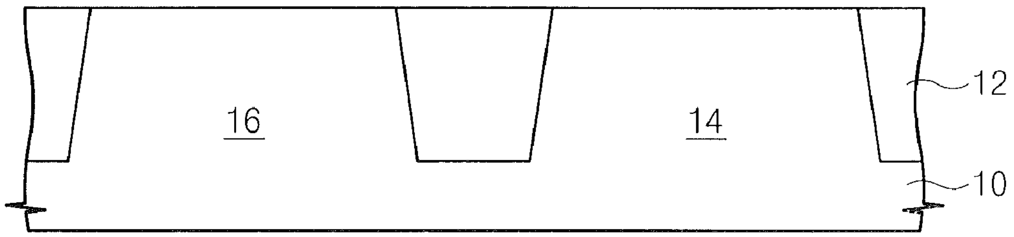


Fig. 2

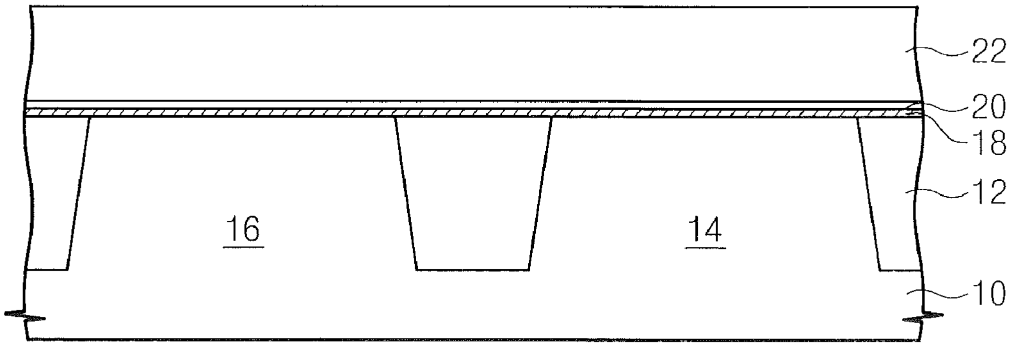


Fig. 3

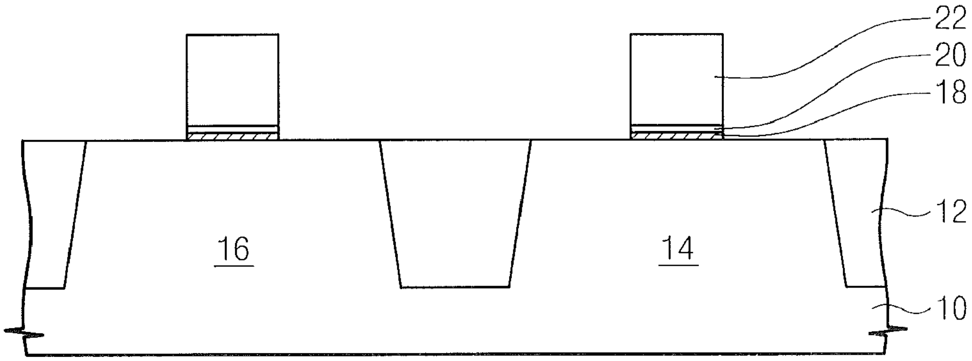
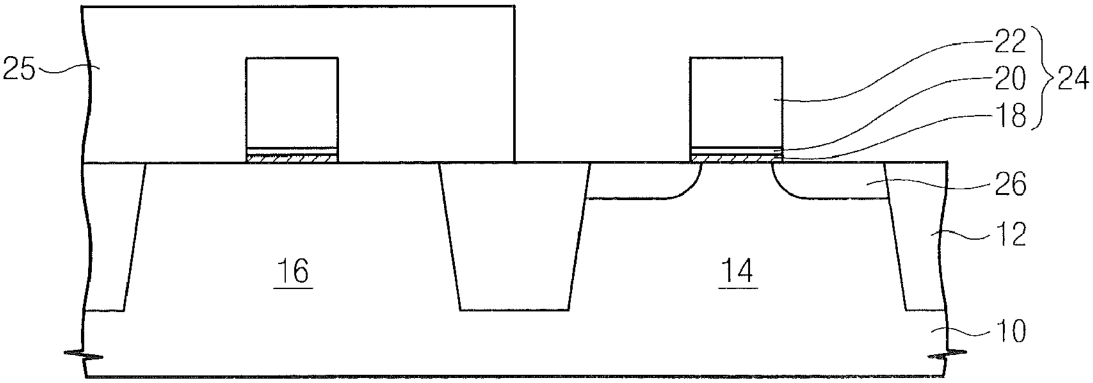


Fig. 4



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