EXHIBIT D

US006819602B2

(12) United States Patent Seo et al.

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(54) MULTIMODE DATA BUFFER AND METHOD FOR CONTROLLING PROPAGATION DELAY TIME

(75) Inventors: Seong-young Seo, Suwon (KR);

Jung-bae Lee, Yongin (KR); Byong-mo

Moon, Seoul (KR)

(73) Assignee: Samsung Electronics Co., Ltd.,

Kyungki-Do (KR)

(*) Notice: Subject to any disclaimer, the term of this

patent is extended or adjusted under 35

U.S.C. 154(b) by 77 days.

(21) Appl. No.: 10/278,071

(22) Filed: Oct. 23, 2002

(65) **Prior Publication Data**

US 2003/0210575 A1 Nov. 13, 2003

Related U.S. Application Data

(60)	Provisional	application	No.	60/379,665,	filed	on	May	10,
	2002.							

(51)	Int. Cl.		G11C	7/00
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(52) **U.S. Cl.** **365/193**; 365/189.05; 365/191; 365/194

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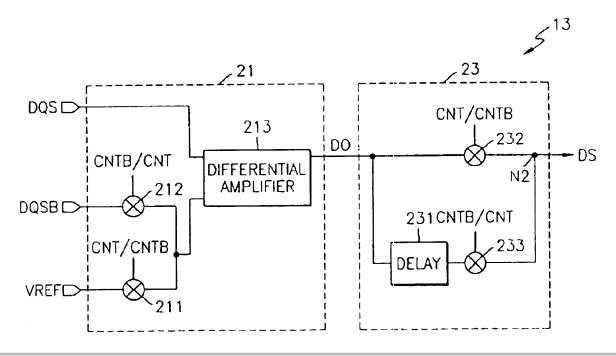
^{*} cited by examiner

Primary Examiner—Van Thu Nguyen (74) Attorney, Agent, or Firm—Harness, Dickey & Pierce, P.L.C.

(57) ABSTRACT

A data buffer, such as a data strobe input buffer or a data input buffer, which may operate in multiple modes, such as a single mode (SM) and a dual mode (DM) and where the mode is selected by providing a signal, such as an external signal such as an address signal or an external command signal. A data buffer which can be used for a SM/DM dual-use and can improve a data setup/hold margin. A semiconductor memory device including one or more of the data buffers described above. A method for controlling propagation delay times which can improve a data setup/hold margin in a SM/DM dual-use data buffer.

29 Claims, 13 Drawing Sheets





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FIG. 1 Prior Art

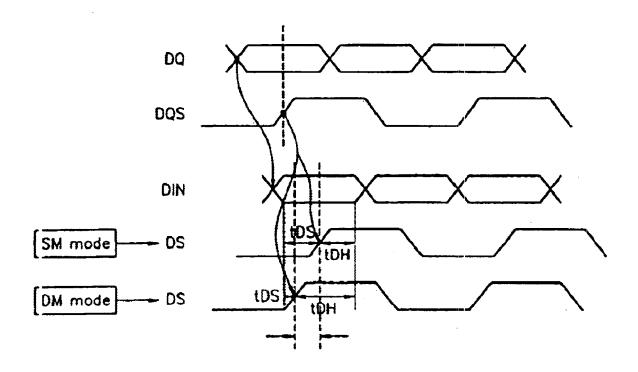
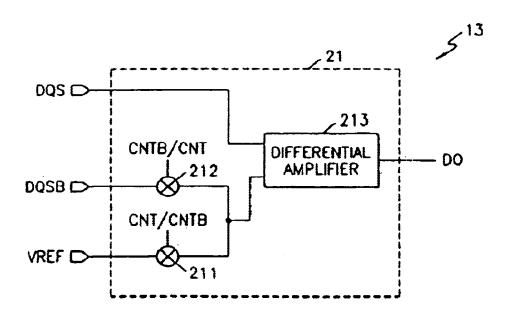


FIG. 2





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FIG. 3A

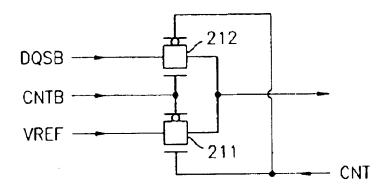


FIG. 3B

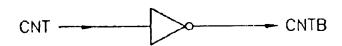
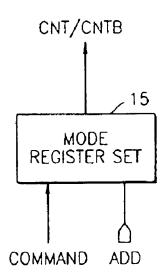


FIG. 4





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FIG. 5A

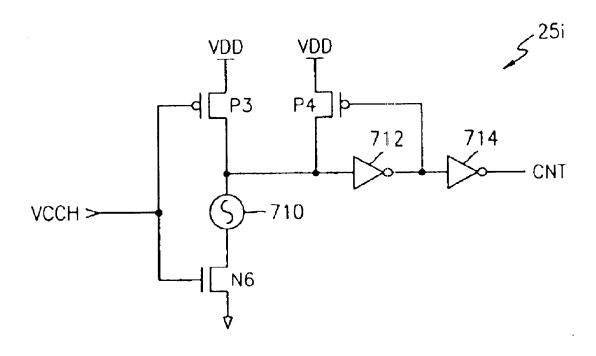
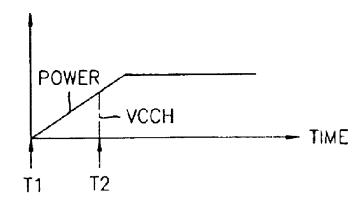


FIG. 5B

VOLTAGE LEVEL





DOCKET

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