EXHIBIT B

US006262938B1

(12) **United States Patent**
Lee et al.

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(45) **Date of Patent: Jul. 17, 2001**

(54) **SYNCHRONOUS DRAM HAVING POSTED CAS LATENCY AND METHOD FOR CONTROLLING CAS LATENCY**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/518,144**

(22) Filed: **Mar. 3, 2000**

(30) **Foreign Application Priority Data**

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Jun. 5, 1999 (KR) 99-20821

(51) **Int. Cl.**[7] **G11C 8/00**

(52) **U.S. Cl.** **365/233**; 365/194; 365/240; 365/236

(58) **Field of Search** 365/78, 194, 205, 365/230.02, 230.03, 236, 240, 233

(56) **References Cited**

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(57) **ABSTRACT**

A synchronous DRAM (SDRAM) having a posted column access strobe (CAS) latency and a method of controlling CAS latency are provided. In order to control a delay time from the application of a CAS command and a column address to the beginning of memory, reading or writing operations in units of clock cycles, a first method of programing the delay time as a mode register set (MRS) and a second method of detecting the delay time using an internal signal and an external signal, are provided. In the second method, the SDRAM can include a counter for controlling the CAS latency. This counter controls the CAS latency of the SDRAM by generating a signal for controlling the CAS latency according to the number of clock cycles of a clock signal from the generation of a row access command to a column access command in the same memory bank and reading the signal. It is therefore possible to appropriately perform a posted CAS latency operation and a general CAS latency operation by the SDRAM without an additional MRS command according to this SDRAM and the method of controlling the CAS latency.

24 Claims, 11 Drawing Sheets

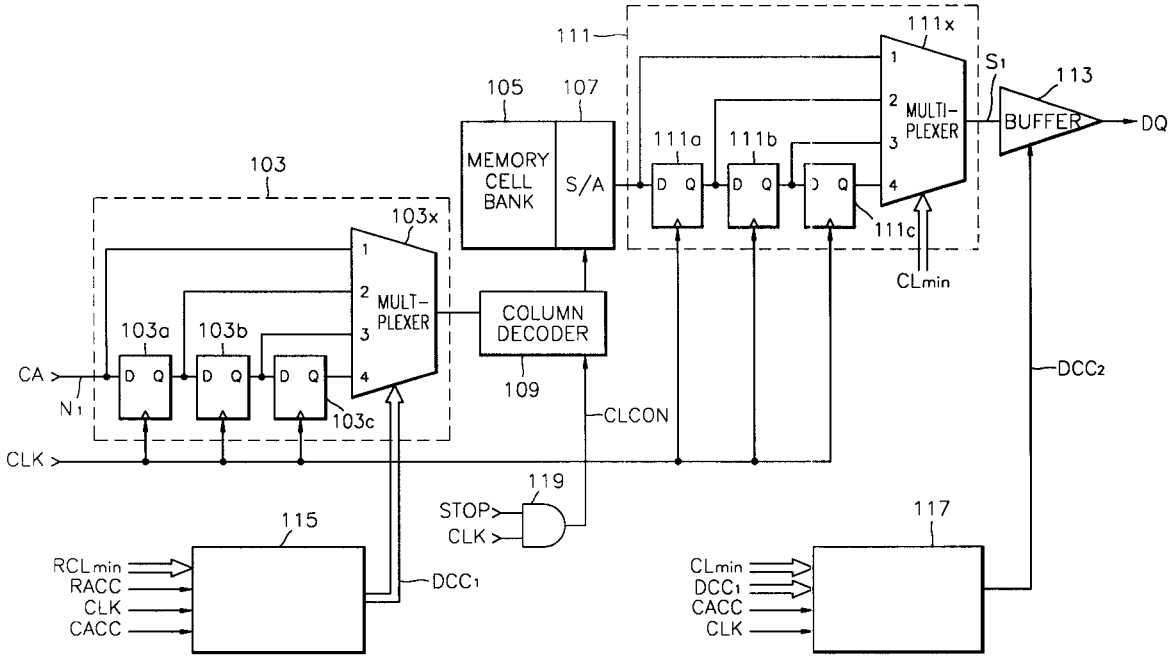


FIG. 1

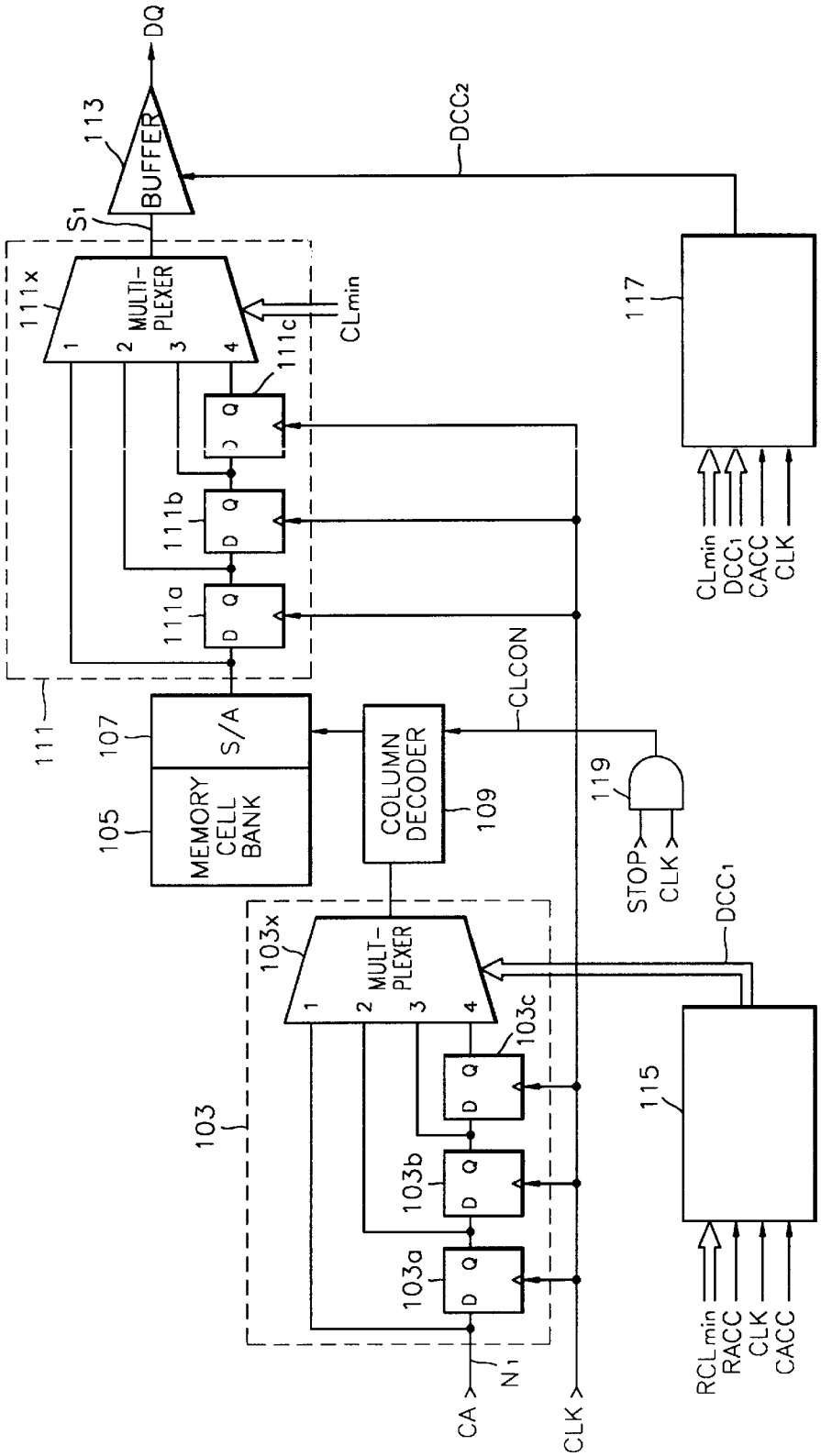


FIG. 2

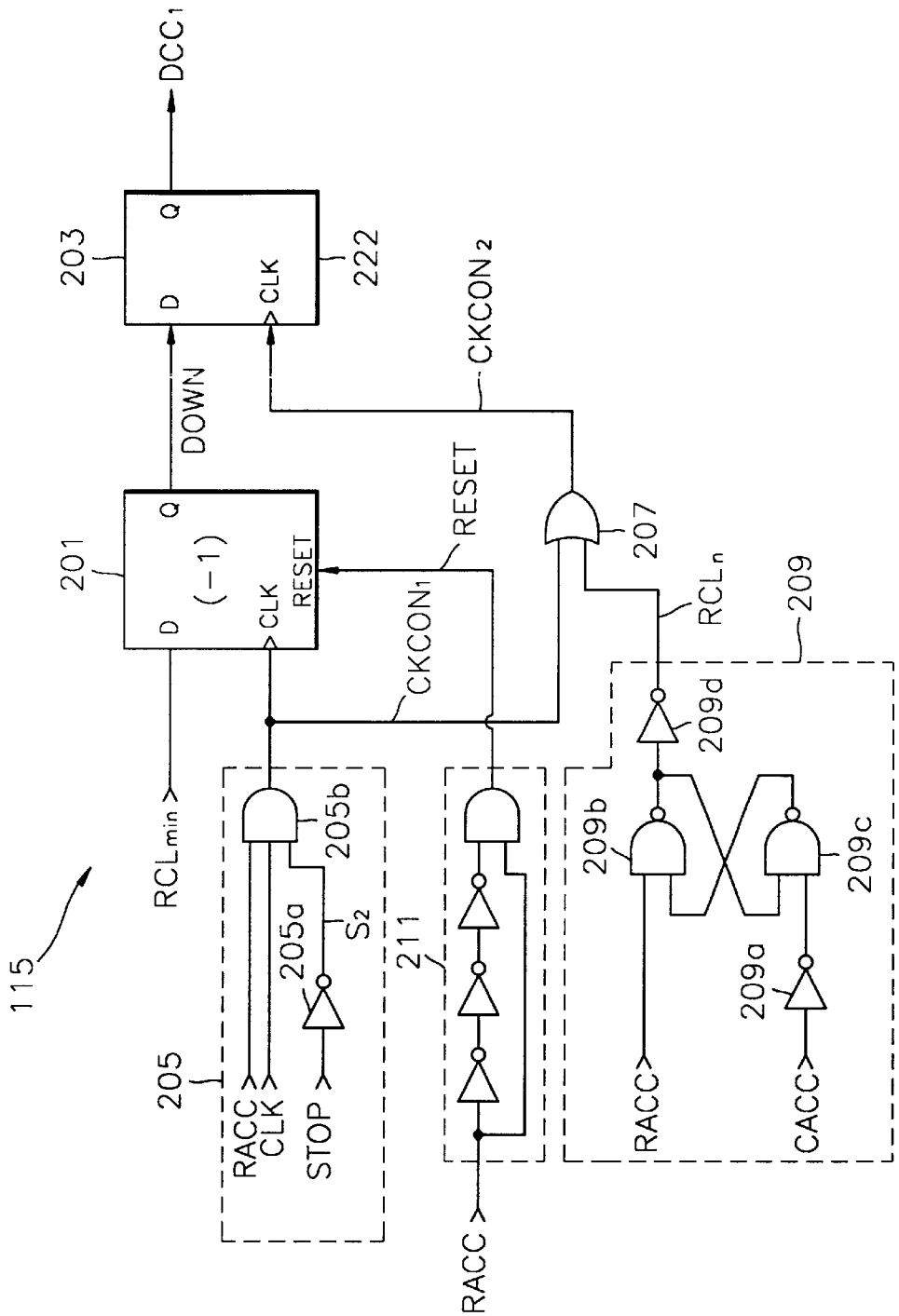
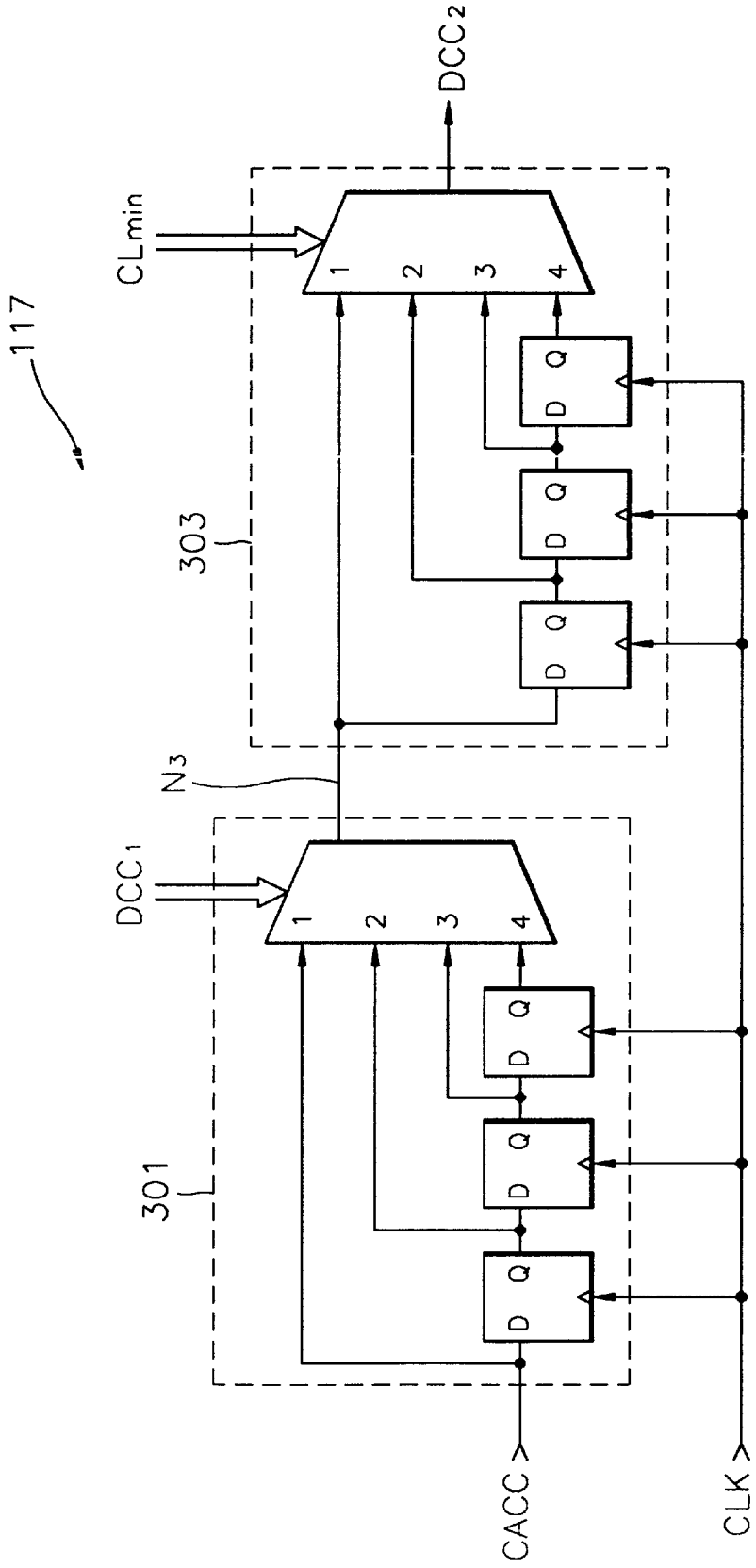


FIG. 3



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