

EXHIBIT A

US005860158A

United States Patent [19]

[11] **Patent Number:** **5,860,158**

Pai et al.

[45] **Date of Patent:** **Jan. 12, 1999**

[54] **CACHE CONTROL UNIT WITH A CACHE REQUEST TRANSACTION-ORIENTED PROTOCOL**

4,899,275	2/1990	Sachs et al.	711/3
5,377,345	12/1994	Chang et al.	395/425
5,418,973	5/1995	Ellis et al.	395/800
5,524,265	6/1996	Balmer et al.	711/212
5,574,849	11/1996	Sonnier et al.	395/182.1
5,659,782	8/1997	Senter et al.	395/800.23

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[21] Appl. No.: **751,149**

[57] **ABSTRACT**

[22] Filed: **Nov. 15, 1996**

A cache control unit and a method of controlling a cache. The cache is coupled to a cache accessing device. A first cache request is received from the device. A request identification information is assigned to the first cache request and provided to the requesting device. The first cache request may begin to be processed. A second cache request is received from the cache accessing device. The second cache request is assigned to the first cache request and provided to the requesting device. The first and second cache requests are finally fully serviced.

[51] **Int. Cl.⁶** **G06F 13/00**

[52] **U.S. Cl.** **711/118; 711/130**

[58] **Field of Search** 711/119, 120, 711/130, 140, 118

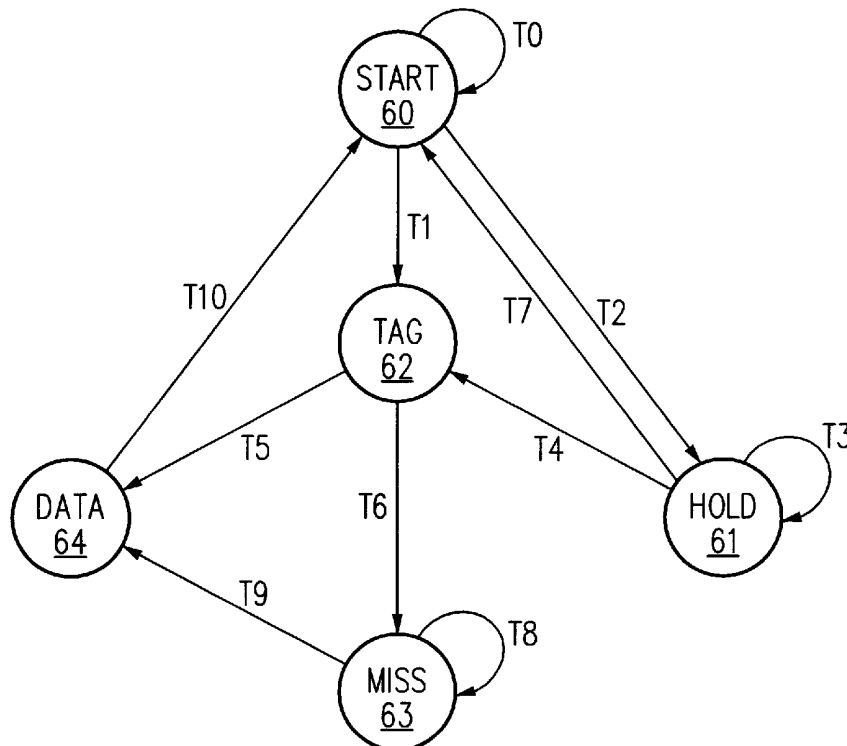
[56] **References Cited**

U.S. PATENT DOCUMENTS

4,695,943	9/1987	Keeley et al.	711/140
4,701,844	10/1987	Thompson et al.	711/119
4,707,784	11/1987	Ryan et al.	711/140

37 Claims, 8 Drawing Sheets

ARM_CCU INTERFACE STATE MACHINE (A_SM)



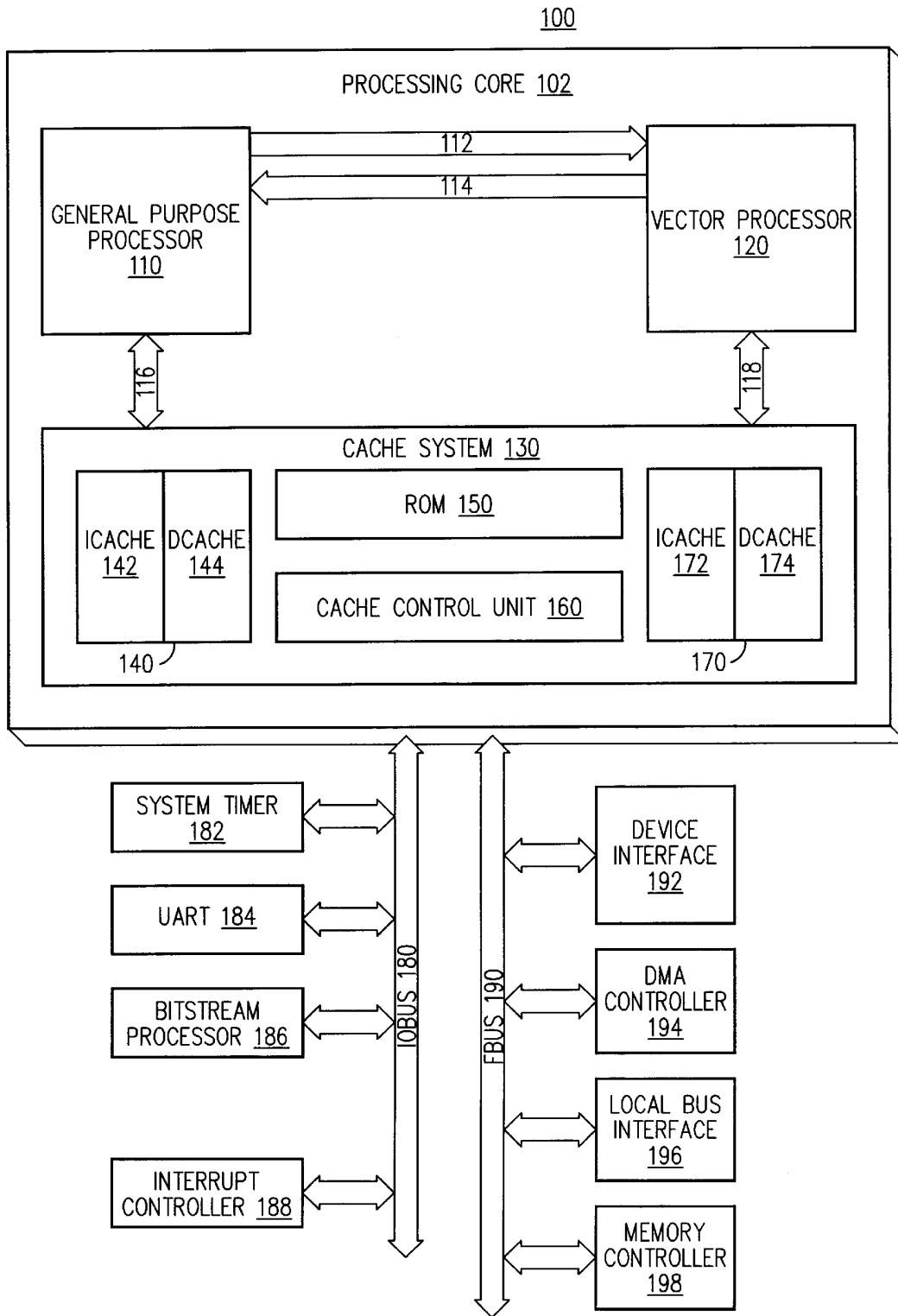


FIG. 1

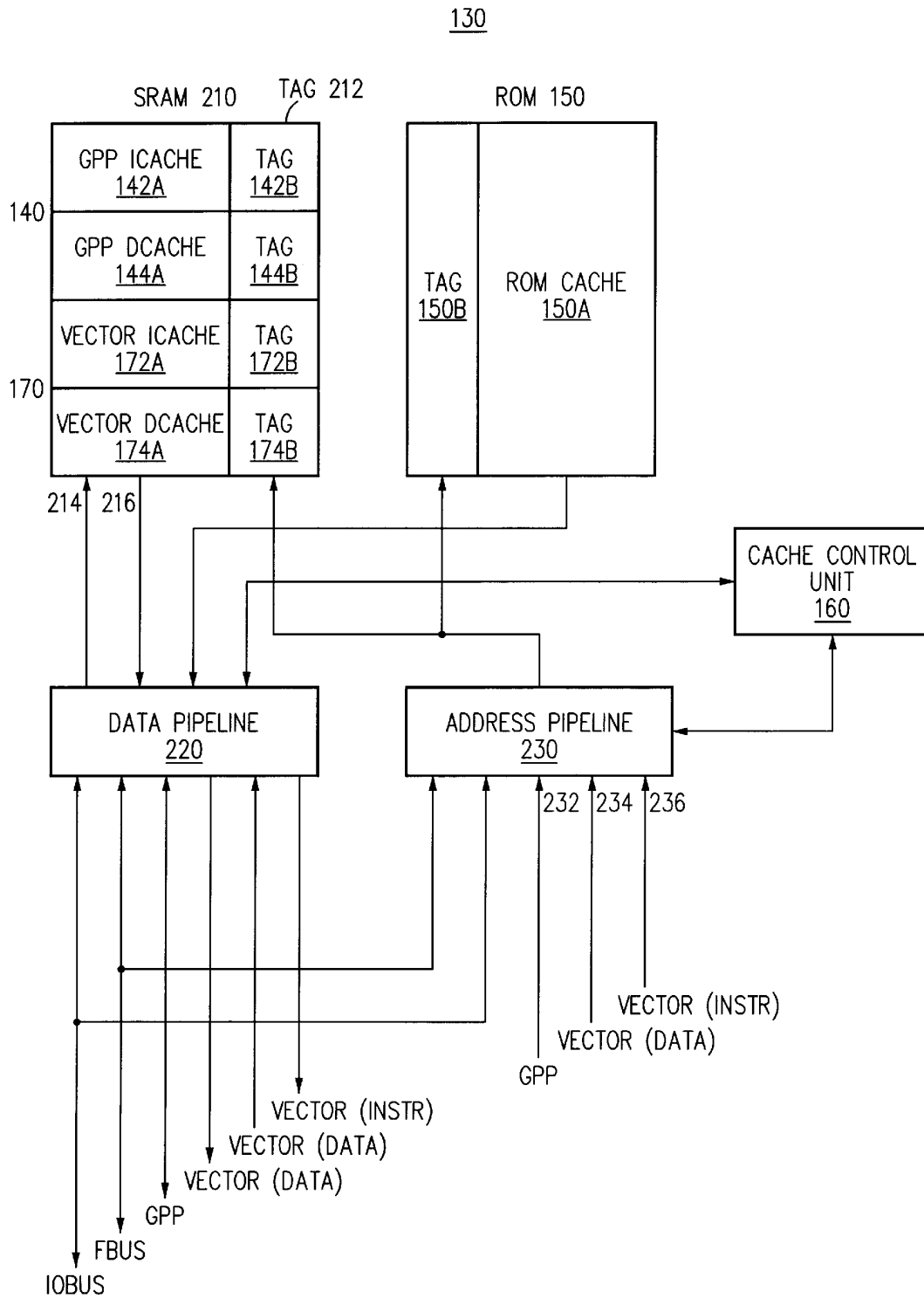


FIG. 2

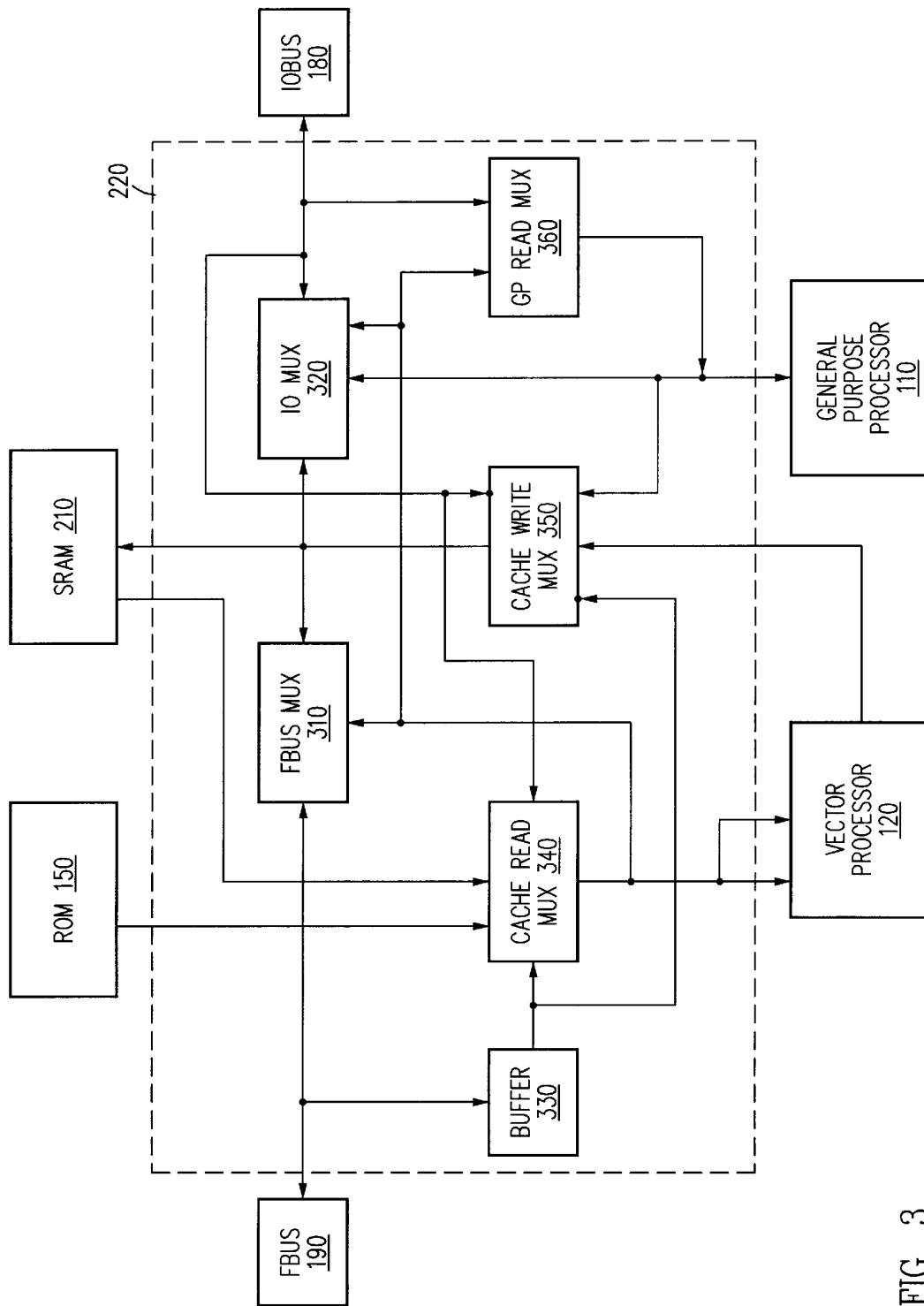


FIG. 3

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