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EXHIBIT I



Case 2:17-cv-00547-RAJ-RJK Document 1-9 Filed 10/18/17 Page 2 of 18 PageID# 200 Exhibit I - US 7,620,800 SRC Labs – Amazon F1 / Mipsology / Xilinx

A (P) method for data processing in a reconfigurable (A) computing system, the reconfigurable computing system colleast one (G) reconfigurable processor, the reconfigurable processor comprising a plurality of functional units, said mecomprising:

ZEBRA - FASTER NEURAL NETWORK INFERENCE FOR AWS F



Mipsology offers <u>FPGA-based</u> class-leading acceleration for Deep Learning, with no FPGA kn required. We leverage more than 20 years designing high-performance FPGA-based systems to offer our users the best solutions for Deep Learning.

Mipsology's first product, Zebra, offers users FPGA-based class leading acceleration for Neural inference. There is zero FPGA knowledge required nor a single line of code to write to use Zebra runs user defined neural network just as it would on GPU or CPU, switching takes minuted.

(P)

Claim 1



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A (P) method for data processing in a reconfigurable (A) computing system, the reconfigurable computing system colleast one (G) reconfigurable processor, the reconfigurable processor comprising a plurality of functional units, said more comprising:

Mipsology

Claim 1

Zebra Deep-Learning engine for Caffe (1 FPGA)

Sold by: Mipsology SAS

(P)

30 Day Free Trial Available - Zebra accelerates neural network inference using FPGA. User-defined neural network by Zebra just as they would be by a GPU or a CPU. Zebra is fully integrated with the traditional Deep Learning info Caffe, MXNet or TensorFlow. There is zero FPGA knowledge required nor a single line of code to write to use Zebra the Zebra library to switch from CPU or GPU to FPGA in minutes. Zebra includes the FPGA image and the software no FPGA compilation or FPGA tools to use. This AMI contains the following components: o Includes Zebra FPGA after Caffe. o This AMI supports your own CNN similar to AlexNet and GoogleNet powerly networks. a Supports 1 EP

with f1.2xlarge). o Pre-i and Caffe. o Includes pr network, VGG-16, VGGhttp://www.mipsology

 (\mathbf{A})

F1 FPGA Instance Types on AWS

- Up to 8 Xilinx UltraScale+ 16nm VU9P FPGA devices in a single inst
- The f1.16xlarge size provides:
 - 8 FPGAs, each with over 2 million customer-accessible FPGA programmable logic cells and over 5000 programmable DSP blo
 - Each of the 8 FPGAs has 4 DDR-4 interfaces, with each interface accessing a 16GiB, 72-bit wide, ECC-protected memory

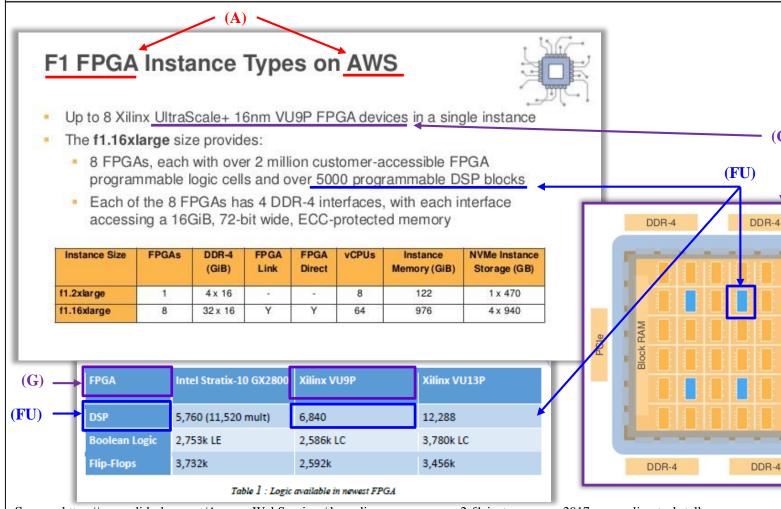
Instance Size	FPGAs	DDR-4 (GiB)	FPGA Link	FPGA Direct	vCPUs	Instance Memory (GiB)	NVMe In Storag
f1.2xlarge	1	4 x 16		-	8	122	1 x
f1.16xlarge	8	32 x 16	Y	Y	64	976	4 x

Source: https://aws.amazon.com/marketplace/pp/B073SHB43M



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A method for data processing in a **(A) reconfigurable computing system**, the reconfigurable computing system comprising one **(G) reconfigurable processor**, the reconfigurable processor comprising a plurality of **(FU) functional units**, said recomprising:



Source: https://www.slideshare.net/AmazonWebServices/deep-dive-on-amazon-ec2-f1-instance-may-2017-aws-online-tech-talks;



Claim 1

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Claim 1

(A)

A (P) method for data processing in a reconfigurable (A) computing system, the reconfigurable computing system co least one (G) reconfigurable processor, the reconfigurable processor comprising a (FU) plurality of functional units, comprising:

(P) In January 2017, our team demonstrated Zebra executed on a KU115 – showcasing the fastest 100 percent FPGA-based solution computing any neural network inference (as far as we've been able to determine).

We ported Zebra to AWS in just two months, and will soon offer access to our Zebra f1 implementation on AWS Marketplace. In Q2, we will support all convolutional neural networks (CNN) similar to AlexNet and GoogLeNet, delivering inference performance reaching 4000 images per second and more than 100 images per second per watt. We will also add support for Caffe and MXNET infrastructures, so our users will never have to worry about their FPGAs running "undercover."

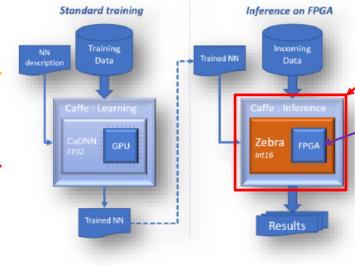
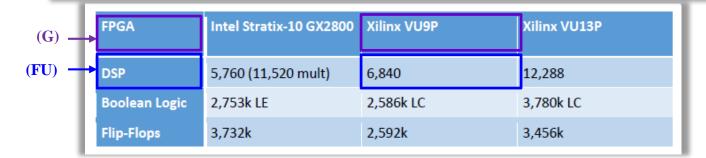


Figure 1: Mipsology Zebra general flow. The GPU is replaced by an FPGA when performing inference in the same infrastructure.





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