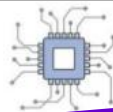

EXHIBIT G

Claim 1

A **(RP) reconfigurable processor** that instantiates an algorithm as hardware comprising:

F1 FPGA Instance Types on AWS



- Up to 8 Xilinx UltraScale+ 16nm VU9P FPGA devices in a single instance
- The **f1.16xlarge** size provides:
 - 8 FPGAs, each with over 2 million customer-accessible FPGA programmable logic cells and over 5000 programmable DSP blocks
 - Each of the 8 FPGAs has 4 DDR-4 interfaces, with each interface accessing a 16GiB, 72-bit wide, ECC-protected memory

Instance Size	FPGAs	DDR-4 (GiB)	FPGA Link	FPGA Direct	vCPUs	Instance Memory (GiB)	NVMe Instance Storage (GB)
f1.2xlarge	1	4 x 16	-	-	8	122	1 x 470
f1.16xlarge	8	32 x 16	Y	Y	64		

(RP)

Introduction

The Xilinx LogiCORE™ IP AXI Central Direct Memory Access (CDMA) core is a soft Xilinx Intellectual Property (IP) core for use with the Vivado® Design Suite. The AXI CDMA provides high-bandwidth Direct Memory Access (DMA) between a memory-mapped source address and a memory-mapped destination address using the AXI4 protocol. An optional Scatter Gather (SG) feature can be used to offload control and sequencing tasks from the system CPU. Initialization, status, and control registers are accessed through an AXI4-Lite slave interface, suitable for the Xilinx MicroBlaze™ processor.

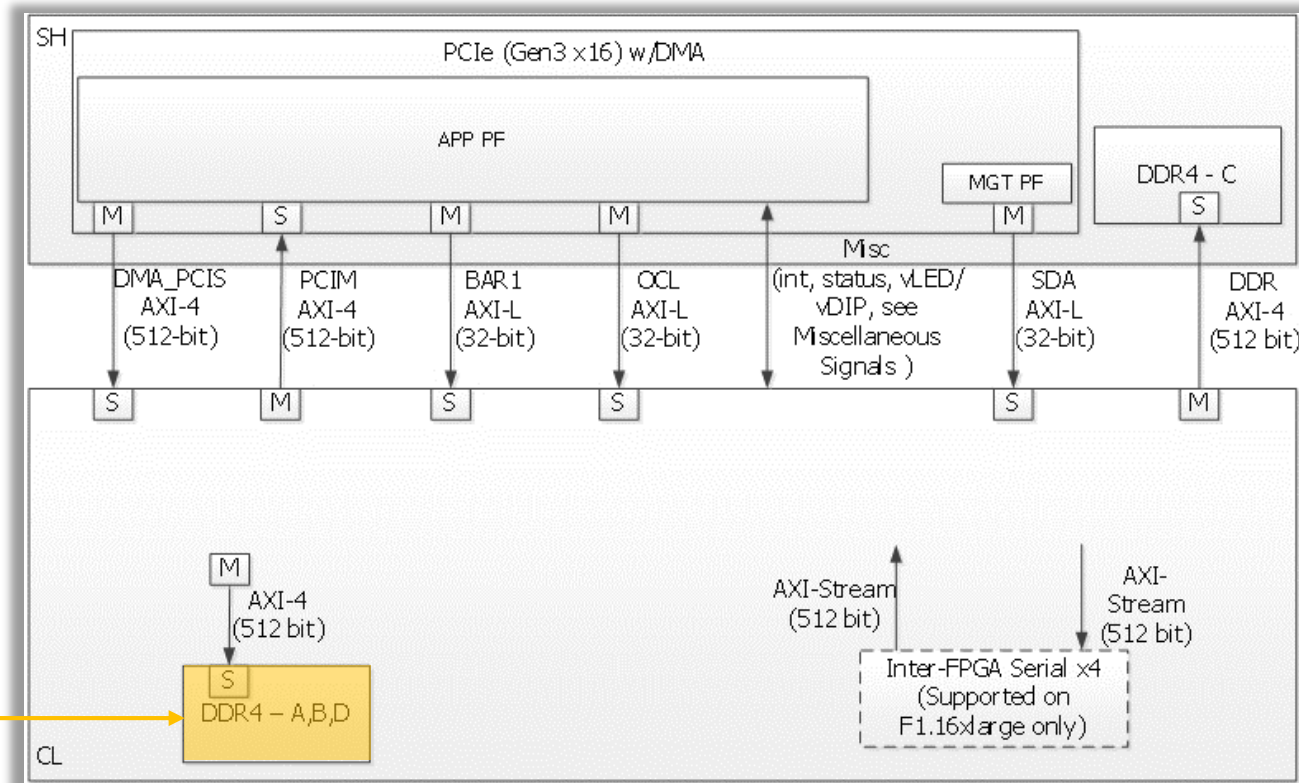
LogiCORE IP Facts Table

Core Specifics	
Supported Device Family ⁽¹⁾	Zynq®-7000 All
Supported User Interfaces	
Resources	See Table
Provided with Core	
Design Files	
Example Design	
Test Bench	
Constraints File	Xilinx Design delivered
Simulation Model	

Source: https://www.xilinx.com/support/documentation/ip_documentation/axi_cdma/v4_1/pg034-axi-cdma.pdf;

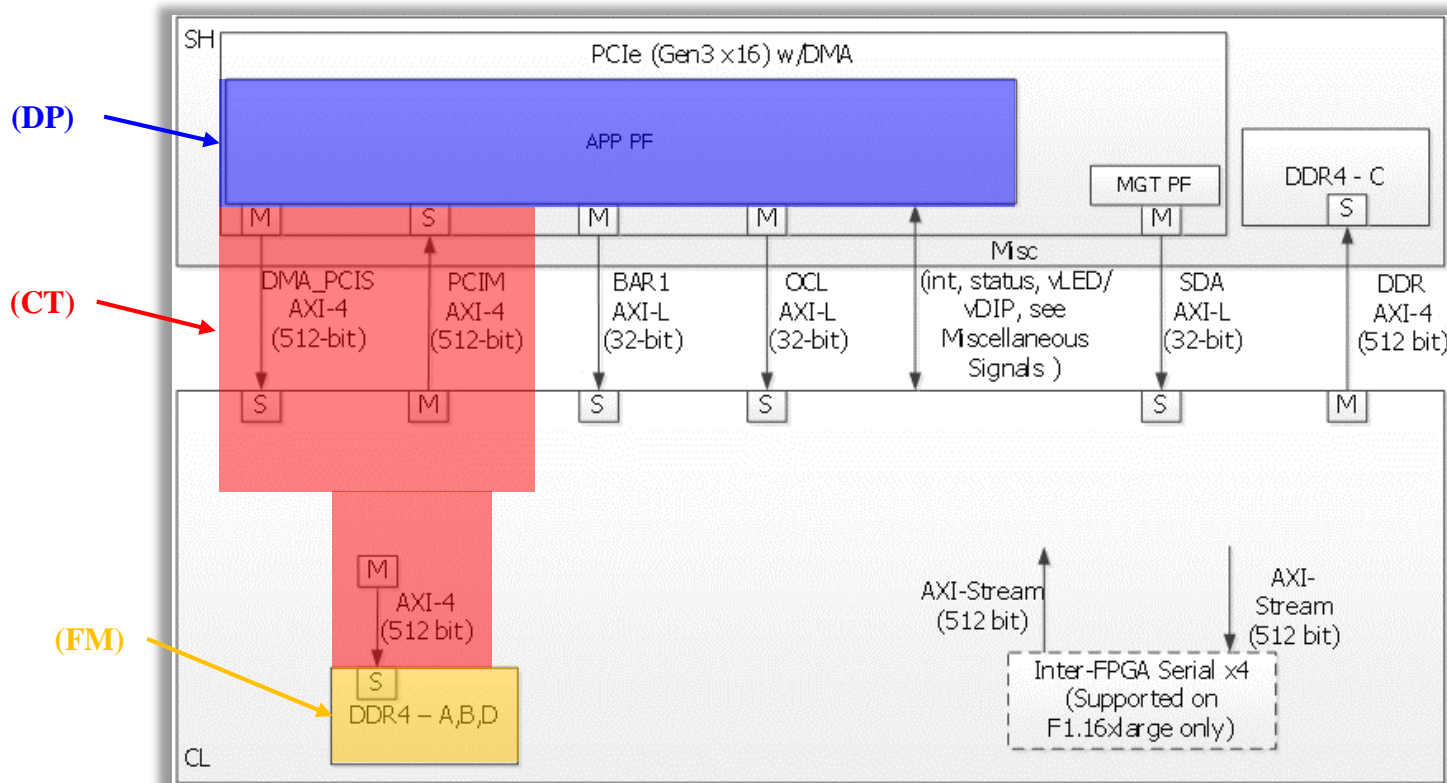
Claim 1

a (FM) first memory having a first characteristic memory bandwidth and/or memory utilization; and



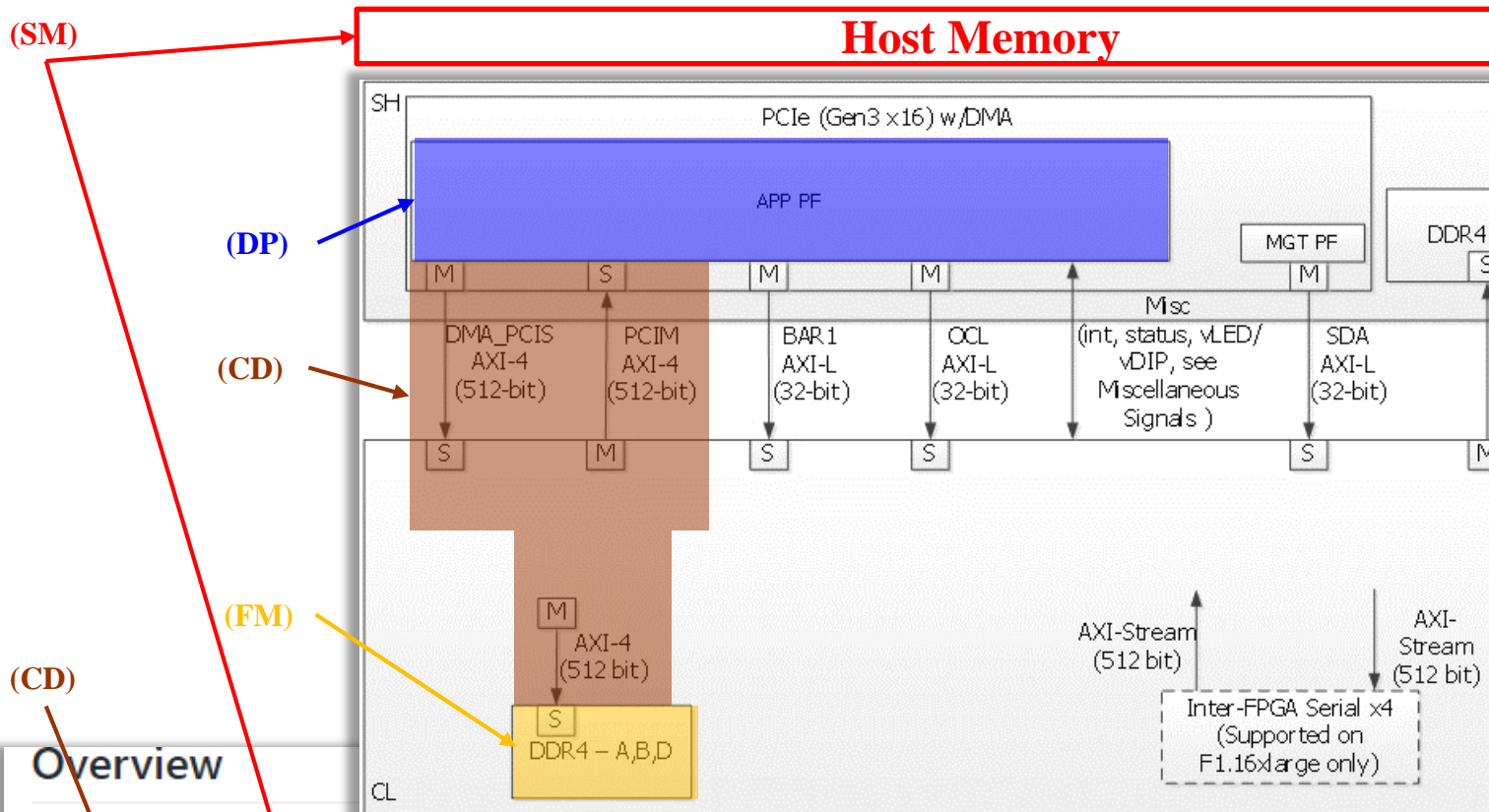
Claim 1

a (DP) data prefetch unit (CT) coupled to the (FM) memory,



Claim 1

wherein the **(DP) data prefetch unit (CD)** retrieves **only computational data required by the algorithm** from a **(SM) memory** of second characteristic memory bandwidth and/or memory utilization and places the retrieved computational **(FM) first memory**



Overview

The CL_DRAM_DMA example demonstrates the use and connectivity for many of the Shell/CL interfaces and functionality, including:

- 5. pcim_AXI4 traffic for host memory accesses from CL

Source: <https://www.slideshare.net/AmazonWebServices/deep-dive-on-amazon-ec2-f1-instance-may-2017-aws-online-tech-talks;>

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