EXHIBIT B

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(12) United States Patent

Poznanovic et al.

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(45) **Date of Patent: Dec. 12, 2006**

(54) SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE

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U.S.C. 154(b) by 0 days.

(21) Appl. No.: 10/869,200

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- (51) Int. Cl. G06F 12/00 (2006.01)
- (52) **U.S. Cl.** 711/170; 711/154
- (58) **Field of Classification Search** 711/170–173; 712/15 See application file for complete search history.

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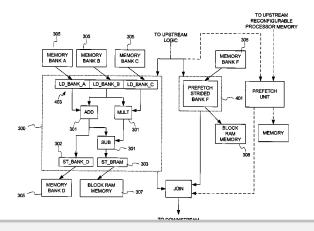
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(57) ABSTRACT

A reconfigurable processor that includes a computational unit and a data prefetch unit coupled to the computational unit, where the data prefetch unit retrieves data from a memory and supplies the data to the computational unit through memory and a data access unit, and where the data prefetch unit, memory, and data access unit is configured by a program. Also, a reconfigurable hardware system that includes a common memory; and one or more reconfigurable processors coupled to the common memory, where at least one of the reconfigurable processors includes a data prefetch unit to read and write data between the unit and the common memory, and where the data prefetch unit is configured by a program executed on the system. In addition, a method of transferring data that includes transferring data between a memory and a data prefetch unit in a reconfigurable processor; and transferring the data between a computational unit and the data prefetch unit.

19 Claims, 12 Drawing Sheets



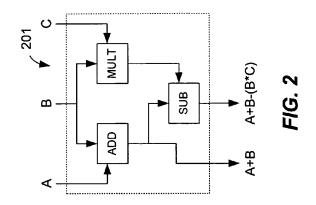


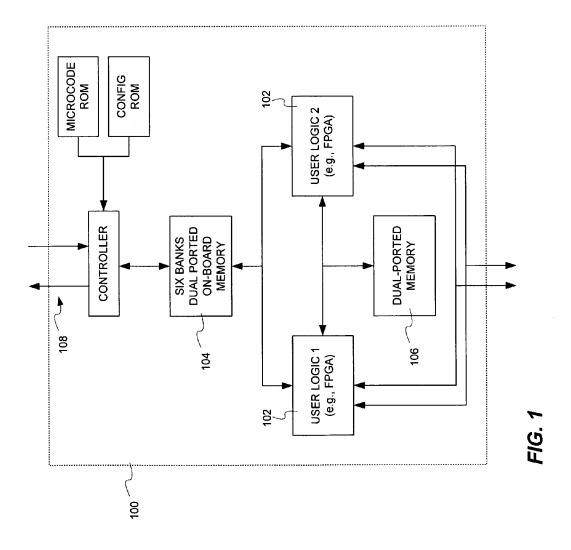
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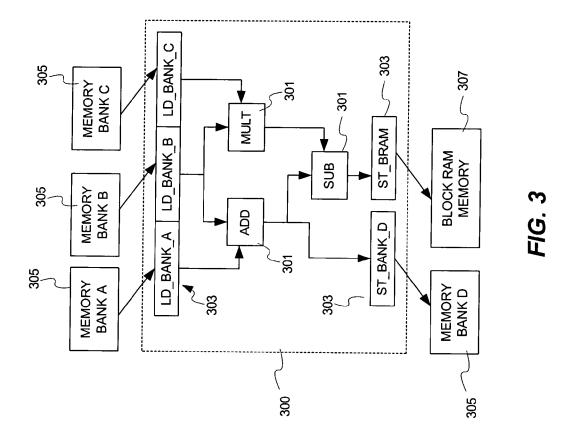


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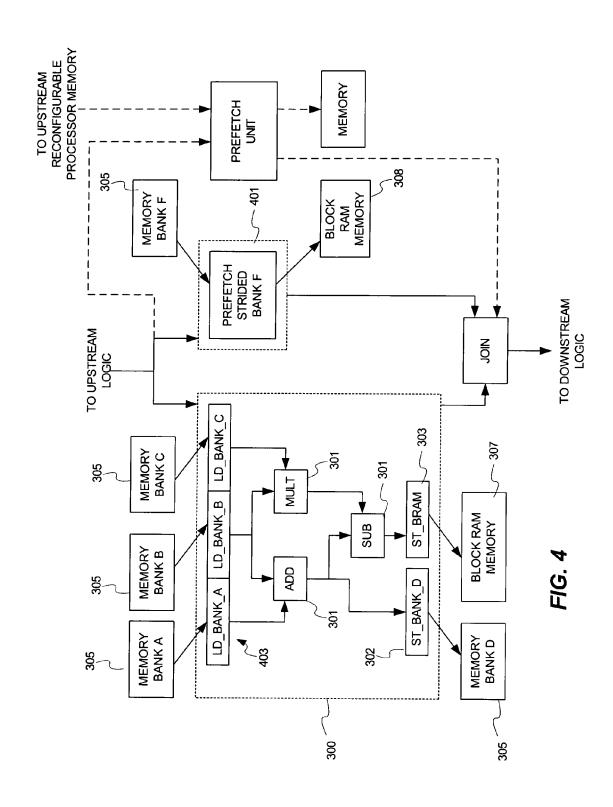


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