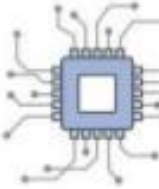

EXHIBIT J

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;

F1 FPGA Instance Types on AWS

← (CS)



- Up to 8 Xilinx UltraScale+ 16nm VU9P FPGA devices in a single instance
- The **f1.16xlarge** size provides:
 - 8 FPGAs, each with over 2 million customer-accessible FPGA programmable logic cells and over 5000 programmable DSP blocks
 - Each of the 8 FPGAs has 4 DDR-4 interfaces, with each interface accessing a 16GiB, 72-bit wide, ECC-protected memory

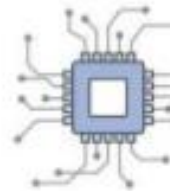
Instance Size	FPGAs	DDR-4 (GiB)	FPGA Link	FPGA Direct	vCPUs	Instance Memory (GiB)	NVMe Instance Storage (GB)
f1.2xlarge	1	4 x 16	-	-	8	122	1 x 470
f1.16xlarge	8	32 x 16	Y	Y	64	976	4 x 940

↑ (DM)

Claim 1

a (RL) reconfigurable logic device having a memory controller coupled to selected inputs and outputs of said DRAM

F1 FPGA Instance Types on AWS



(RL)



- Up to 8 Xilinx UltraScale+ 16nm VU9P FPGA devices in a single instance
- The **f1.16xlarge** size provides:
 - 8 FPGAs, each with over 2 million customer-accessible FPGA programmable logic cells and over 5000 programmable DSP blocks
 - Each of the 8 FPGAs has 4 DDR-4 interfaces, with each interface accessing a 16GiB, 72-bit wide, ECC-protected memory

Instance Size	FPGAs	DDR-4 (GiB)	FPGA Link	FPGA Direct	vCPUs	Instance Memory (GiB)	NVMe Instance Storage (GB)
f1.2xlarge	1	4 x 16	-	-	8	122	1 x 470
f1.16xlarge	8	32 x 16	Y	Y	64	976	4 x 940

Claim 1

a (RL) reconfigurable logic device having a (MC) memory controller coupled to selected inputs and outputs of said (RL) reconfigurable logic device; and

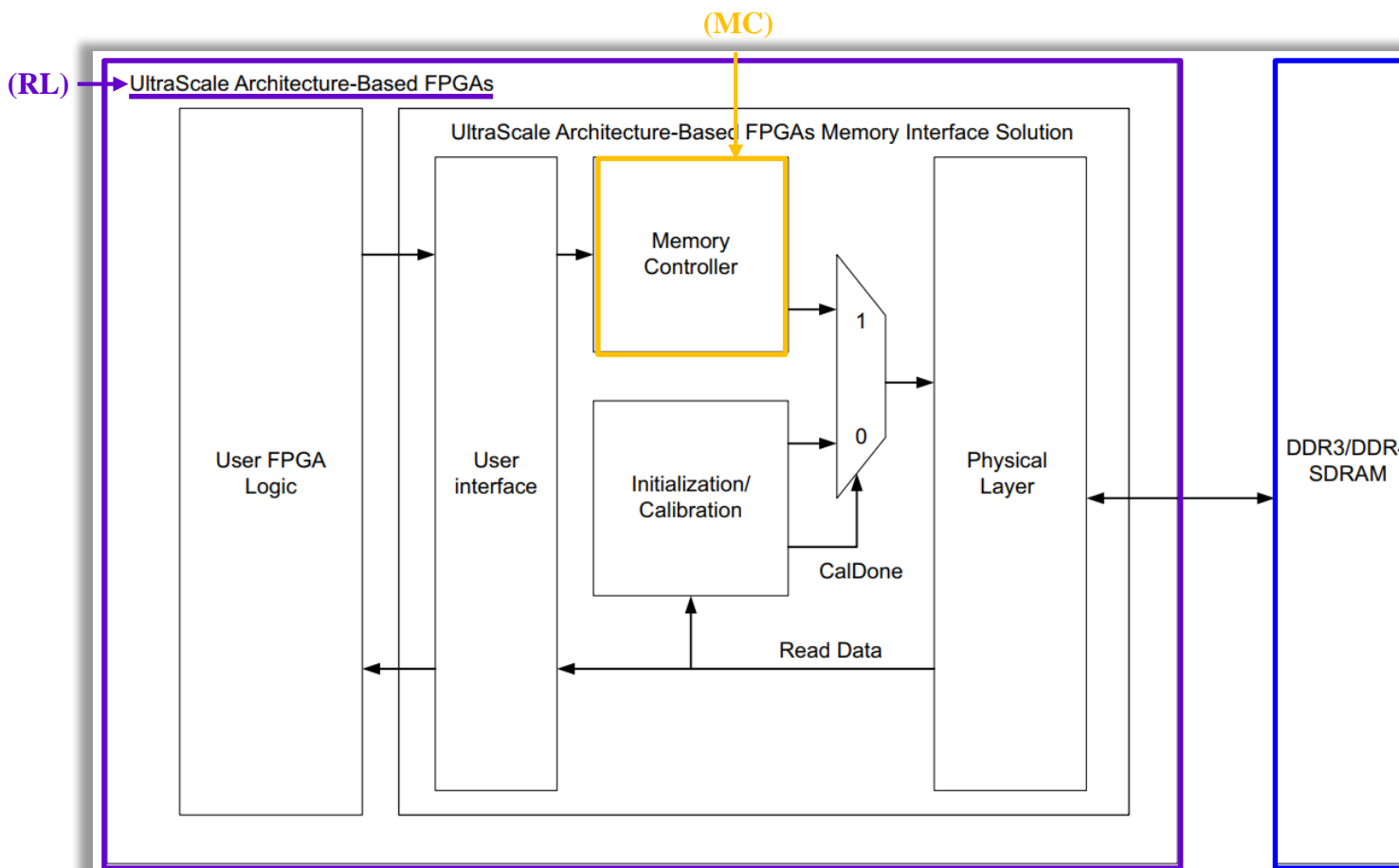


Figure 3-1: UltraScale Architecture-Based FPGAs Memory Interface Solution Core Architecture

Claim 1

a (DM) data maintenance block coupled to said (RL) reconfigurable logic device and (SR) self-refresh command in (D) DRAM memory,

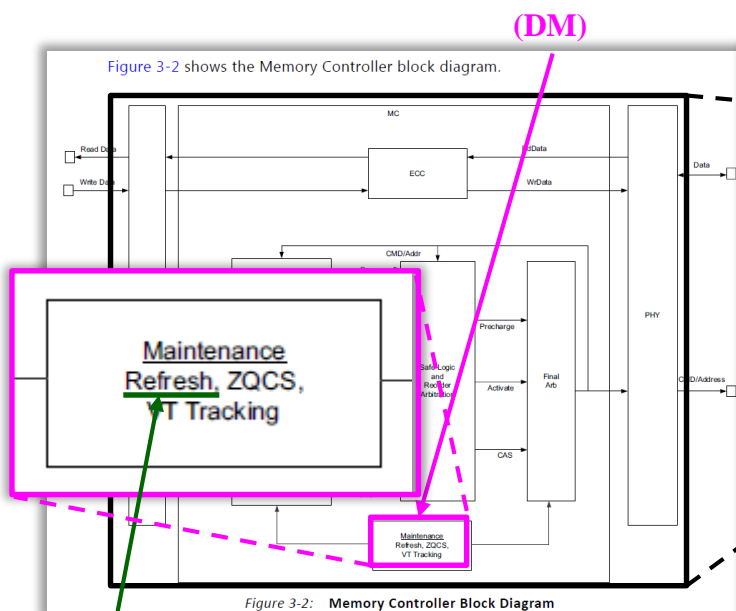


Figure 3-2: Memory Controller Block Diagram

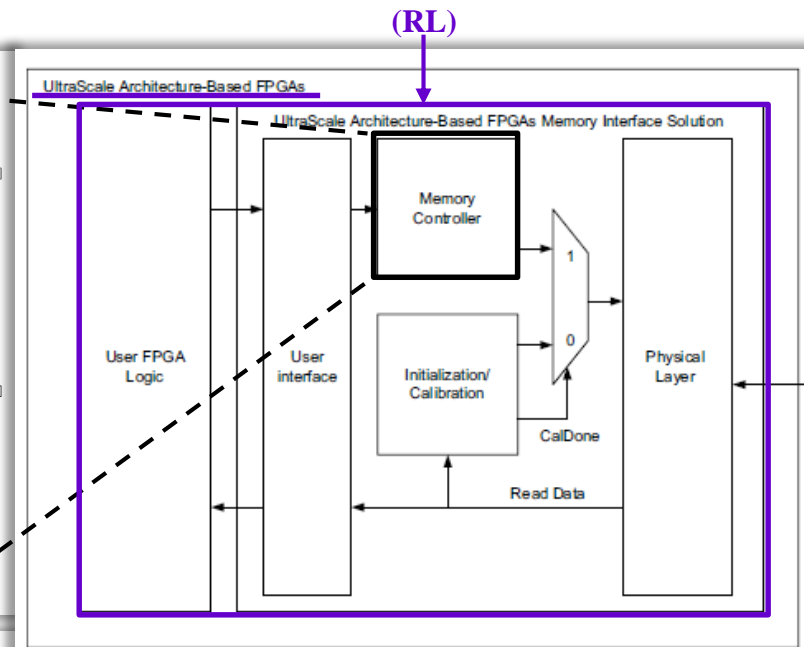


Figure 3-1: UltraScale Architecture-Based FPGAs Memory Interface Solution Core

Partial Reconfiguration

(SR) The Partial Reconfiguration option can be selected from the **Disable OBUF on reset# (DDR3) or reset_n (DDR4)** option in **Advance Memory Options** section in the **Advanced Options** tab (see Figure 5-5 and Figure 5-6) when **Self Refresh** or **Save-Restore** option is enabled. When Partial Reconfiguration is enabled, the `ddr3_reset#/ddr4_reset_n` port is not included in the pin planning list and is a part of the user interface. It is your responsibility to use this port in driving the actual memory interface pin outside the DDR3/DDR4 IP design. The DDR3/DDR4 IP design is a part of the reconfigurable block, while the driver of the `ddr3_reset#/ddr4_reset_n` pin stays in the static location.

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