Exhibit F

EXHIBIT F
U.S. Patent No. 8,933,945

Claim 1	Exemplary Accused Product: NXP i.MX 8QuadMax Applications Processor
A graphics processing circuit, comprising:	To the extent that the preamble is limiting, the NXP processors meet this limitation. The NXP processors perform graphics processing. To illustrate: Graphics processing is handled by two (2x) Graphics Processing Units (GP some of the latest graphic APIs including OpenVX for computer vision. Vi managed by a dedicated video engine with decoding formats including HE to 4K60, H.264 up to 4K30 and encoding in H.264 up to 1080p30. The chi various display interfaces that supports up to four displays. In order to feed high demanding blocks, i.MX8QM has two (2) DRAM controllers supporti LPDDR4 memory types. i.MX 8QuadMax Applications Processor Reference Manual, § 1.1.1, Document No.: I 9/2021 (downloaded from nxp.com). The NXP processors include one or more Graphics Processing Unit (GPU) subsystem more GPUs. To illustrate: 16.1.1 Overview This section provides a high-level overview of the Graphics Processing U subsystem and the Video Processing Unit (VPU) subsystem on the chip. 16.1.1.1 GPU This chip embeds two identical GPU sub-systems. *Id.*, § 16.1.1. To illustrate further:

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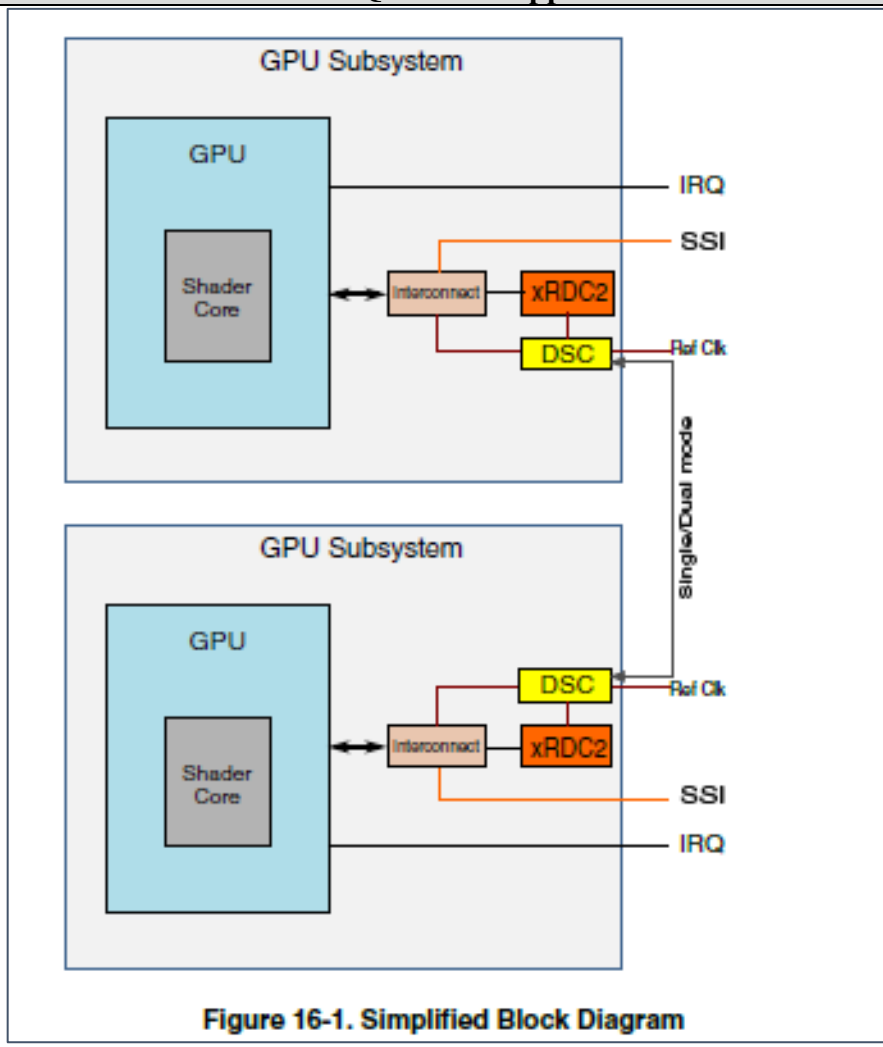

Figure 16-1. Simplified Block Diagram

Id.

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at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations,	On information and belief, the NXP processors meet this limitation. For instance, the NXP processors perform "massively parallel data processing" across engines," and "each compute unit has its own arithmetic logic units (ALUs) . . . that ca computations." OpenCL uses parallel execution SIMD (single instruction, multiple data) engines found in GPU computational density by performing massively parallel data processing on multiple data iter compute engines. Each compute unit has its own arithmetic logic units (ALUs), including pipe (FP), integer (INT) units and a special function unit (SFU) that can perform computations as w operations. The parallel computations and associated series of operations are called a kernel, can execute a kernel on thousands of work-items in parallel at any given time. i.MX Graphic User's Guide, § 5.1.1, Document No. IMXGRAPHICUG, Rev. 0, 05/20 https://www.nxp.com/docs/en/user-guide/i.MX_AA_Graphics_User's_Guide.pdf. To illustrate further, NXP's user guides show the Vivante OpenCL data pipeline used NXP's public demonstrations of its processors depicts the use of multiple graphics pip

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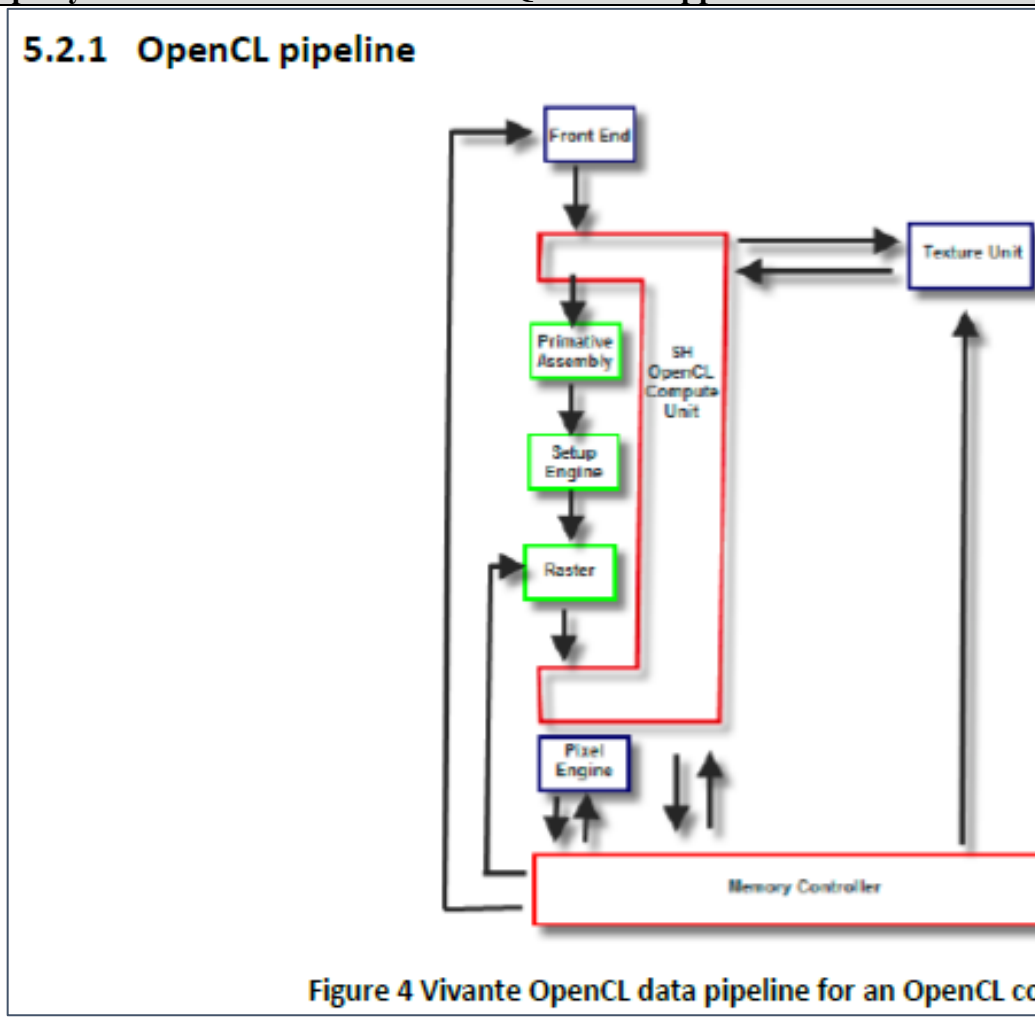

Id., § 5.2.1. To illustrate further, the NXP processors exhibit "massive data parallelism rasterization":

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