Exhibit E

EXHIBIT E
U.S. Patent No. 7,804,435

Claim 1	Exemplary Accused Product: NXP i.MX 8QuadMax Applications Processor
An apparatus comprising:	To the extent that the preamble is limiting, the NXP processors meet this limitation. The NXP processors include a Video Processing Unit: This chapter introduces the i.MX 8QuadMax (i.MX8QM). The i.MX8Q comprehensive multimedia device targeting high-end automotive and in segments. The chip is built using a leading edge process to achieve both performances and low-power consumption. The chip relies on a powerfu core complex based on a dual (2x) Cortex-A72 cluster for use-cases requ computing performances and a quad (4x) Cortex-A53 cluster running m cases at a lower-power consumption. i.MX 8QuadMax Applications Processor Reference Manual, § 1.1.1, Document No.: IM 9/2021 (downloaded from nxp.com). To illustrate further: • 1x VPU • 4x M0+ processors with 16KB Cache (1x for decode, 2x for transport stream) • Supports H.265 decode (4Kp60) • Supports H.264 decode (4Kp30) • H.264 encoder (1080p30) *Id.*, § 1.1.2.

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Claim 1	Exemplary Accused Product: NXP i.MX 8QuadMax Applications Processor
a power management controller	The NXP processors include a System Control Unit (SCU) that handles power manage

> **1.2.1.1 SCU**
>
> The System Controller Unit (SCU) is made of a Cortex-M4 processo 266MHz with 256KB of TCM and a set of peripherals and interfaces external PMIC and to control internal subsystems. The SCU Cortex- processor to boot the chip (see System Boot). The SCU is responsibl
>
> - Booting the system
> - Interfacing with the external PMIC through a dedicated I2C and
> - Managing power, clocking, and reset of internal subsystems
> - Controlling pin multiplexing and IO control (drive strength and
> - Managing resource partitioning through isolation (see xRDC cha
> - Managing thermal

i.MX 8QuadMax Applications Processor Reference Manual, § 1.2.1.1, Document No.: 0, 9/2021 (downloaded from nxp.com).

> **8.18.4 System Clocks**
>
> All system resources are controlled only through SCU Firmware using the functions. These functions can be found in the SCU Firmware Guide. The table and the clock tree provides information about the module clocks, the associated with them, and its clock roots.

Id., § 8.18.4. To illustrate further:

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Claim 1	Exemplary Accused Product: NXP i.MX 8QuadMax Applications Processor

13.1.7.1 Power Management Service

All aspects of power management including power control, bias control, reset control, and wake-up event monitoring are grouped within the SC P Management service.

- **Power Control** - The SC firmware is responsible for centralized mar power controls and external power management devices. It manages and voltage of power domains as well as bias control. It also resets p required due to power state transitions. This is all done via the API b communicating power state needs for individual resources.
- **Clock Control** - The SC firmware is responsible for centralized man clock controls. This includes clock sources such as oscillators and PL clock dividers, muxes, and gates. This is all done via the API by com clocking needs for individual resources.
- **Reset Control** - The SC firmware is responsible for reset control. Th booting/rebooting a partition, obtaining reset reasons, and starting/sto

Id., § 13.1.7.1.

The SC firmware runs on the SCU immediately after the SCU Read-only-memory (ROM) finish images from the first container. It is responsible for initializing many aspects of the system. Th power and clock configuration and resource isolation hardware configuration. By default, the SC the primary boot core to own most of the resources and launches the boot core. Additional confi by boot code.

System Controller Firmware API Reference Guide, § 1.1, i.MX8 QXP Die (Version 1.5 *available at* https://community.nxp.com/pwmxy87654/attachments/pwmxy87654/imx-processors/150415/1/sc_fw_api_qx_b0.pdf.

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Claim 1	Exemplary Accused Product: NXP i.MX 8QuadMax Applications Processor
	To illustrate further: **1.3.1 Power Management Service** All aspects of power management including power control, bias control, clock control, reset contr monitoring are grouped within the SC Power Management service. • **Power Control** - The SC firmware is responsible for centralized management of power power management devices. It manages the power state and voltage of power domains as also resets peripherals as required due to power state transitions. This is all done via the A power state needs for individual resources. • **Clock Control** - The SC firmware is responsible for centralized management of clock contro sources such as oscillators and PLLs as well as clock dividers, muxes, and gates. This is a communicating clocking needs for individual resources. • **Reset Control** - The SC firmware is responsible for reset control. This includes booting obtaining reset reasons, and starting/stopping of CPUs. Before any hardware in the SoC can be used, SW must first power up the resource and enable any otherwise access will generate a bus error. The Power Management (PM) API is documented he *Id.*, § 1.3.1.

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