

Exhibit B



(12) **United States Patent**
Leather et al.

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(45) **Date of Patent:** **Jan. 13, 2015**

(54) **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

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(65) **Prior Publication Data**

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(51) **Int. Cl.**

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G06F 13/14 (2006.01)
G06F 12/02 (2006.01)
G06T 11/40 (2006.01)
G06T 15/00 (2011.01)
G09G 5/36 (2006.01)

(52) **U.S. Cl.**

CPC . **G06T 11/40** (2013.01); **G06T 1/20** (2013.01);
G06T 15/005 (2013.01); **G09G 5/363** (2013.01)
USPC **345/506**; **345/519**; **345/544**

(58) **Field of Classification Search**

USPC **345/506**, **530**, **505**, **588**, **544**, **545**, **532**,
345/501, **502**, **531**, **519**
See application file for complete search history.

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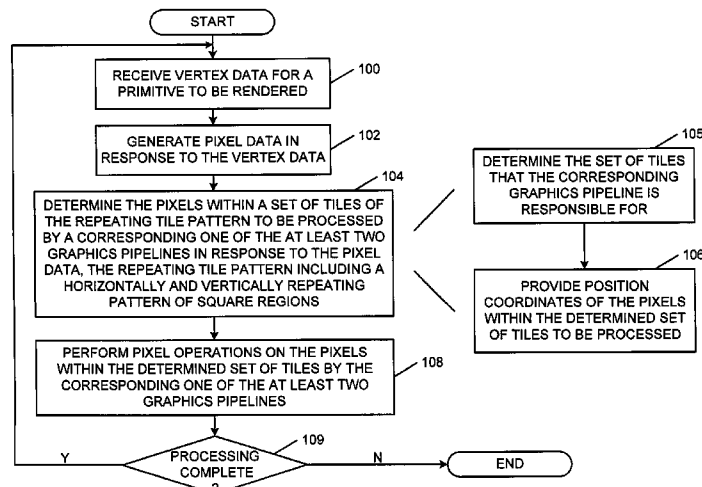
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(57) **ABSTRACT**

A graphics processing circuit includes at least two pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern, a respective one of the at least two pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions. A graphics processing method includes receiving vertex data for a primitive to be rendered; generating pixel data in response to the vertex data; determining the pixels within a set of tiles of a repeating tile pattern to be processed by a corresponding one of at least two graphics pipelines in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions; and performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines.

21 Claims, 5 Drawing Sheets



US 8,933,945 B2

Page 2

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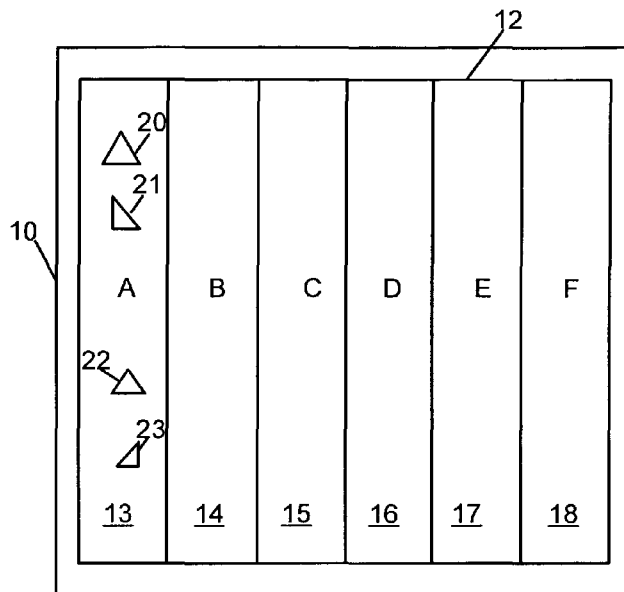


FIG. 1
PRIOR ART

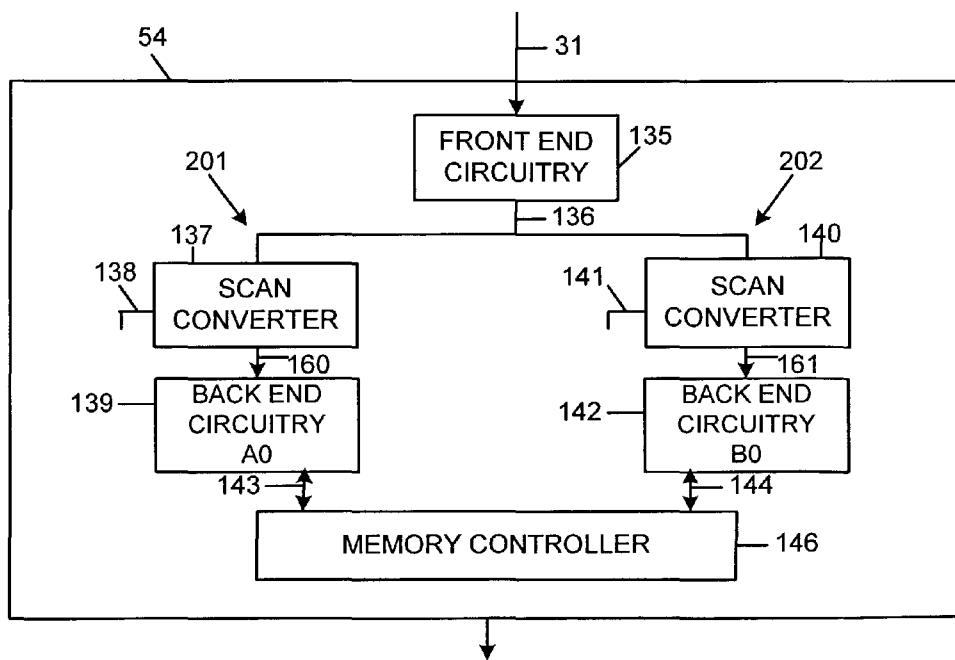


FIG. 5

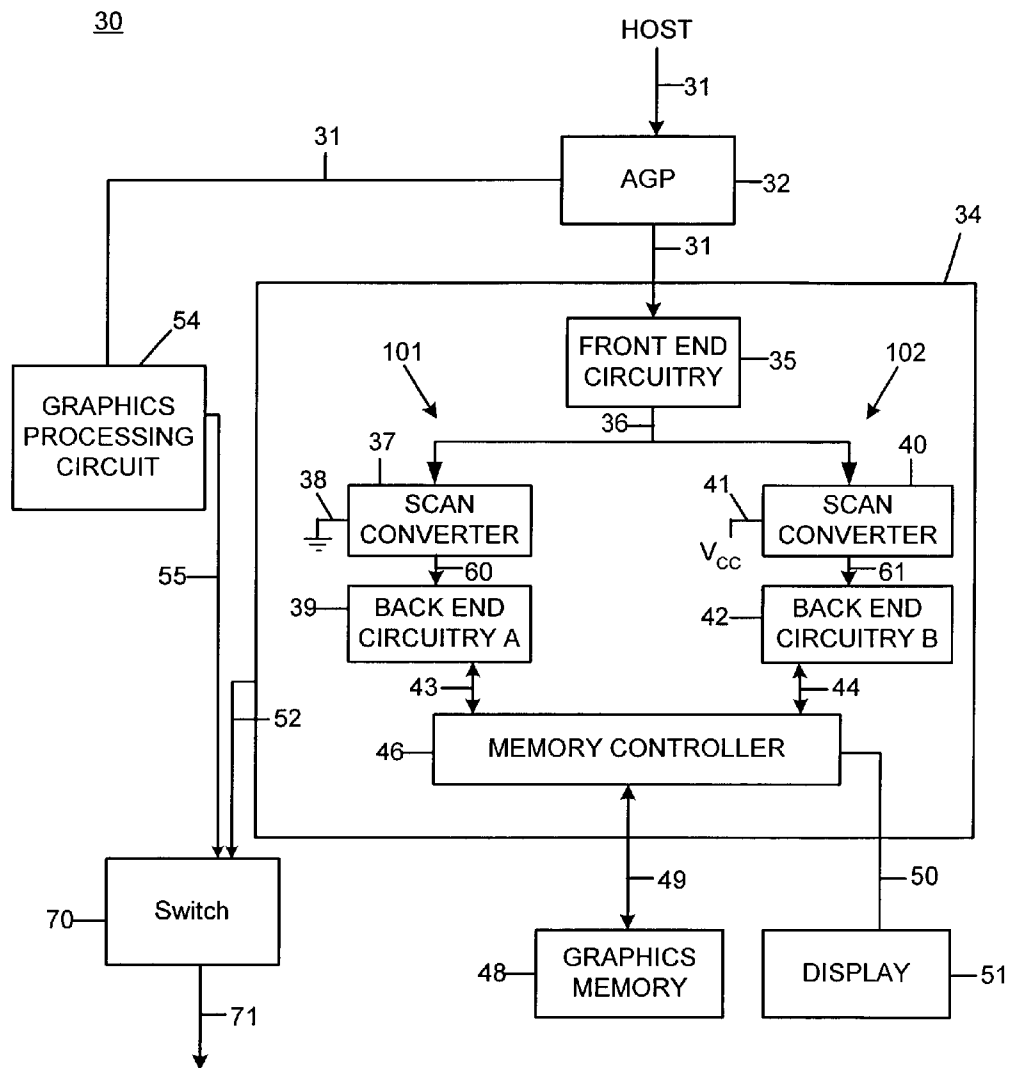


FIG. 2

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