UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

Advanced Silicon Technologies LLC, Plaintiff, v. NXP Semiconductors N.V., NXP B.V., and NXP USA, Inc., Defendants.	Case No. 6:22-cv-00466-ADA-DTG **Jury Trial Demanded**

AST's Sur-Reply Claim Construction Brief

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1. Introduction

NXP's Reply (ECF No. 56) reads as if NXP need only identify a single embodiment or a theoretical interpretation of the claim language to support its narrowing constructions. The Court, of course, requires more, which NXP does not supply. Evidence to justify NXP's extremist proposals simply does not exist, and it certainly does not exist in the record. For this reason, NXP's Reply focuses instead on "gotcha" attempts that misinterpret or simply miss AST's reasons why each disputed term has and should be afforded its plain meaning.

2. NXP's Reply Cites No Disavowals of Claim Scope or Compelling Evidence to Define the Disputed Terms Other than According to Their Plain and Ordinary Meaning

2.1. "A method for reducing power consumption for a video decoder comprising" ('435 Patent, Claim 26)

Term	Claim(s)	AST's Proposal	NXP's Proposal
"A method for reducing power consumption for a video decoder comprising"	'435 Patent, Claim 26	Non-limiting	Limiting

NXP's Reply misinterprets yet mocks AST's brief (ECF No. 50) as "paradoxical" while offering no reason for the Court to depart from the "general rule" that "preamble language is not treated as limiting." *E.g.*, *Cochlear Bone Anchored Sols. AB v. Oticon Med.*, 958 F.3d 1348, 1354 (Fed. Cir. 2020) (internal cites omitted). NXP questions how AST could say the preamble describes the benefit of the claim—"reducing power consumption for a video decoder"—while arguing against NXP's narrowing construction that reads out any functionality that at any time increases power consumption for a video decoder. AST gave the answer: the claim improves the "reactive" prior art techniques for conserving power with a "proactive" method that dynamically adjusts power consumption based on the detected input stream. '435 Patent at 1:45-48, 2:43-45.

This "proactive" approach "reduc[es] power consumption" ***overall*** by adjusting power levels dynamically instead of only in response to significant discharge. Claim 26's method steps

confirm this understanding. They describe "***varying*** power consumption of at least one operational portion of a video decoder" in response to "determining input stream encoding description data." They also describe exactly what NXP's construction would read out: "if more than one input stream is received . . . ***increasing*** the power consumption of at least one operational portion of a video decoder." Claim 26 teaches this method to "select one of a plurality of different power consumption states for a video decoder" to reduce overall power consumption, including "varying" and "increasing" power as needed. NXP's argument that the plain meaning conflicts with the preamble assumes what it sets out to prove—that the preamble means "reducing" power every time the method is performed, not "reducing" overall power consumption by performing the method instead of prior art techniques. The claim language confirms NXP's presumption is wrong.

The preamble to Claim 26 of the '435 Patent is not limiting because it does not "recite[] essential structure or steps" and is not "necessary to give life, meaning, and vitality" to the claim. *E.g.*, *Catalina Mktg. Int'l v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002).

2.2. "graphics pipeline" ('945 Patent, Claims 1, 4, 12, 21)

Term	Claims	AST's Proposal	NXP's Proposal
"graphics pipeline"	'945 Patent, Claims 1, 4, 12, 21	Plain and ordinary meaning	"hardware, which may be one or more circuits~~, that processes graphics data~~"[1]

NXP presents no evidence that a POSITA would understand "graphics pipeline" to include only hardware. NXP instead interprets exemplary embodiments in the specification to include hardware components. *See* ECF No. 49 at 6. NXP's briefs cite no disavowal of claim scope or limiting language that would restrict the plain meaning of "graphics pipeline" to purely hardware

[1] NXP withdrew its "that processes graphics data" limitation, now asking the Court to construe "graphics pipeline" as "hardware, which may be one or more circuits." ECF No. 56 at 4 n.4.

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