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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Leather et al. Examiner:

Serial No.: Art Group:

Filing Date: June 12, 2003 Docket No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop Patent Application
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06/12/03 Winona K. Jackson
Date *Winona K. Jackson*

PRELIMINARY AMENDMENT

Dear Sir:

Prior to examination, Applicants respectfully request that the above-identified application be amended as follows:

In The Specification:

Please add the following new paragraph directly below the invention title on page 1 of the specification as follows:

This application claims the benefit of U. S. Provisional Application Ser. No. 60/429,641 filed November 27, 2002, entitled "Dividing Work Among Multiple Graphics Pipelines Using a Super-Tiling Technique", having as inventors Mark M. Leather and Eric Demers, and owned by instant assignee.

CHICAGO/#1083968.1

REMARKS

Applicants submit that the specification is fully supported by the original provisional application, and the claims are fully supported by the originally filed provisional application.

Respectfully submitted,

By: _____
Christopher J. Reckamp
Reg. No. 34,414

Dated: June 12, 2003

Vedder, Price, Kaufman & Kammholz
222 North LaSalle Street
Chicago, Illinois 60601
Telephone: (312) 609-7500
Facsimile: (312) 609-5005

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PATENT APPLICATION
ATTY. DOCKET NO. 00100.02.0053

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

FILING OF A UNITED STATES PATENT APPLICATION

DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE

INVENTORS:

Mark M. Leather 12187 Woodside Drive Saratoga, California 95070	Eric Demers 901 Sycamore Drive Palo Alto, California 94303

ATTORNEY OF RECORD:
CHRISTOPHER J. RECKAMP
REGISTRATION NO. 34,414
VEDDER PRICE KAUFMAN & KAMMHOLZ
222 NORTH LASALLE STREET, SUITE 2600
CHICAGO, ILLINOIS 60601
PHONE (312) 609-7500
FAX (312) 609-5005

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Name of Depositor: Winona K. Jackson

Signature: Winona K. Jackson

DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE

RELATED CO-PENDING APPLICATION

[0001] This is a related application to a co-pending application entitled "Parallel Pipeline Graphics System" having docket number 010025, having serial number _____, having Leather et al. as the inventors, filed on even date, owned by the same assignee and hereby incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0001] The present invention generally relates to graphics processing circuitry and, more particularly, to dividing graphics processing operations among multiple pipelines.

BACKGROUND OF THE INVENTION

[0002] Computer graphics systems, set top box systems or other graphics processing systems typically include a host processor, graphics (including video) processing circuitry, memory (e.g. frame buffer), and one or more display devices. The host processor may have a graphics application running thereon, which provides vertex data for a primitive (e.g. triangle) to be rendered on the one or more display devices to the graphics processing circuitry. The display device, for example, a CRT display includes a plurality of scan lines comprised of a series of pixels. When appearance attributes (e.g. color, brightness, texture) are applied to the pixels, an object or scene is presented on the display device. The graphics processing circuitry receives the vertex data and generates pixel data including the appearance attributes which may be presented on the display device according to a particular protocol. The pixel data is typically stored in the frame buffer in a manner that corresponds to the pixels location on the display device.

[0003] FIG. 1 illustrates a conventional display device 10, having a screen 12 partitioned into a series of vertical strips 13-18. The strips 13-18 are typically 1-4 pixels in width. In like manner, the frame buffer of conventional graphics processing systems is partitioned into a series of vertical strips having the same screen space width.

Alternatively, the frame buffer and the display device may be partitioned into a series of horizontal strips. Graphics calculations, for example, lighting, color, texture and user viewing information are performed by the graphics processing circuitry on each of the primitives provided by the host. Once all calculations have been performed on the primitives, the pixel data representing the object to be displayed is written into the frame buffer. Once the graphics calculations have been repeated for all primitives associated with a specific frame, the data stored in the frame buffer is rendered to create a video signal that is provided to the display device.

[0004] The amount of time taken for an entire frame of information to be calculated and provided to the frame buffer becomes a bottleneck in graphics systems as the calculations associated with the graphics become more complicated. Contributing to the increased complexity of the graphics calculation is the increased need for higher resolution video, as well as the need for more complicated video, such as 3-D video. The video image observed by the human eye becomes distorted or choppy when the amount of time taken to render an entire frame of video exceeds the amount of time in which the display device must be refreshed with a new graphic or frame in order to avoid perception by the human eye. To decrease processing time, graphics processing systems typically divide primitive processing among several graphics processing circuits where, for example, one graphics processing circuit is responsible for one vertical strip (e.g. 13) of the frame while another graphics processing circuit is responsible for another vertical strip (e.g. 14) of the frame. In this manner, the pixel data is provided to the frame buffer within the required refresh time.

[0005] Load balancing is a significant drawback associated with the partitioning systems as described above. Load balancing problems occur, for example, when all of the primitives 20-23 of a particular object or scene are located in one strip (e.g. strip 13) as illustrated in FIG. 1. When this occurs, only the graphics processing circuit responsible strip 13 is actively processing primitives; the remaining graphics processing circuits are idle. This results in a significant waste of computing resources as at most only half of the graphics processing circuits are operating. Consequently, graphics processing system performance is decreased as the system is only operating at a maximum of fifty percent capacity.

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