

(12) **United States Patent**
Wang et al.

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(54) **MULTIPLE PIPELINE MEMORY
 CONTROLLER FOR SERVICING REAL
 TIME DATA**

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(*) Notice: Under 35 U.S.C. 154(b), the term of this
 patent shall be extended for 0 days.

(21) Appl. No.: **08/885,335**

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(51) Int. Cl.⁷ **G06F 13/16**

(52) U.S. Cl. **345/521; 345/506; 711/151;**
711/158

(58) Field of Search **345/521, 506,**
345/512, 302; 711/147, 151, 158, 169;
395/729, 731, 732; 710/241, 243, 244

(56) **References Cited**

U.S. PATENT DOCUMENTS

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* cited by examiner

Primary Examiner—Raymond J. Bayerl

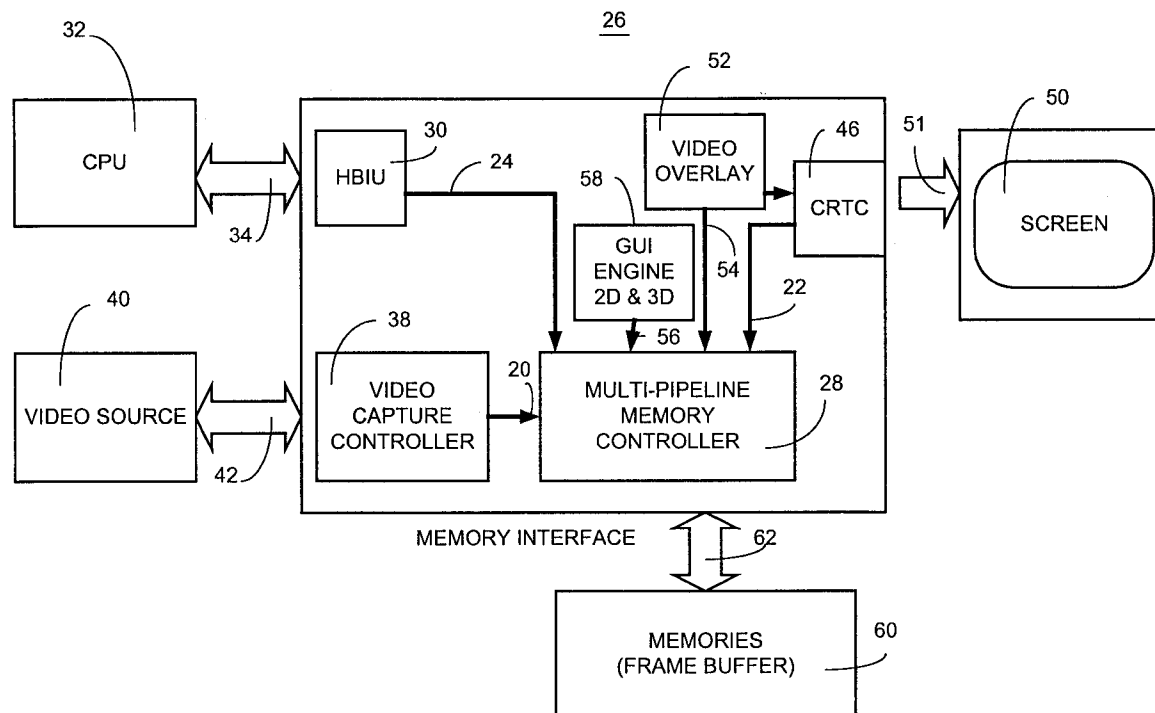
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(57) **ABSTRACT**

A multiple pipeline memory controller has a plurality of two stage pipeline processors dedicated to separately process real time video capture and display refresh input request signals. A separate pipeline processor processes non-real time input signals. The multiple pipeline design reduces memory access latency and improves throughput of data in display FIFO memory to effect improved resolution. The multiple pipeline memory controller can be integrated in a video graphics controller (VGC).

21 Claims, 4 Drawing Sheets



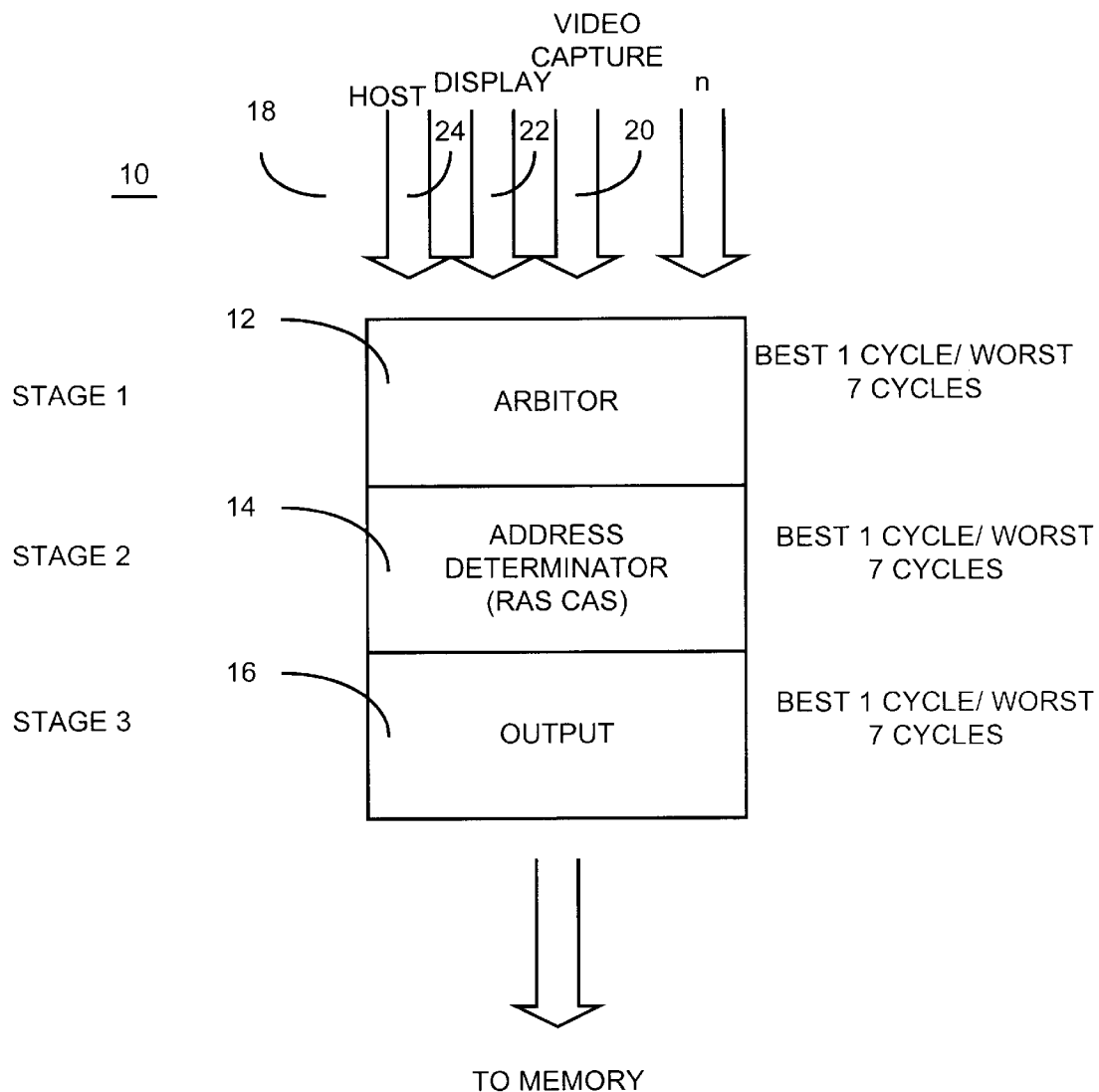


FIG. 1
PRIOR ART

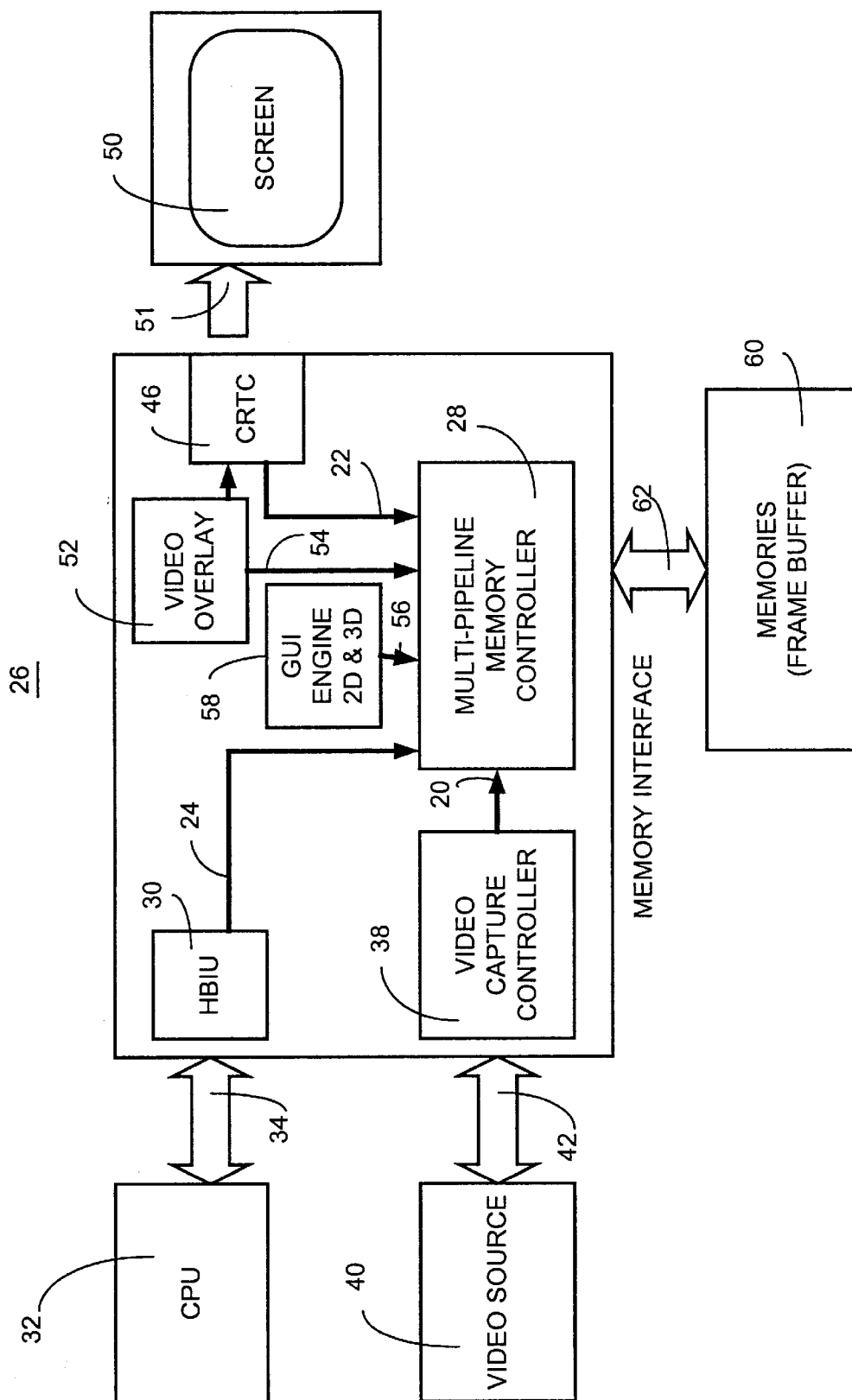


FIG. 2

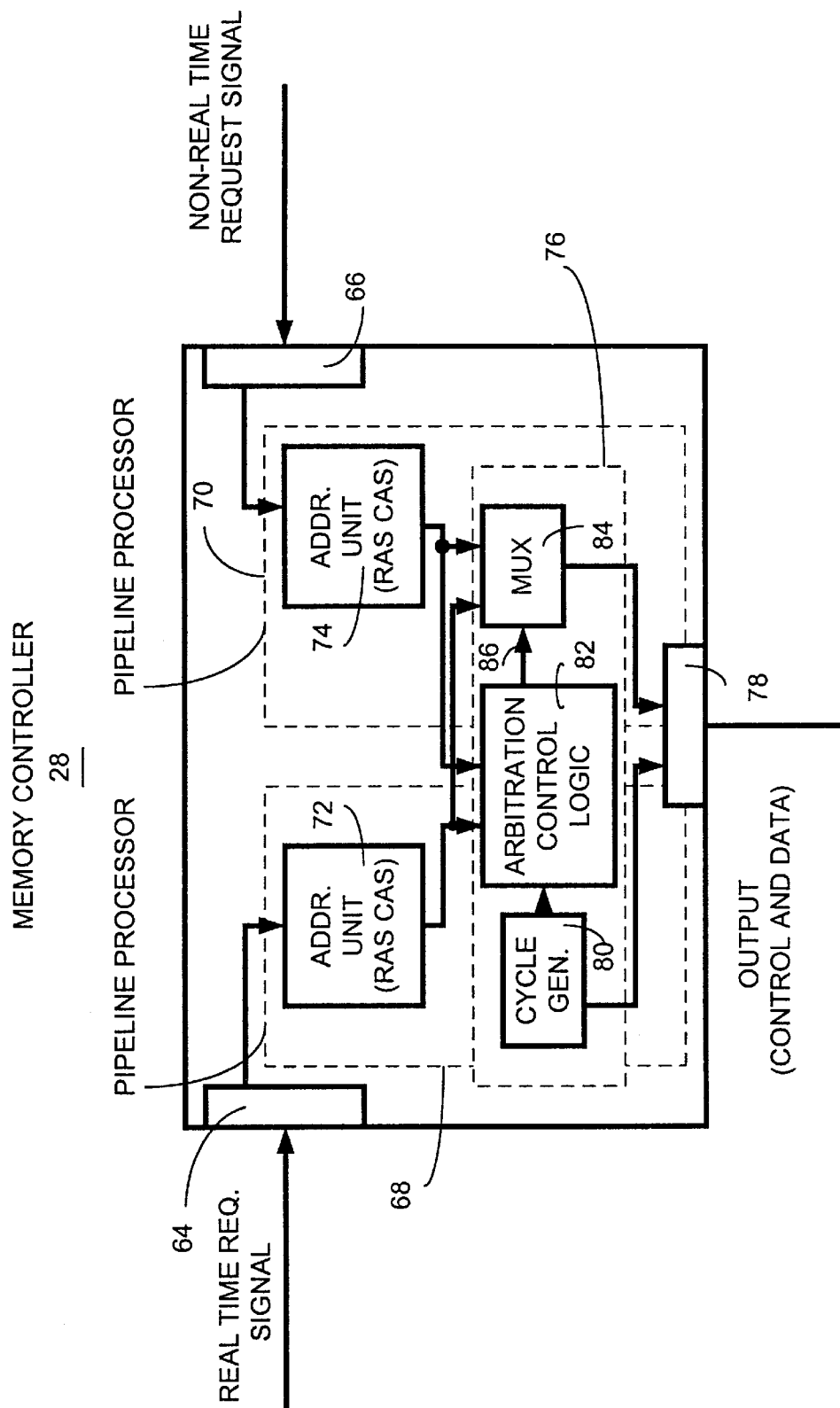


FIG. 3

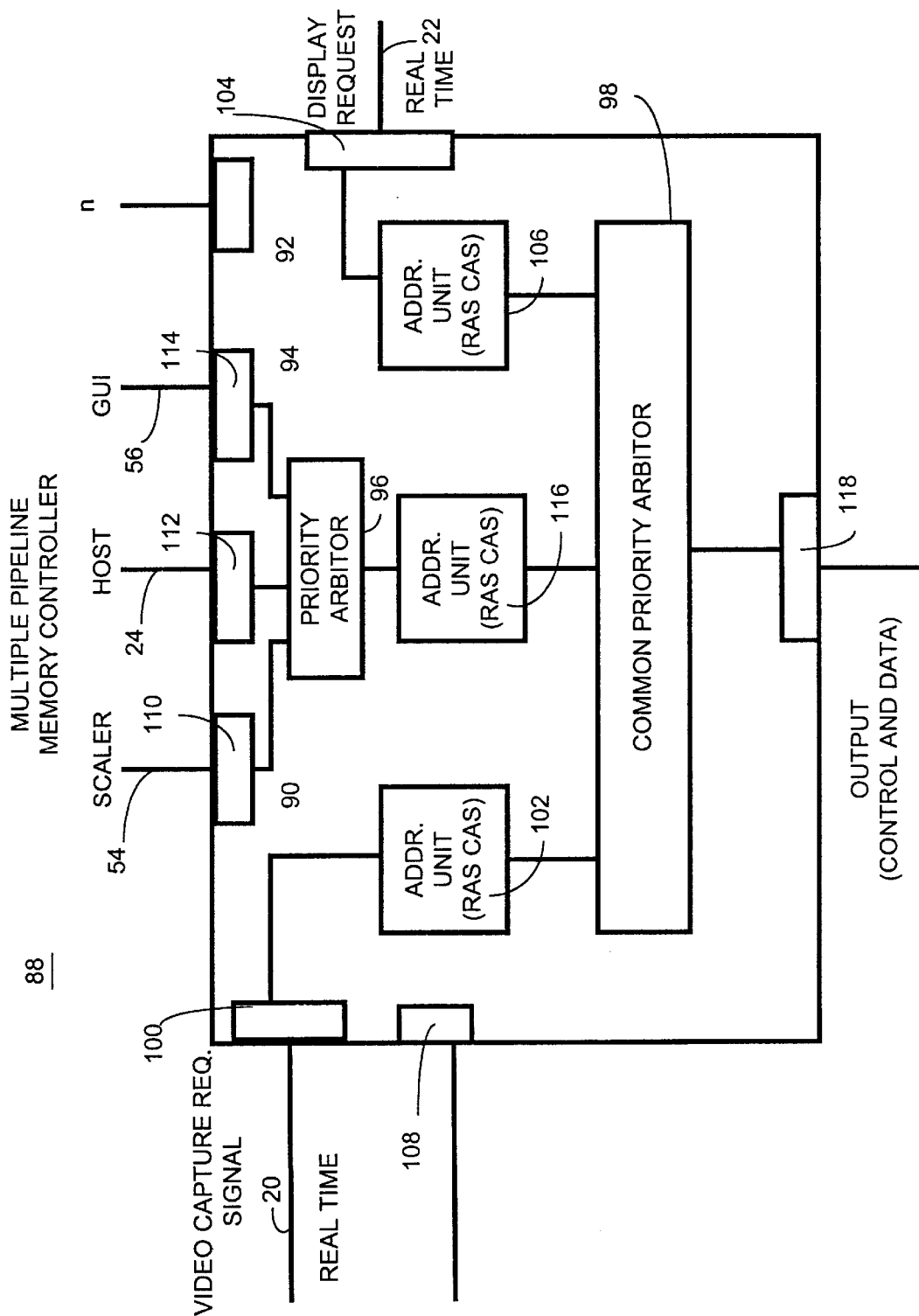


FIG. 4

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