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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
04/22/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	JONI HSU	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/25/10*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____ .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on January 25, 2010 was filed after the mailing date of the application on June 12, 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Arguments

2. Applicant's arguments filed January 25, 2010 have been fully considered but they are not persuasive.

3. Applicant argues that it is improper to use hindsight reconstruction and ignore the teachings of the reference as a whole in an effort to render a claim obvious (p. 9).

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

4. As per Claim 1, Applicant argues that the separate modules from the memory controller 310 provide the specific scalability provided by the architecture of Perego (US006864896B2). Perego requires the separate memory controller 310 to be off chip and separate from the memory

modules. As such, combining the graphic pipeline teachings of Perego with those of MacInnis (US006570579B1) would render the Perego system inoperable (p. 10).

In reply, the Examiner respectfully points out that the main reference MacInnis is used to teach that the graphics pipeline (58, Fig. 2) and the memory controller (54) are on the same chip (10) (Fig. 2; col. 4, lines 65-67; col. 5, lines 36-41). Perego is used for its teaching of two graphics pipelines on the same chip to process data in a set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the two graphics pipelines operative to process data in a dedicated tile; wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions. Perego is used as a secondary reference to modify the device of the main reference MacInnis. Thus, these teachings from the secondary reference Perego are being implemented into the device of the main reference MacInnis. Perego is not being used as the main reference, and so the teaching that the graphics pipeline and the memory controller are on the same chip from MacInnis is not being implemented into the device of Perego to render the device of Perego inoperable. Since these teachings from the secondary reference Perego are being implemented into the device of the main reference MacInnis, and the device of the main reference MacInnis is still operable after this implementation, the combination is proper.

5. Applicant argues that the shared memories 314 of Perego are dedicated memories that are each dedicated to a dedicated graphics pipeline and in no embodiment are these dedicated memories that are on separate modules ever described as storing data from more than one rendering engine. This is because this would eliminate the advantages of Perego's scalable unified memory architecture (p. 10). As shown in Fig. 8, memory devices 804 are only in

communication with rendering engine 8012 whereas memory devices 812 are only in communication with rendering engine 810. These memories are dedicated and are separate and are not shared among graphics pipelines or rendering engines 802 and 810 (p. 11).

In reply, the Examiner points out that Perego describes "The shared memory 314 typically includes multiple memory devices coupled together to form a block of storage space" (col. 4, lines 8-10). Thus, the block of storage space is considered to be a memory shared among the two graphics pipelines. Claim 1 recites "at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile…wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions", and Claim 2 recites "wherein the square regions comprise a two dimensional partitioning of memory". Since each graphics pipeline processes a dedicated tile that is a square region, and each square region is a partition of memory, this means that each graphics pipelines stores data to a partition of memory. Since Perego teaches that each graphics pipeline stores data to a partition of the block of storage space, and the block of storage space is shared among the two graphics pipelines (col. 1, lines 44-54; col. 3, lines 3-6, 65-67; col. 4, lines 1-10, 48-65; col. 5, lines 42-44), Perego reads on the limitations as recited in the claim.

6. As per Claim 24, Applicant argues that Fig. 8 of Perego shows separate front end circuitry being employed since separate rendering engines 802 and 810 are employed and each of these are identical in structure. Thus, Perego does not teach that there is one front end circuitry that sends pixel data to both the first back end circuitry and the second back end circuitry (p. 11).

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