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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

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EXAMINER
HSU, JONI

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/28/07*

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other:

DETAILED ACTION

Information Disclosure Statement

1. Information disclosure statement (IDS) submitted on November 28, 2007 was filed after mailing date of application on June 12, 2003. Submission is in compliance with provisions of 37 CFR 1.97. Accordingly, information disclosure statement is being considered by the examiner.

Response to Arguments

2. Applicant's arguments, see pages 9-11, filed November 28, 2007, with respect to the rejection(s) of claim(s) 1-4, 7, 10, 12, 14, 20-22, and 25 under 35 U.S.C. 102(e) and claims 5, 6, 11, 13, 15-19, and 24 under 35 U.S.C. 103(a) have been fully considered and are persuasive. So, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Furtner (US006778177B1) and MacInnis (US006570579B1).

3. Applicant argues Perego (US006864896B2) does not teach multi-graphics pipeline circuitry on same chip nor memory controller on the same chip but instead teaches discrete memory modules having separate and single graphics engines thereon. The memory controller taught in Perego is not on a same chip nor is it part of the memory module (page 10).

In reply, new grounds of rejection are made in view of Furtner and MacInnis.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-4, 6, 7, 10, 12, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Furtner (US006778177B1), further in view of MacInnis (US006570579B1).

6. As per Claim 1, Perego teaches graphics processing circuit (300, Fig. 3; c. 3, ll. 61-63) having at least 2 graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least two graphics pipelines operative to process data in dedicated tile (c. 5, ll. 19-27, 38-44); and memory controller (310, Fig. 3) in communication with at least 2 graphics pipelines (312), operative to transfer pixel data between each of 1st pipeline and 2nd pipeline and shared memories (314) (c. 3, ll. 65-67; c. 4, ll. 1-10, 48-65). Shared memories (314) are each part of main memory (c. 1, ll. 44-54; c. 3, ll. 3-6), and so are considered to be one memory. Repeating tile pattern includes horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (c. 5, ll. 19-27, 38-44).

However, Perego does not teach that the graphics pipelines are on a same chip. However, Furtner teaches that the graphics pipelines are on a same chip (c. 6, ll. 30-32).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Perego so graphics pipelines are on same chip as suggested by Furtner. Placing plurality of modules on single chip takes up less space as compared to using multiple chips, and this is well-known in the art.

However, Perego and Furtner do not teach memory controller is also on the same chip. However, MacInnis teaches memory controller (54) is on same chip (10) as graphics pipeline (58), as shown in Fig. 2 (c. 4, ll. 65-67; c. 5, ll. 36-41; c. 6, ll. 10-13). This would be obvious for same reasons given above.

7. As per Claim 2, Perego teaches square regions have two dimensional partitioning of memory (c. 5, ll. 19-33).

8. As per Claim 3, Perego discloses that the memory is a frame buffer (c. 5, ll. 32-33).

9. As per Claim 4, Perego teaches each of at least two graphics pipelines includes front end circuitry (308, Fig. 3) operative to generate pixel data corresponding to primitive to be rendered, and back end circuitry (312), coupled to front end circuitry, operative to receive and process portion of pixel data (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44). In order for front end circuitry (308) to generate pixel data, it must inherently receive vertex data.

10. As per Claim 6, Perego does not explicitly teach each tile of set of tiles has 16x16 pixel array. But, Furtner teaches each tile of set of tiles has 16x16 pixel array (c. 11, ll. 45-48, 64-65).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego so each tile of set of tiles further has 16x16 pixel array because Furtner suggests depending on number of parallel image-rendering pipelines and depending on memory organization, optimum tile size and shape can be selected (c. 11, ll. 45-48, 64-65), and

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