

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicants: Mark M. Leather et al.  
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Examiner: Joni Hsu  
Art Unit: 2628  
Our File No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING  
A SUPER-TILING TECHNIQUE**

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Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**AMENDMENT AND RESPONSE**

Dear Sir:

In response to the Office Action mailed August 28, 2007, Applicants respond as follows.

**Amendments to the Specification** begin on page 2 of this paper.

**Amendments to the Claims** begin on page 3 of this paper.

**Remarks** begin on page 9 of this paper.

**Amendments to the Specification:**

Please replace paragraph [0001] with the following amended paragraph:

[0001] This is a related application to a co-pending application entitled “Parallel Pipeline Graphics System” ~~having docket number 010025~~, having serial number 10/724,384, having Leather et al. as the inventors, filed on ~~even date~~ November 26, 2003, owned by the same assignee and hereby incorporated by reference in its entirety.

**Amendments to the Claims:**

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

**Listing of Claims:**

1. (currently amended) A graphics processing circuit, comprising:  
  
at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile;  
  
and  
  
a memory controller on the chip in communication with the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory;  
  
wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.
2. (original) The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.
3. (original) The graphics processing circuit of claim 2, wherein the memory is a frame buffer.
4. (original) The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. (original) The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

6. (original) The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

8. (canceled)

9. (canceled)

10. (original) The graphics processing circuit of claim 4, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. (original) The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. (previously presented) The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern.

13. (previously presented) The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to front end circuitry and back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

14. (original) The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. (original) The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for

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