

EXHIBIT 1

**Exhibit A – AST’s Preliminary Infringement Contentions
Claim Chart of Asserted Claims – U.S. Patent No. 7,804,435**

The following is intended to provide examples of infringement by NXP’s i.MX family of microprocessor products with substantially similar features and functionality (the “Accused Instrumentalities”), without limitation. The following claim chart supplements the allegations made in the Complaint (ECF No. 1) and Exhibit A (ECF No. 1) and incorporates by reference in full. This preliminary claim chart exists to supply reasonable notice of AST’s infringement, not an exhaustive recitation of every possible theory and instance of infringement. The claim construction process is ongoing, and AST’s factual investigation remains ongoing, and AST believes NXP and third parties uniquely possess information regarding infringement of these asserted claims, including source code. AST thus cannot provide its complete and final construction of the asserted claims until discovery as to the Accused Instrumentalities, including inspection and source code review.

Claim 1	Evidence of Infringement
<p>[1a] An apparatus comprising:</p>	<p>The Accused Instrumentalities are or include an apparatus within the meaning of this claim. For example and not limitation, the i.MX QuadMax Applications Processor is an application processor including a Video Processing Unit.</p> <p style="text-align: center;">This chapter introduces the i.MX 8QuadMax (i.MX8QM). The i.MX8QM is a fully comprehensive multimedia device targeting high-end automotive and industrial market segments. The chip is built using a leading edge process to achieve both high-performance and low-power consumption. The chip relies on a powerful fully-coherent core complex based on a dual (2x) Cortex-A72 cluster for use-cases requiring high-computing performances and a quad (4x) Cortex-A53 cluster running most of the use-cases at a lower-power consumption.</p> <p>See i.MX 8QuadMax Applications Processor Reference Manual, § 1.1.1, Document NXP Rev 0, 9/2021 (downloaded from nxp.com).</p> <ul style="list-style-type: none"> • 1x VPU <ul style="list-style-type: none"> • 4x M0+ processors with 16KB Cache (1x for decode, 2x for encode, 1x for transport stream) • Supports H.265 decode (4Kp60) • Supports H.264 decode (4Kp30) • H.264 encoder (1080p30) <p>See i.MX 8QuadMax Applications Processor Reference Manual, § 1.1.2, Document NXP Rev 0, 9/2021 (downloaded from nxp.com).</p>

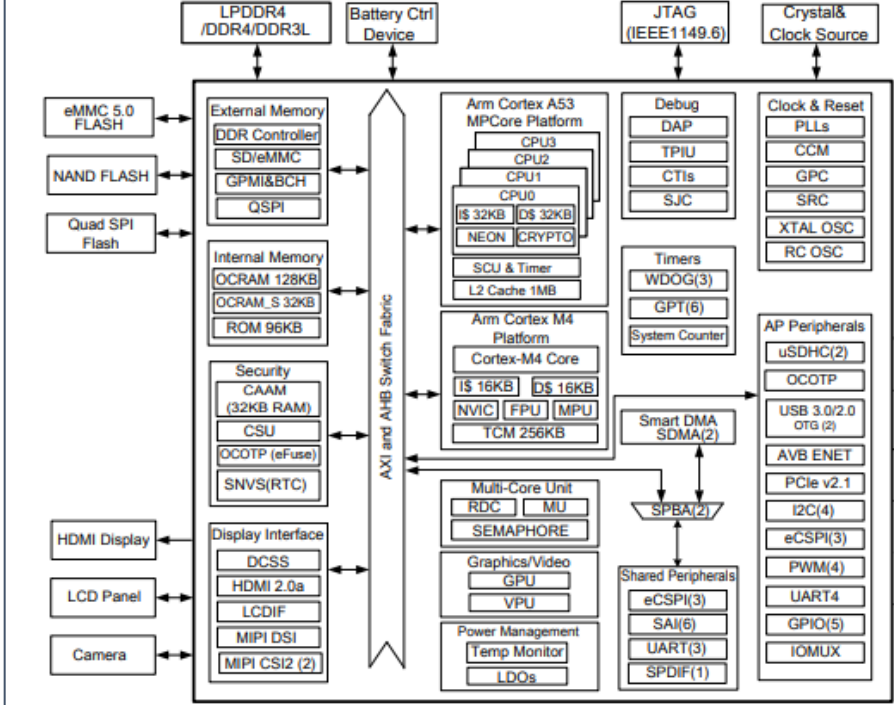
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	<p>As another example, the i.MZ 8M Applications Processors are applications processors Processing Unit.</p> <div style="border: 1px solid black; padding: 10px; margin: 10px 0;"> <p>1.1 Product Overview</p> <p>This chapter introduces the architecture of the i.MX 8M Dual/8M QuadLite/ Applications Processors.</p> <p><u>The i.MX 8M Dual/8M QuadLite/8M Quad is a family of products focused on an excellent 4K video and audio experience, combining media-specific features with high-performance processing optimized for low-power consumption.</u></p> <p>1.2 Target Applications</p> <p><u>The i.MX 8M Dual/8M QuadLite/8M Quad Applications Processors achieve high performance and low power consumption and rely on a powerful, fully-coherent system-on-chip complex based on a quad Cortex-A53 cluster, with graphics processing GPU and support for the latest graphic APIs.</u></p> </div> <p>i.MX 8M Dual/8M QuadLite/8M Quad Applications Processors Reference Manual, § 1.1.1, IMX8MDQLQRM, Rev. 3.1, 06/2021 (downloaded from nxp.com).</p>

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	<p>1.4.10 Video Processing Unit (VPU)</p> <p>The chip incorporates the following Video Processing Unit (VPU) features:</p> <ul style="list-style-type: none"> • VP9 Profile 0, 2 (10 bit) decoder (VPU G2) • HEVC/H.265 Main, Main10 decoder (VPU G2) • AVC/H.264 Baseline, Main, High decoder (VPU G1) • VP8 decoder (VPU G1) • Frame Buffer Compression – Lossless compression of buffers • TrustZone support <p>i.MX 8M Dual/8M QuadLite/8M Quad Applications Processors Reference Manual, § No.: IMX8MDQLQRM, Rev. 3.1, 06/2021 (downloaded from nxp.com).</p>

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	<p>1.5.1 Block Diagram</p> <p>The high-level block diagram is shown in the figure below.</p>  <p>Figure 1-1. Block Diagram</p> <p>i.MX 8M Dual/8M QuadLite/8M Quad Applications Processors Reference Manual, § No.: IMX8MDQLQRM, Rev. 3.1, 06/2021 (downloaded from nxp.com).</p> <p>Further details about how the Accused Instrumentalities disclose this limitation are de to elements [1b], [1c], and [1d] below.</p>

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