

EXHIBIT B
U.S. Patent No. 8,933,945

Claim 1	Exemplary Accused Product: NXP i.MX 8QuadMax Applications Processor
A graphics processing circuit, comprising:	<p>To the extent that the preamble is limiting, the NXP processors meet this limitation.</p> <p>The NXP processors perform graphics processing. To illustrate:</p> <div style="border: 1px solid black; padding: 10px;"> <p>Graphics processing is handled by two (2x) Graphics Processing Units (GPU) some of the latest graphic APIs including OpenVX for computer vision. Video managed by a dedicated video engine with decoding formats including HEVC to 4K60, H.264 up to 4K30 and encoding in H.264 up to 1080p30. The chip supports various display interfaces that supports up to four displays. In order to feed high demanding blocks, i.MX8QM has two (2) DRAM controllers supporting LPDDR4 memory types.</p> </div> <p>i.MX 8QuadMax Applications Processor Reference Manual, § 1.1.1, Document No.: I 9/2021 (downloaded from nxp.com).</p> <p>The NXP processors include one or more Graphics Processing Unit (GPU) subsystems or more GPUs. To illustrate:</p> <div style="border: 1px solid black; padding: 10px;"> <p>16.1.1 Overview</p> <p>This section provides a high-level overview of the Graphics Processing Unit subsystem and the Video Processing Unit (VPU) subsystem on the chip.</p> <p>16.1.1.1 GPU</p> <div style="border: 2px solid red; padding: 5px;"> <p>This chip embeds two identical GPU sub-systems.</p> </div> </div> <p><i>Id.</i>, § 16.1.1. To illustrate further:</p>

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	<div> <p>Figure 16-1. Simplified Block Diagram</p> </div> <p><i>Id.</i></p>

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at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations,	<p>On information and belief, the NXP processors meet this limitation.</p> <p>For instance, the NXP processors perform “massively parallel data processing” across engines,” and “each compute unit has its own arithmetic logic units (ALUs) . . . that ca computations.”</p> <div style="border: 1px solid black; padding: 5px;"><p>OpenCL uses parallel execution SIMD (single instruction, multiple data) engines found in GPU computational density by performing massively parallel data processing on multiple data iter compute engines. Each compute unit has its own arithmetic logic units (ALUs), including pipe (FP), integer (INT) units and a special function unit (SFU) that can perform computations as w operations. The parallel computations and associated series of operations are called a kernel can execute a kernel on thousands of work-items in parallel at any given time.</p></div> <p>i.MX Graphic User’s Guide, § 5.1.1, Document No. IMXGRAPHICUG, Rev. 0, 05/20 https://www.nxp.com/docs/en/user-guide/i.MX_AA_Graphics_User's_Guide.pdf.</p> <p>To illustrate further, NXP’s user guides show the Vivante OpenCL data pipeline used NXP’s public demonstrations of its processors depicts the use of multiple graphics pip</p>

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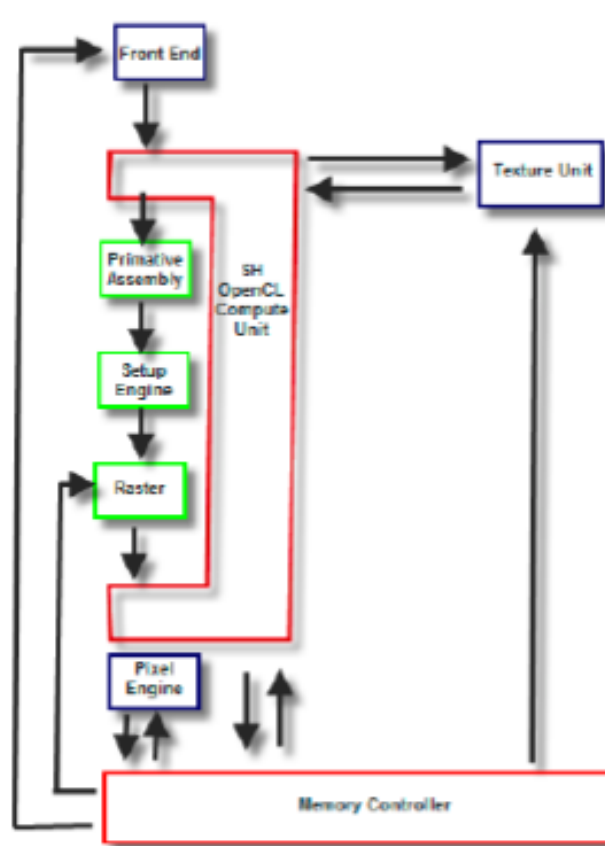
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	<p>5.2.1 OpenCL pipeline</p>  <p style="text-align: center;">Figure 4 Vivante OpenCL data pipeline for an OpenCL co</p> <p><i>Id.</i>, § 5.2.1. To illustrate further, the NXP processors exhibit “massive data parallelism rasterization”:</p>

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	<div style="text-align: center;"> <h3>Scalable Ultra-Threaded Unified Shader</h3> </div> <div> <ul style="list-style-type: none"> • Architectural Features <ul style="list-style-type: none"> - Massive data parallelism - Up to 16x SIMD Vec-4 shaders - Balanced performance/bandwidth <ul style="list-style-type: none"> ▪ Tile rasterization ▪ Many caches ▪ Fast depth culling ▪ Fast clear ▪ Texture compression - Native OpenGL ES 3.2 rendering - High quality 4x MSAA anti-aliasing - Up to 256 independent threads per shader operate on discrete data in parallel </div> <div> </div> <div style="text-align: center;"> <p>13 PUBLIC USE #NXPFTF</p> </div>
	<p>R. Malewski, i.MX 8 Graphics Architecture, FTF-DES-N1940, FTF 2016 Technology (2016), https://community.nxp.com/pwmxy87654/attachments/pwmxy87654/ftf2016/8/N1940%20i.MX%208%20Graphics%20Architecture.pdf. The presence of multiple sh engines, textures engines, and pixel engines indicates the presence of multiple pipeline</p> <p>On information and belief, the pipelines are operative to process data in a corresponding repeating tile pattern corresponding to screen locations. As shown in the figure above, use “tile rasterization,” which is believed to refer to a rasterizer that rasterizes graphics and with the tiles comprising a repeating tile pattern corresponding to screen locations the processor also includes additional references to tiles.</p>

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