**UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

FUTURE LINK SYSTEMS, LLC,	
Plaintiff,	Case No. 6:21-cv-0263-ADA
v.	
APPLE INC.,	JURY TRIAL DEMANDED
Defendant.	
FUTURE LINK SYSTEMS, LLC,	
Plaintiff,	Case No. 6:21-cv-0264-ADA
v.	
BROADCOM INC.; BROADCOM CORP.,	JURY TRIAL DEMANDED
Defendants.	
FUTURE LINK SYSTEMS, LLC,	
Plaintiff,	Case No. 6:21-cv-0265-ADA
v.	
QUALCOMM INCORPORATED; QUALCOMM TECHNOLOGIES, INC.,	JURY TRIAL DEMANDED
Defendants.	
FUTURE LINK SYSTEMS, LLC,	
Plaintiff,	Case No. 6:21-cv-0363-ADA
v.	
REALTEK SEMICONDUCTOR CORPORATION,	JURY TRIAL DEMANDED
Defendant.	

**PLAINTIFF FUTURE LINK SYSTEMS, LLC'S RESPONSE TO CRSR
DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF**

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I.   INTRODUCTION

Plaintiff Future Link Systems, LLC ("FLS") submits this response to CRSR Defendants' ("Defendants") Opening Claim Construction Brief ("Op. Br."). As set forth below, the disputed terms have a plain and ordinary meaning to a POSA, and Defendants' attempts to rewrite the claims or hold them indefinite should be rejected.

II.   THE '804 PATENT

A. "A circuit arrangement for interfacing a plurality of functional blocks to one another in an integrated circuit device, the circuit arrangement comprising" (claim 1)

FLS's Proposed Construction	Defendants' Proposed Construction
Limiting	Not limiting

As Defendants acknowledge, a preamble may be limiting when it recites "essential structure or steps, or is 'necessary to give life, meaning, and vitality to the claim." Op. Br. at 3. What Defendants do not acknowledge, however, is that preambles may also be limiting "when reciting additional structure or steps underscored as important by the specification." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002).

Here, the preamble is limiting because the preamble recites structure underscored as important by the specification—that the claimed "circuit arrangement" is "in an integrated circuit device." The specification repeatedly teaches the importance of implementing the invention within an integrated circuit device, starting with the title of the '804 Patent: "Concurrent serial interconnect for integrating functional blocks *in an integrated circuit device*." Likewise, the field of the invention states:

The invention is generally related to integrated circuit device design and architecture, and in particular, to an interface for interconnecting multiple functional blocks together *in an integrated circuit device*.

'804 Patent at 1:6-9. Likewise, the background of the invention repeatedly emphasizes the importance of advances in integrated circuit design, as well as the difficulties that arise within the specific field of integrated circuit architecture. *See, e.g.*, *id.* at 1:12-42, 2:21-23, 2:58-64:

Computer technology has advanced a great deal over the last several decades. Whereas computers once filled entire rooms, and were constructed using individually packaged transistors and/or vacuum tubes to perform different logical functions, ***innovations in semiconductor manufacturing techniques have enabled multiple transistors, or logic gates, to be integrated together on a single integrated circuit device, or "chip"*** to perform a greater number of logical functions. *The size and number of logic gates that can be integrated together on a chip continues to improve, and whereas early chips had at most only a few hundred gates, more recent chips have been developed that incorporate more on the order of millions of gates. Furthermore, advances in integration have permitted designs that were at one time implemented using multiple chips to be implemented in a single chip.*

As chip designs become more complex, however, the design and development process becomes more expensive and time consuming. To alleviate this difficulty, design tools have been developed that enable developers to build custom chips by assembling together smaller, generic components that perform basic functions required for the design.

…

The ability to integrate greater numbers of gates onto a chip has also permitted the complexity of the generic components used by design tools to increase.

…

However, bus-type interconnections suffer from a number of drawbacks that limit their usefulness in ***interconnecting multiple functional blocks in a chip***.

…

Therefore, ***a significant need exists in the art for an improved manner of interconnecting components*** such as functional blocks and the like ***in an***

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