IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

FUTURE LINK SYSTEMS, LLC Plaintiff, v. APPLE INC., Defendant.	Civil Action No. 6:21-cv-00263-ADA **JURY TRIAL DEMANDED**
FUTURE LINK SYSTEMS, LLC Plaintiff, v. BROADCOM INC., BROADCOM CORP., Defendants.	Civil Action No. 6:21-cv-00264-ADA **JURY TRIAL DEMANDED**
FUTURE LINK SYSTEMS, LLC Plaintiff, v. QUALCOMM INCORPORATED, QUALCOMM TECHNOLOGIES, INC., Defendants.	Civil Action No. 6:21-cv-00265-ADA **JURY TRIAL DEMANDED**
FUTURE LINK SYSTEMS, LLC Plaintiff, v. REALTEK SEMICONDUCTOR CORPORATION, Defendant.	Civil Action No. 6:21-cv-00363-ADA **JURY TRIAL DEMANDED**

APPLE INC., BROADCOM INC., BROADCOM CORP., QUALCOMM INCORPORATED, QUALCOMM TECHNOLOGIES, INC. AND REALTEK SEMICONDUCTOR CORPORATION'S OPENING CLAIM CONSTRUCTION BRIEF
U.S. PATENT NOS. 7,917,680, 6,317,804, and 6,807,505

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INTRODUCTION

Apple Inc. ("Apple"), Broadcom Inc., Broadcom Corp. (collectively "Broadcom"), Qualcomm Incorporated, Qualcomm Technologies, Inc. (collectively "Qualcomm"), and Realtek Semiconductor Corporation ("Realtek") (collectively, the "CRSR Defendants") hereby jointly submit this opening claim construction brief pursuant to the Court's Joint Agreed Scheduling Order, to construe terms of U.S. Patent Nos. 7,917,680 (the "'680 patent"); 6,317,804 (the "'804 patent"); and 6,807,505 (the "'505 patent").[1] *See* Dkt. No. 29 (Joint Agreed Scheduling Order) at 3.

I. OVERVIEW OF THE TECHNOLOGY

A. The '804 Patent

The '804 patent, entitled "Concurrent Serial Interconnect for Integrating Functional Blocks in an Integrated Circuit Device," relates to an arrangement and method for arranging functional blocks to interface via serial interconnects. '804 Patent, Abstract. The patent describes that functional blocks are associated with serial ports, which are, in turn, selectively coupled to each other by way of an interface controller. *See id.* at Abstract, 2:66-3:12, cl. 1. These functional blocks, according to the patent, can be "difficult" to implement as a result of their communication requirements. *Id.* at 1:48-65. The patent teaches that relying on parallel, or bus-type, interconnections to solve this problem "suffer[s] from a number of drawbacks." *Id.* at 2:21-23; *see also id.* at 2:32-57 (describing that parallel architectures are undesirable because, *inter alia*, they use additional space, can have slower transmission, and may allow transmission

[1] Future Link is asserting the '505 patent against Apple alone. *See Future Link Sys. v. Apple, Inc.*, Case No. 6:21-cv-00263-ADA (W.D. Tex. 2020), Dkt. No. 1. Neither Future Link nor Apple identified any term from the '505 patent that required construction. As a result, there are no disputed claim constructions for the '505 patent.

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