Exhibit 6

U.S. Patent No. 6,807,505 ("'505 Patent")

Accused Products

Apple products including computers containing JEDEC DDR4 SDRAM and related versions, such as the ("Apple Mac Pro") infringe at least Claim 1 of the '505 Patent.

Claim 1

Claim 1	Apple Mac Pro
1[pre]. An electronic circuit comprising:	To the extent the preamble is limiting, the Apple Mac Pro comprise circuit as claimed. For example, the Apple Mac Pro includes at least 32GB of 2666MI memory compliant to DDR4 JEDEC Standard JESD79-4, Sep. 201 *See, e.g.*:

Claim 1	Apple Mac Pro
	Memory Configure up to 1.5TB of DDR4 ECC memory in 12 user-accessible DIMM slots **32GB** Four 8GB DIMMs **48GB** Six 8GB DIMMs **96GB** Six 16GB DIMMs **192GB** Six 32GB DIMMs **384GB** Six 64GB DIMMs **768GB** Six 128GB DIMMs or **1.5TB** 12 128GB DIMMs Requires 24-core or 28-core processor. https://www.apple.com/mac-pro/specs/
1[a] a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects,	The Apple Mac Pro comprises a plurality of input/output (I/O) node electronic circuit to a further electronic circuit via interconnects. For example, the DDR4 memory within the Apple Mac Pro include pins/nodes, such as BA0-1, BG0-1, A0-A9, A10/AP, A11, A12/BC

Claim 1	Apple Mac Pro
	WE_n/A14, CAS_n/A15, RAS_n/A16, RESET_n, CKE, ACT_n, C CLK_c, DML_n, DBIL_n, DMU_n/DBIU_n, Parity, and Alert_n, t connect the DDR4 SDRAM to a further electronic circuit (e.g., mer processor chip) via interconnecting wires between the I/O pins and electronic circuit. *See, e.g.*: **Table 50 — Pin Classification of DDR4 Memory Device in Connectivity** **Pin Type in CT Mode** | **Pin Names during Normal Memory Opera** Test Enable | TEN Chip Select | CS_n Test Input | BA0-1, BG0-1, A0-A9, A10/AP, A11, A12/BC_n, A13, WE_n/A14 RESET_n, CKE, ACT_n, ODT, CLK_t, CLK_c, DML_n, DBIL_n, DM Test Output | DQ0-DQ15, DQSU_t, DQSU_c, DQSL_t, DQSL_c DDR4 JEDEC Standard JESD79-4, Sep. 2012.

Claim 1	Apple Mac Pro

2.6 Pinout Description

Symbol	Type	Function
BG0 - BG1	Input	Bank Group Inputs : BG0 - BG1 define to which bank grou Precharge command is being applied. BG0 also determine accessed during a MRS cycle. X4/8 have BG0 and BG1 b
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Precharge command is being applied. Bank address also register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE C address for Read/Write commands to select one location respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_ additional functions, see other rows.The address inputs al Mode Register Set commands.A17 is only defined for the
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write comm Autoprecharge should be performed to the accessed bank operation. (HIGH: Autoprecharge; LOW: no Autoprecharg Precharge command to determine whether the Precharge LOW) or all banks (A10 HIGH). If only one bank is to be pr by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Writ burst chop (on-the-fly) will be performed. (HIGH, no burst See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RE when RESET_n is HIGH. RESET_n must be HIGH during a CMOS rail to rail signal with DC high and low at 80% an

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