

Exhibit 5



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De Jong et al.

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(54) **CIRCUIT WITH INTERCONNECT TEST UNIT**

(75) Inventors: **Franciscus G. M. De Jong**, Eindhoven (NL); **Mathias N. M. Muris**, Eindhoven (NL); **Robertus M. W. Raaijmakers**, Eindhoven (NL); **Guillaume E. A. Lousberg**, Eindhoven (NL)

(73) Assignee: **Koninklijke Philips Electronics N.V.**, Eindhoven (NL)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/621,002**

(22) Filed: **Jul. 16, 2003**

(65) **Prior Publication Data**

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Related U.S. Application Data

(62) Division of application No. 09/402,154, filed as application No. PCT/IB99/00172 on Jan. 29, 1999, now Pat. No. 6,622,108.

(30) **Foreign Application Priority Data**

Feb. 22, 1998 (EP) 98200288
May 6, 1998 (EP) 98201482
Nov. 30, 1998 (EP) 98204042

(51) **Int. Cl.**⁷ **G01R 31/28**

(52) **U.S. Cl.** **702/118; 324/500**
(58) **Field of Search** 702/57-59, 108, 702/117, 118; 324/500, 512, 527; 326/16, 106; 714/25, 27, 30, 718, 719, 726, 727, 733

(56) **References Cited**

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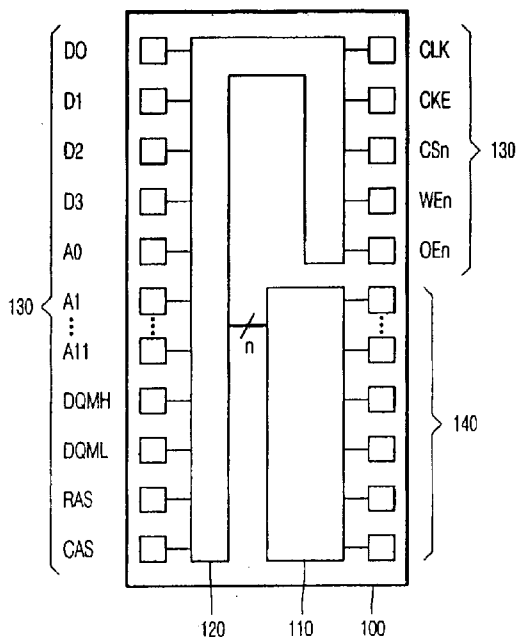
* cited by examiner

Primary Examiner—Marc S. Hoff
Assistant Examiner—Craig Steven Miller

(57) **ABSTRACT**

An electronic circuit comprises a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects. A main unit implements a normal mode function of the electronic circuit. A test unit tests the interconnects. The electronic circuit has a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit. In the test mode the test unit is operable as a low complexity memory via the I/O nodes.

9 Claims, 3 Drawing Sheets



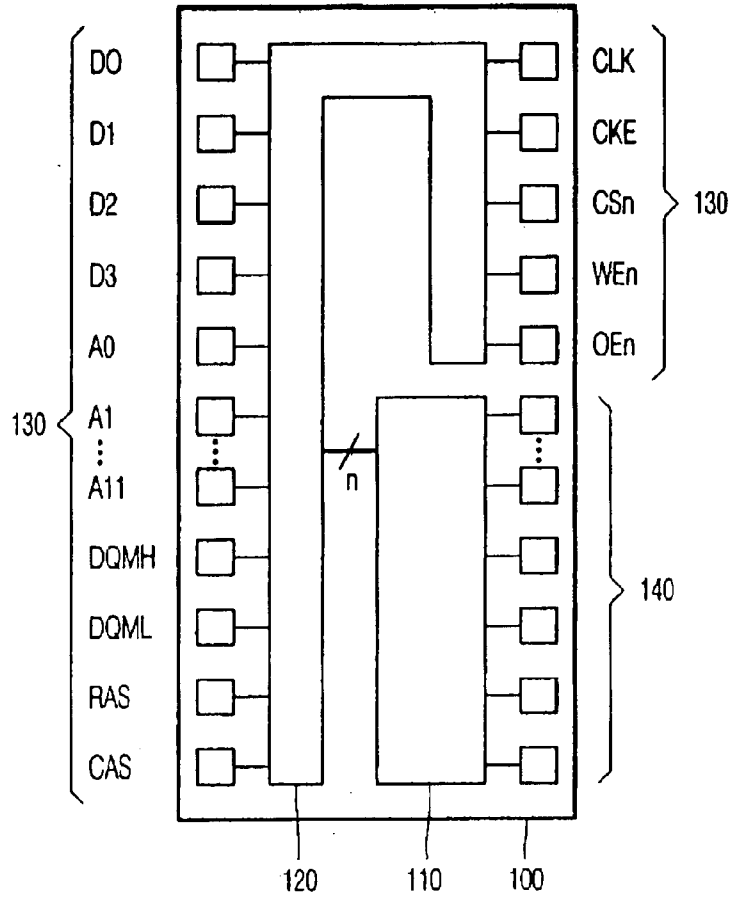


FIG. 1

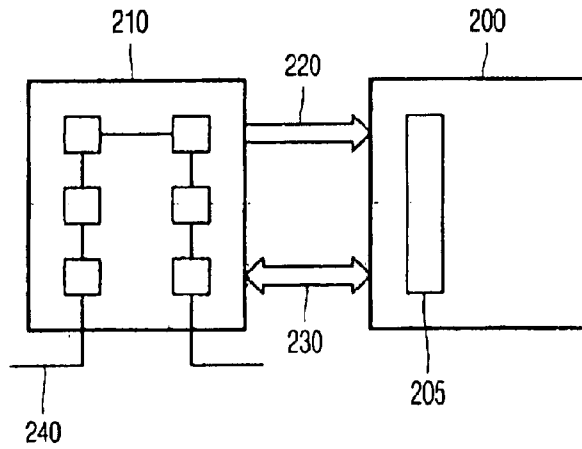


FIG. 2

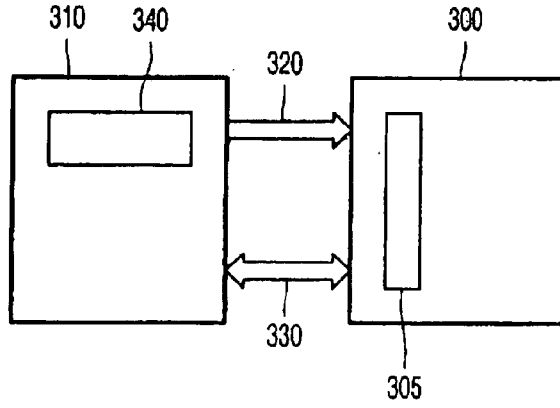


FIG. 3

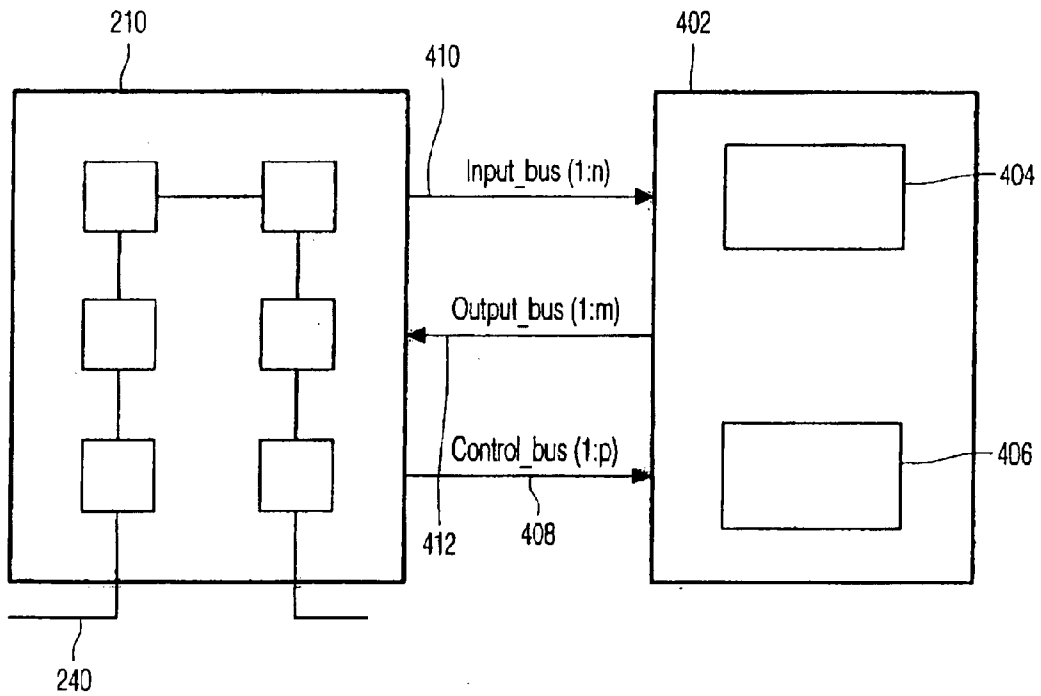


FIG. 4

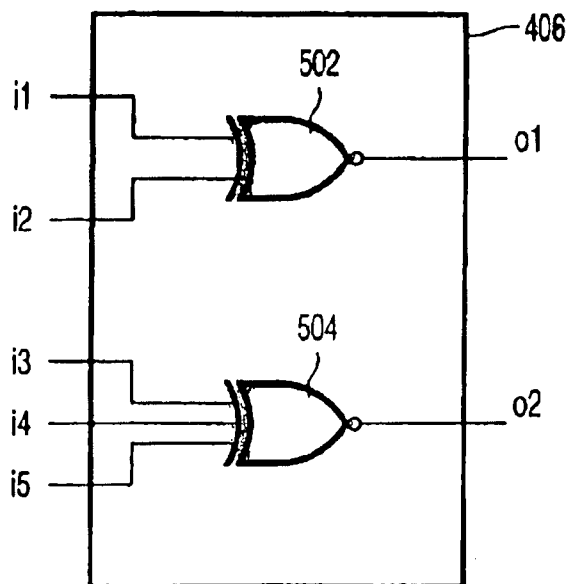


FIG. 5

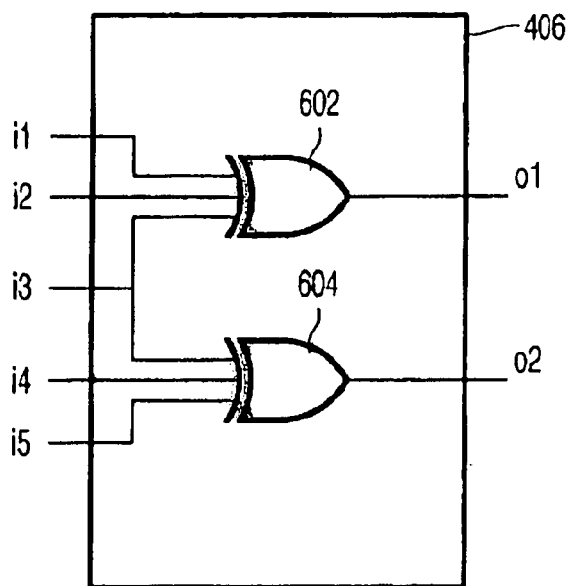


FIG. 6

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