

# Exhibit 3

(12) **United States Patent**  
**De Jong et al.**

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(45) **Date of Patent:** **Sep. 16, 2003**

(54) **CIRCUIT WITH INTERCONNECT TEST UNIT AND A METHOD OF TESTING INTERCONNECTS BETWEEN A FIRST AND A SECOND ELECTRONIC CIRCUIT**

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(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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Nov. 30, 1998 (EP) ..... 98204042

(51) **Int. Cl.<sup>7</sup>** ..... **G01R 31/28**

(52) **U.S. Cl.** ..... **702/118; 324/500**

(58) **Field of Search** ..... 702/57-59, 108, 702/117, 118; 324/500, 512, 527; 326/16, 106; 714/FOR 100, 25, 27, 30, 718, 719, 726, 727, 733

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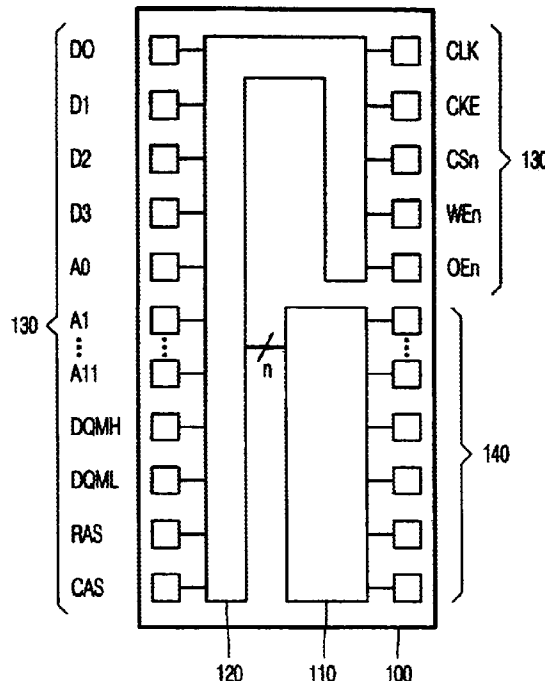
*Primary Examiner*—Marc S. Hoff

*Assistant Examiner*—Craig Steven Miller

(57) **ABSTRACT**

An electronic circuit comprises a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects. A main unit implements a normal mode function of the electronic circuit. A test unit tests the interconnects. The electronic circuit has a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit. In the test mode the test unit is operable as a low complexity memory via the I/O nodes.

**13 Claims, 3 Drawing Sheets**



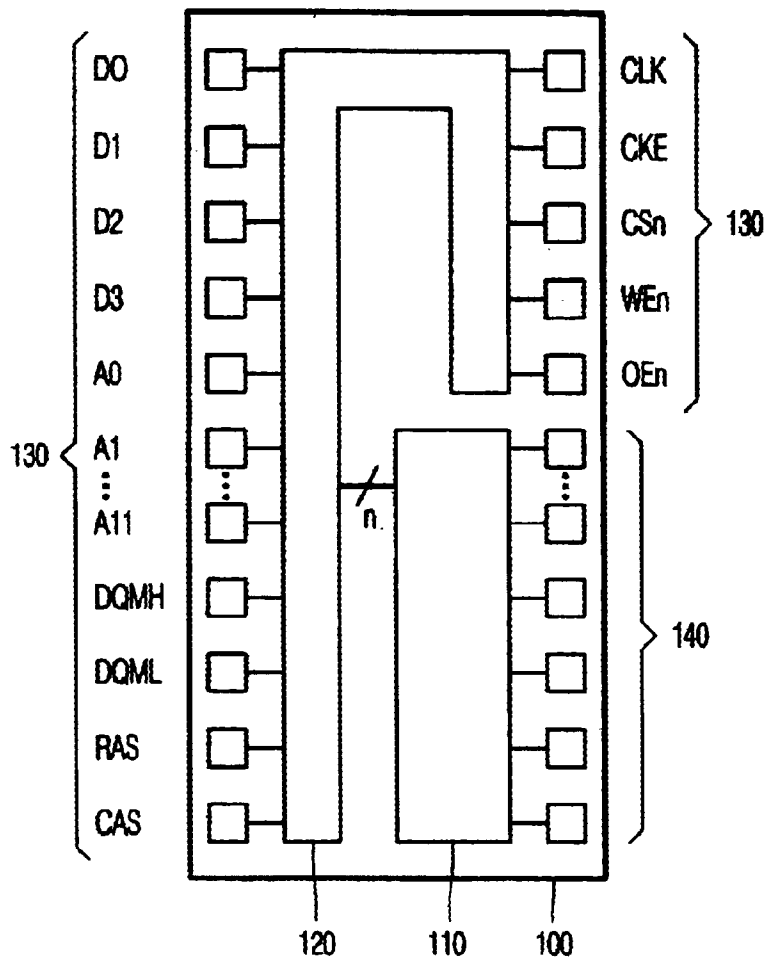


FIG. 1

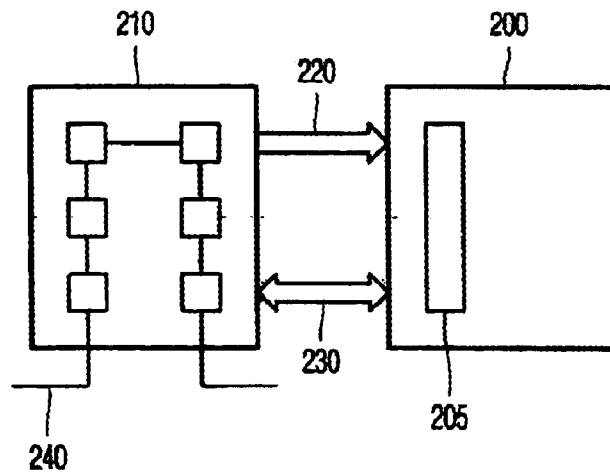


FIG. 2

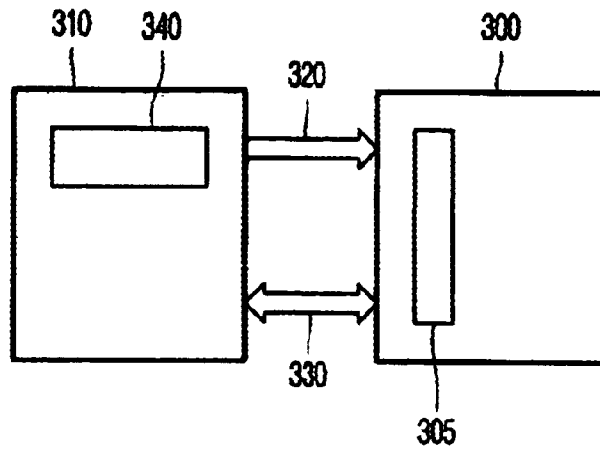


FIG. 3

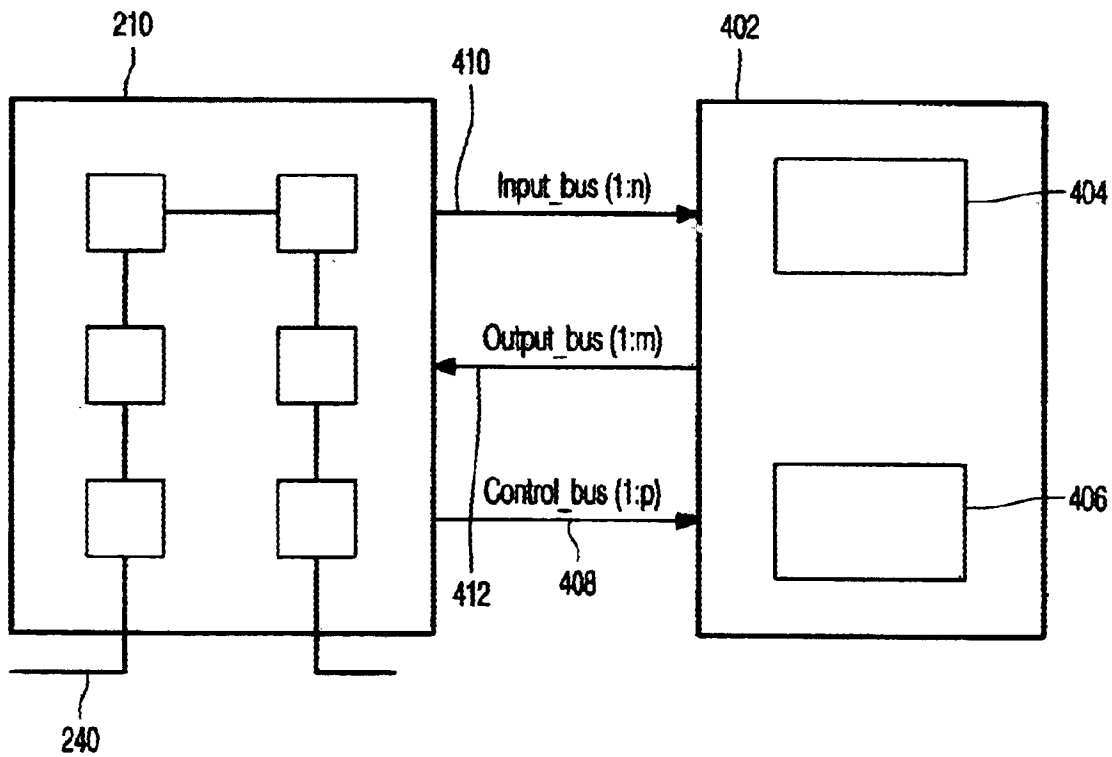


FIG. 4

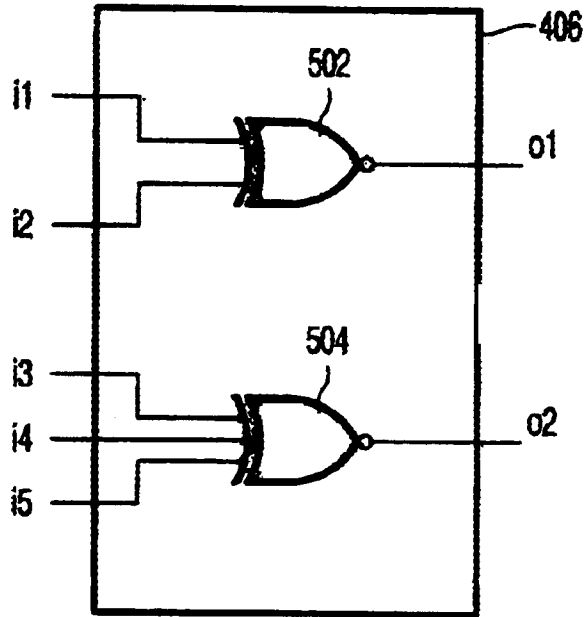


FIG. 5

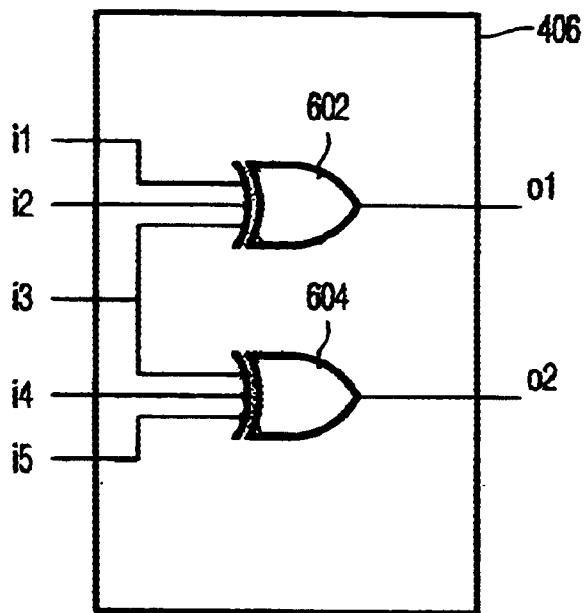


FIG. 6

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