

Exhibit 2

U.S. Patent No. 6,317,804 (“’804 Patent”)

Accused Products

Apple products incorporating Apple Ax processors (“Apple Ax System”) infringe at least Claim 1 of the

Claim 1

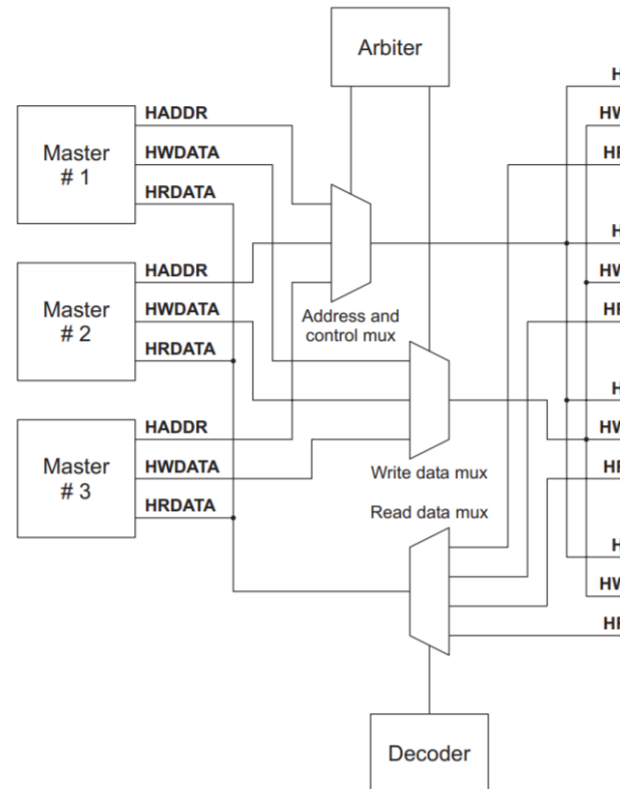
Claim 1	Apple Ax System
<p>1[pre]. A circuit arrangement for interfacing a plurality of functional blocks to one another in an integrated circuit device, the circuit arrangement comprising:</p>	<p>To the extent the preamble is limiting, the Apple Ax System comprises a circuit arrangement for interfacing a plurality of functional blocks to one another in an integrated circuit device.</p> <p>For example, the Apple Ax System comprises a circuit arrangement for interfacing a plurality of functional blocks to one another in an integrated circuit device, the circuit arrangement comprising:</p> <p>ARM AMBA (Advanced Microcontroller Bus Architecture) specification, including newer revisions.</p> <p><i>See, e.g.:</i></p> <p>1.1 Overview of the AMBA specification</p> <p>The <i>Advanced Microcontroller Bus Architecture (AMBA)</i> specification is a <u>chip communications standard</u> for designing high-performance microcontrollers.</p> <p>Three distinct buses are defined within the AMBA specification:</p> <ul style="list-style-type: none">• <u>the <i>Advanced High-performance Bus (AHB)</i></u>• the <i>Advanced System Bus (ASB)</i>• the <i>Advanced Peripheral Bus (APB)</i>. <p>1.1.1 Advanced High-performance Bus (AHB)</p> <p>The AMBA AHB is for high-performance, high clock frequency applications. The AHB acts as the high-performance system <i>backbone</i> for an efficient connection of processors, on-chip memories and other components. The AHB interfaces with low-power peripheral macrocell functions. The AHB ensures ease of use in an efficient design flow using synthesis techniques.</p>

Claim 1	Apple Ax System
	AMBA Specification, Rev. 2.0, May 13, 1999.

3.2 Bus interconnection

The AMBA AHB bus protocol is designed to be used with a central interconnection scheme. Using this scheme all bus masters drive control signals indicating the transfer they wish to perform and the decoder which master has its address and control signals routed to all of the slaves. A decoder is also required to control the read data and response signals. The decoder selects the appropriate signals from the slave that is involved in the transfer.

Figure 3-2 illustrates the structure required to implement an AMBA AHB bus with three masters and four slaves.



AMBA Specification, Rev. 2.0, May 13, 1999.

Claim 1	Apple Ax System
<p>1[a] a plurality of serial ports, each serial port associated with and coupled to a functional block via a point-to-point connection to permit external communication therewith, and each serial port including separate serial command, data and clock interconnects; and</p>	<p>The Apple Ax System comprises a plurality of serial ports, each serial port associated with and coupled to a functional block via a point-to-point connection to permit external communication therewith, and each serial port including separate serial command, data and clock interconnects.</p> <p>For example, the Apple Ax System comprises a plurality of serial ports, each serial port associated with the ARM Advanced High-Performance Bus, each of which is coupled to a functional block via a point-to-point connection to permit external communication therewith, and each serial port including separate serial command interconnects (for example and not by way of limitation, HWRITE, HTRANS, HSIZE, HPROT), data interconnects (for example and not by way of limitation, HRDATA), and clock interconnects (for example and not by way of limitation, HLOCK).</p> <p><i>See, e.g.:</i></p>

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