

EXHIBIT 7

United States Patent [19]

[11] **Patent Number:** **6,127,070**

Yang et al.

[45] **Date of Patent:** **Oct. 3, 2000**

[54] **THIN RESIST WITH NITRIDE HARD MASK FOR VIA ETCH APPLICATION**

FOREIGN PATENT DOCUMENTS

[75] Inventors: **Chih Yuh Yang**, San Jose; **Christopher F. Lyons**, Fremont; **Harry J. Levinson**, Saratoga; **Khanh B. Nguyen**, San Mateo; **Fei Wang**; **Scott A. Bell**, both of San Jose, all of Calif.

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[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

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Assistant Examiner—George Goudreau
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[21] Appl. No.: **09/203,283**

[22] Filed: **Dec. 1, 1998**

[57] **ABSTRACT**

[51] **Int. Cl.**⁷ **H01L 21/302**

[52] **U.S. Cl.** **430/5; 438/723; 438/724; 438/725; 438/692; 438/694; 438/700; 438/736**

[58] **Field of Search** **438/636, 723, 438/724, 725, 692, 694, 700, 736, 743, 744; 430/5**

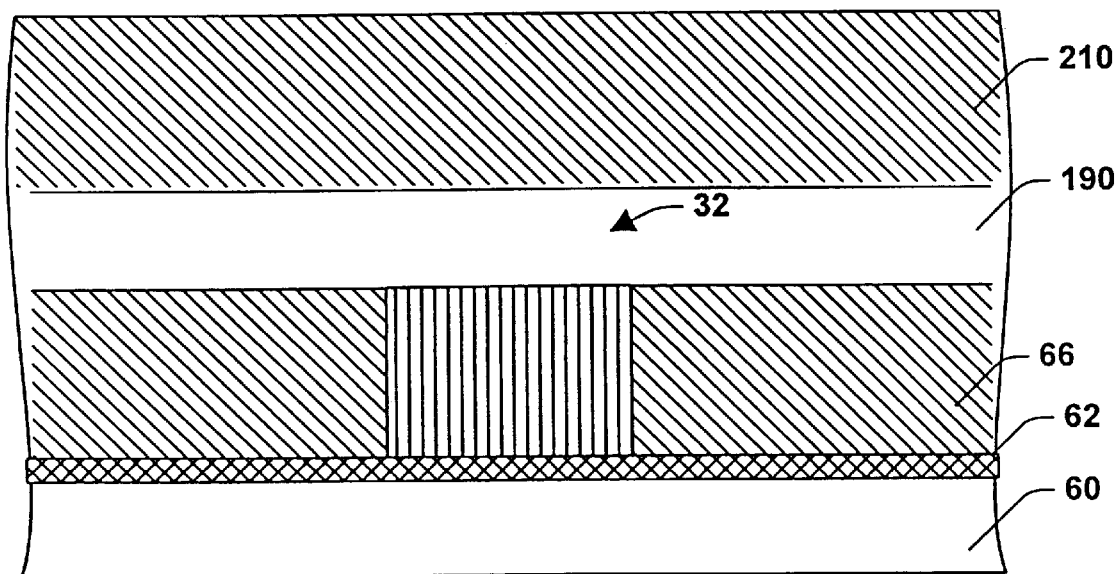
A method of forming a via structure is provided. In the method, a dielectric layer is formed on an anti-reflective coating (ARC) layer covering a first metal layer; and a nitride layer is formed on the dielectric layer. An ultra-thin photoresist layer is formed on the nitride layer, and the ultra-thin photoresist layer is patterned with short wavelength radiation to define a pattern for a via. The patterned ultra-thin photoresist layer is used as a mask during a first etch step to transfer the via pattern to the nitride layer. The first etch step includes an etch chemistry that is selective to the nitride layer over the ultra-thin photoresist layer and the dielectric layer. The nitride layer is employed as a hard mask during a second etch step to form a contact hole corresponding to the via pattern by etching portions of the dielectric layer.

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2 Claims, 9 Drawing Sheets



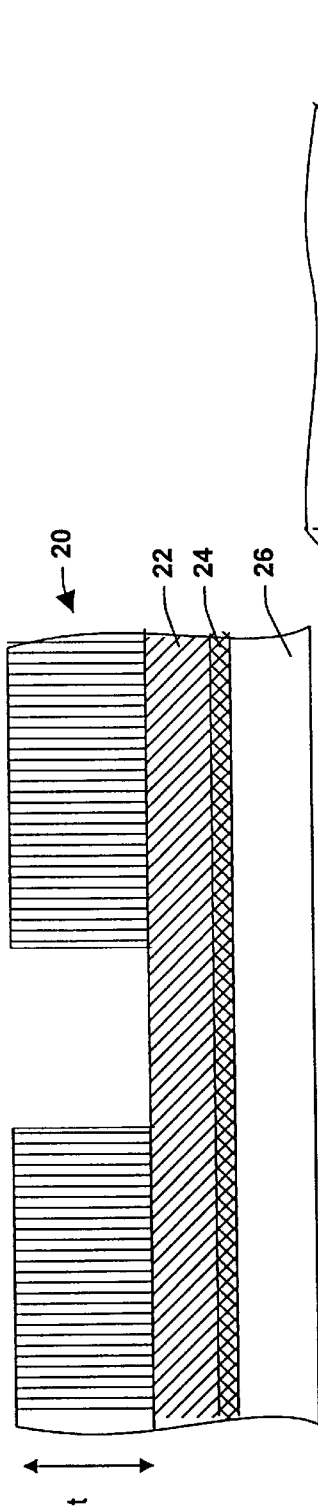


Fig. 1
Prior Art

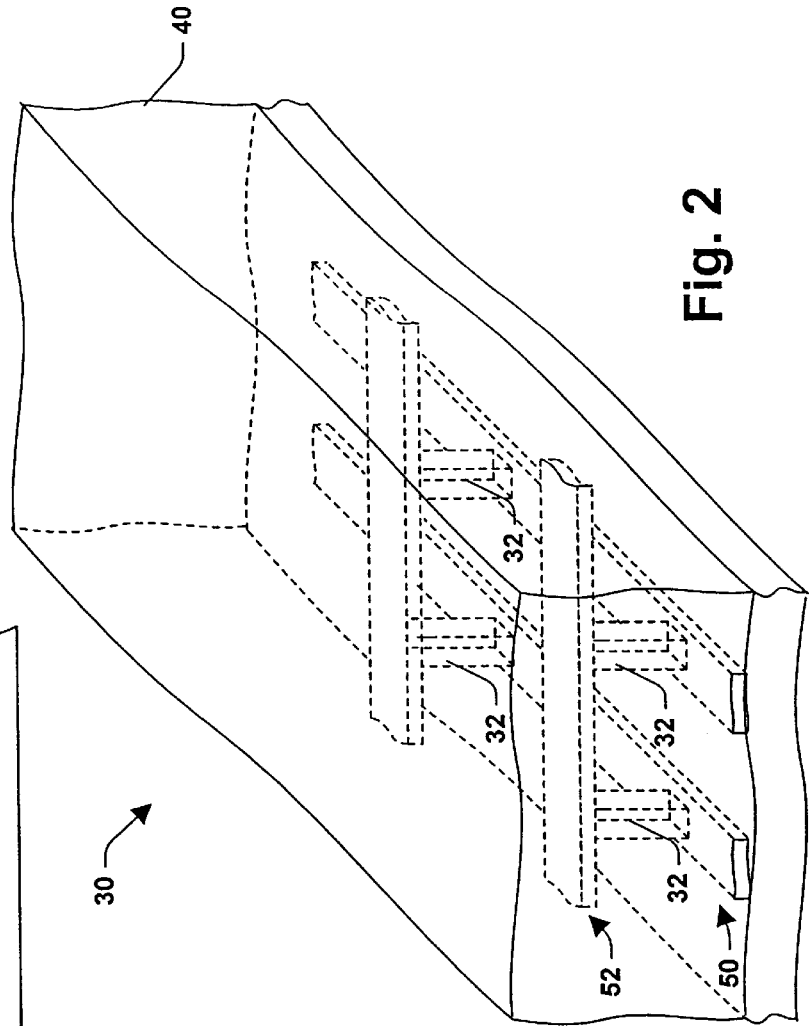


Fig. 2

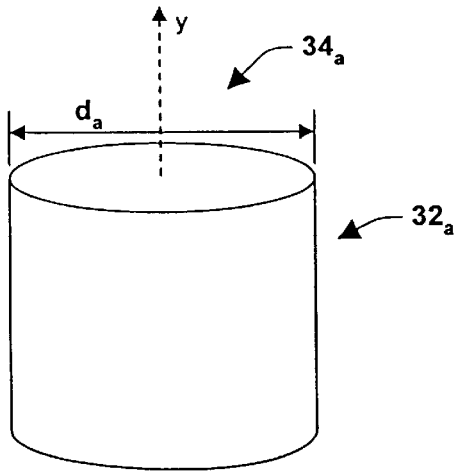


Fig. 3a

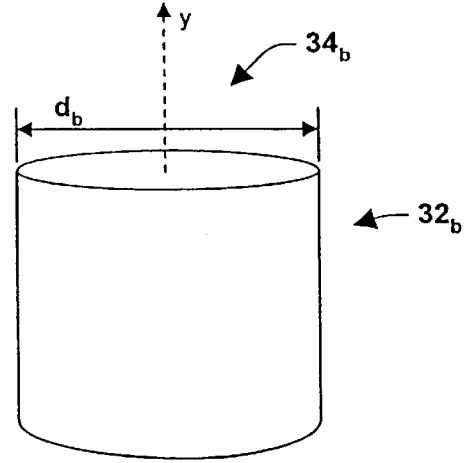


Fig. 3b

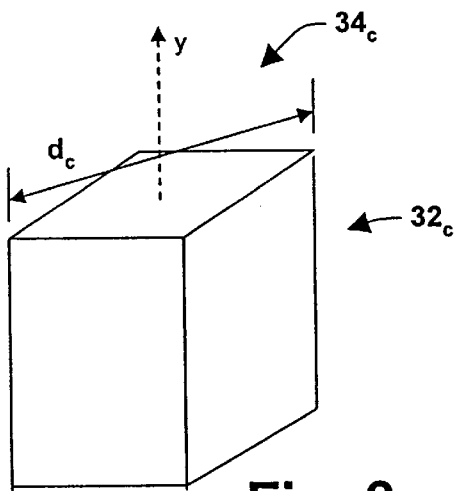


Fig. 3c

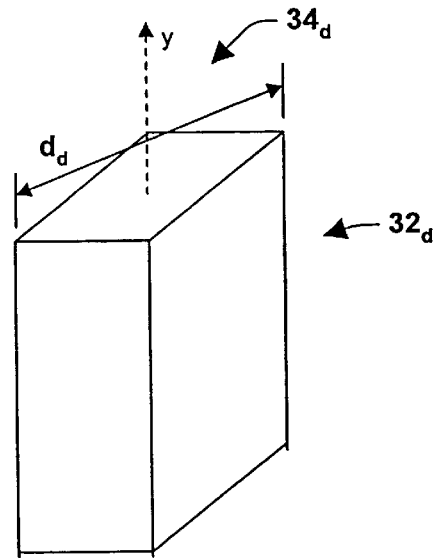


Fig. 3d

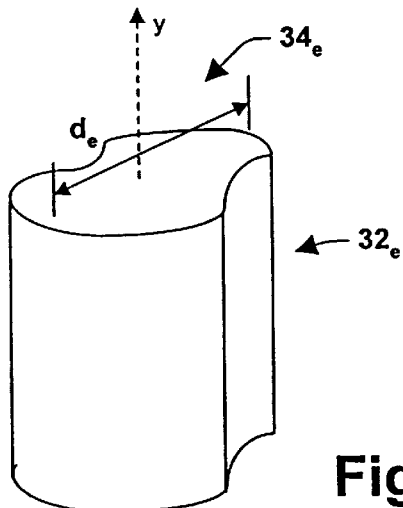


Fig. 3e

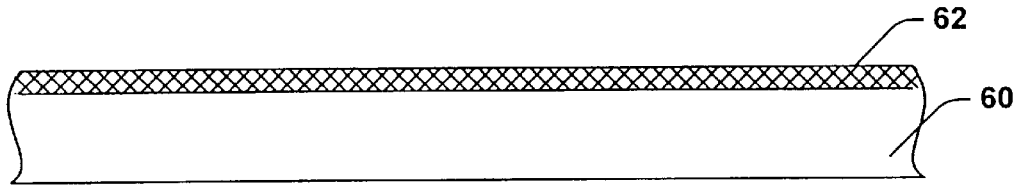


Fig. 4

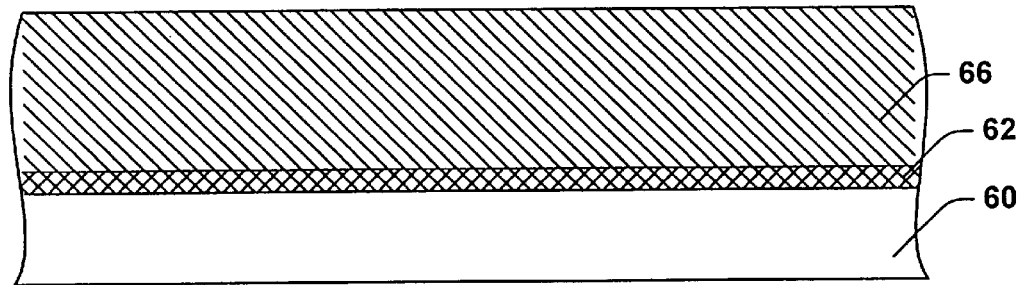


Fig. 5

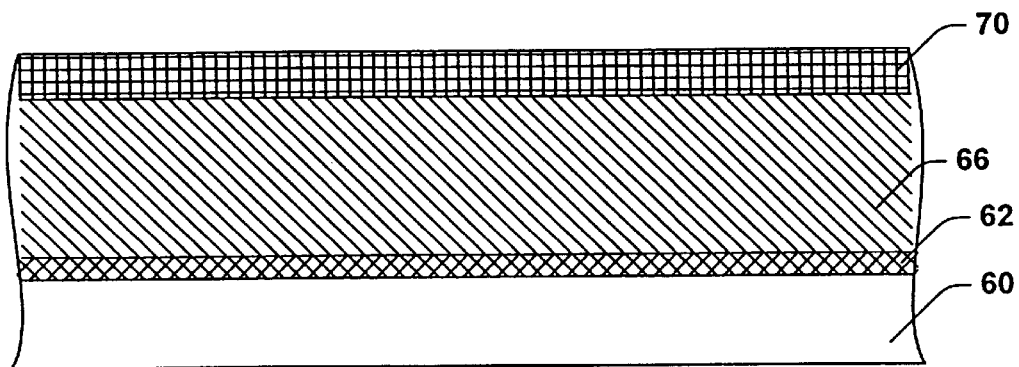


Fig. 6

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