

EXHIBIT 3



US007080330B1

(12) **United States Patent**
Choo et al.

(10) **Patent No.:** **US 7,080,330 B1**
 (45) **Date of Patent:** **Jul. 18, 2006**

(54) **CONCURRENT MEASUREMENT OF CRITICAL DIMENSION AND OVERLAY IN SEMICONDUCTOR MANUFACTURING**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 433 days.

(57) **ABSTRACT**

A system and methodology are disclosed for monitoring and controlling a semiconductor fabrication process. One or more structures formed on a wafer matriculating through the process facilitate concurrent measurement of critical dimensions and overlay via scatterometry or a scanning electron microscope (SEM). **The concurrent measurements mitigate fabrication inefficiencies, thereby reducing time and real estate required for the fabrication process.** The measurements can be utilized to generate feedback and/or feed-forward data to selectively control one or more fabrication components and/or operating parameters associated therewith to achieve desired critical dimensions and to mitigate overlay error.

(21) Appl. No.: **10/379,738**

(22) Filed: **Mar. 5, 2003**

(51) Int. Cl. **G06F 17/50** (2006.01)

(52) U.S. Cl. **716/4; 716/19; 716/21**

(58) Field of Classification Search **716/4, 716/19, 20, 21**

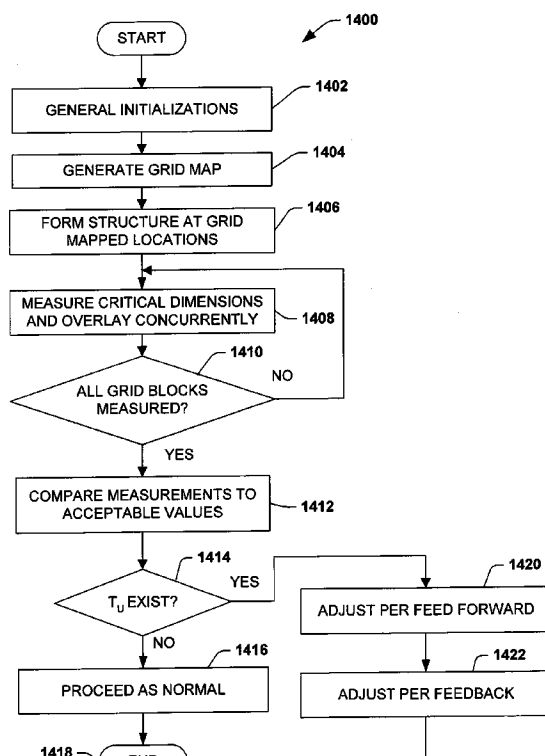
See application file for complete search history.

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25 Claims, 18 Drawing Sheets



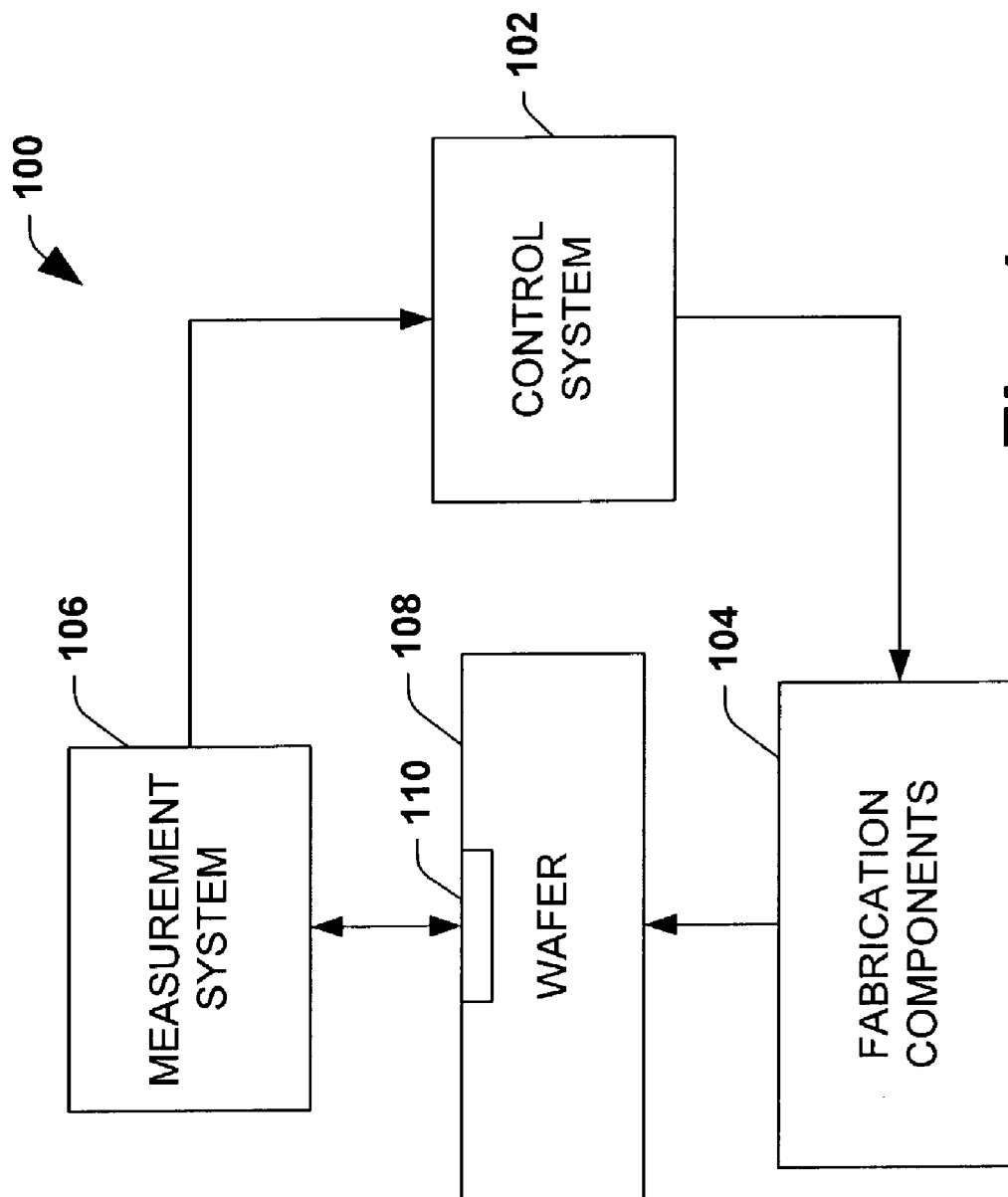


Fig. 1

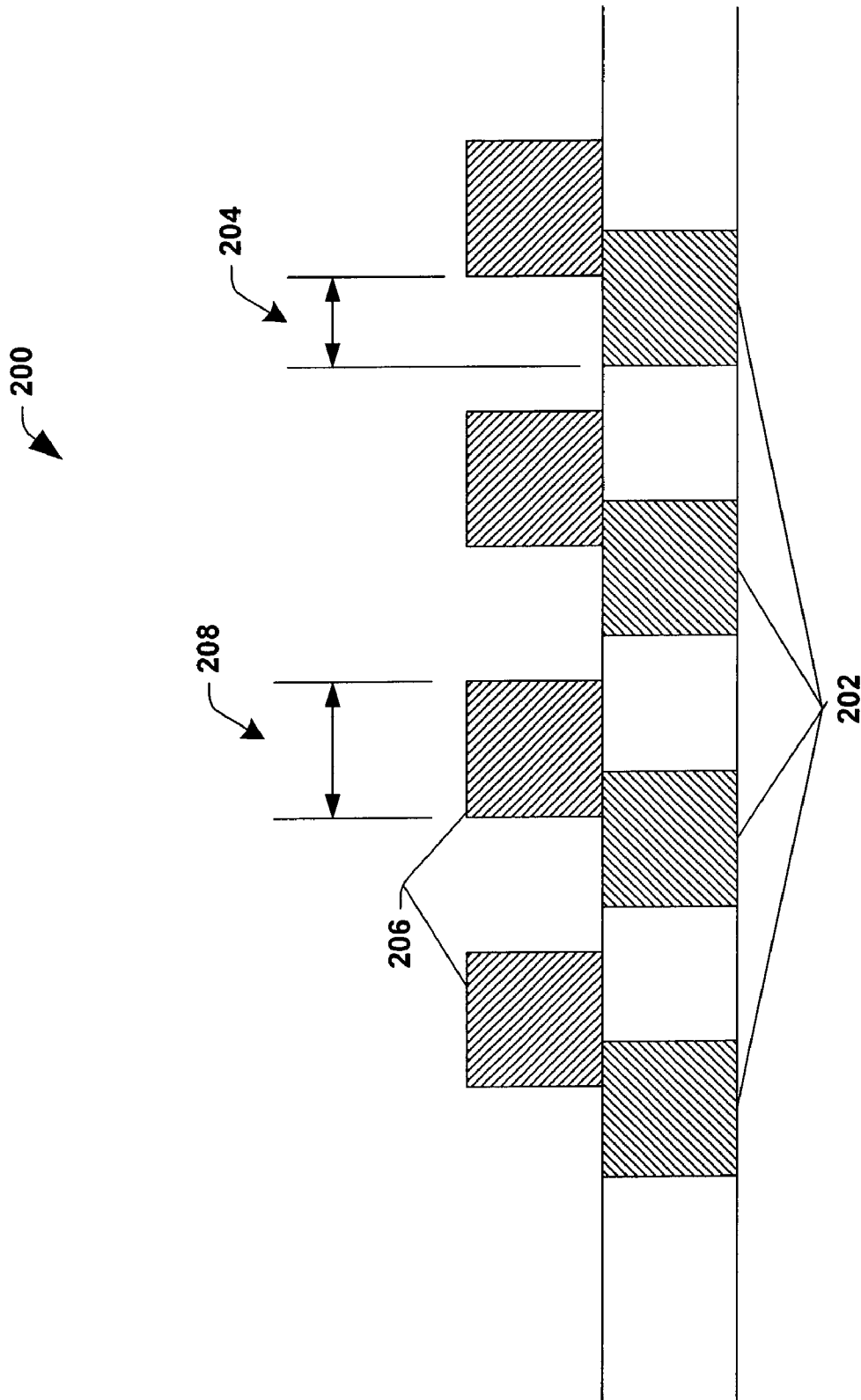


Fig. 2

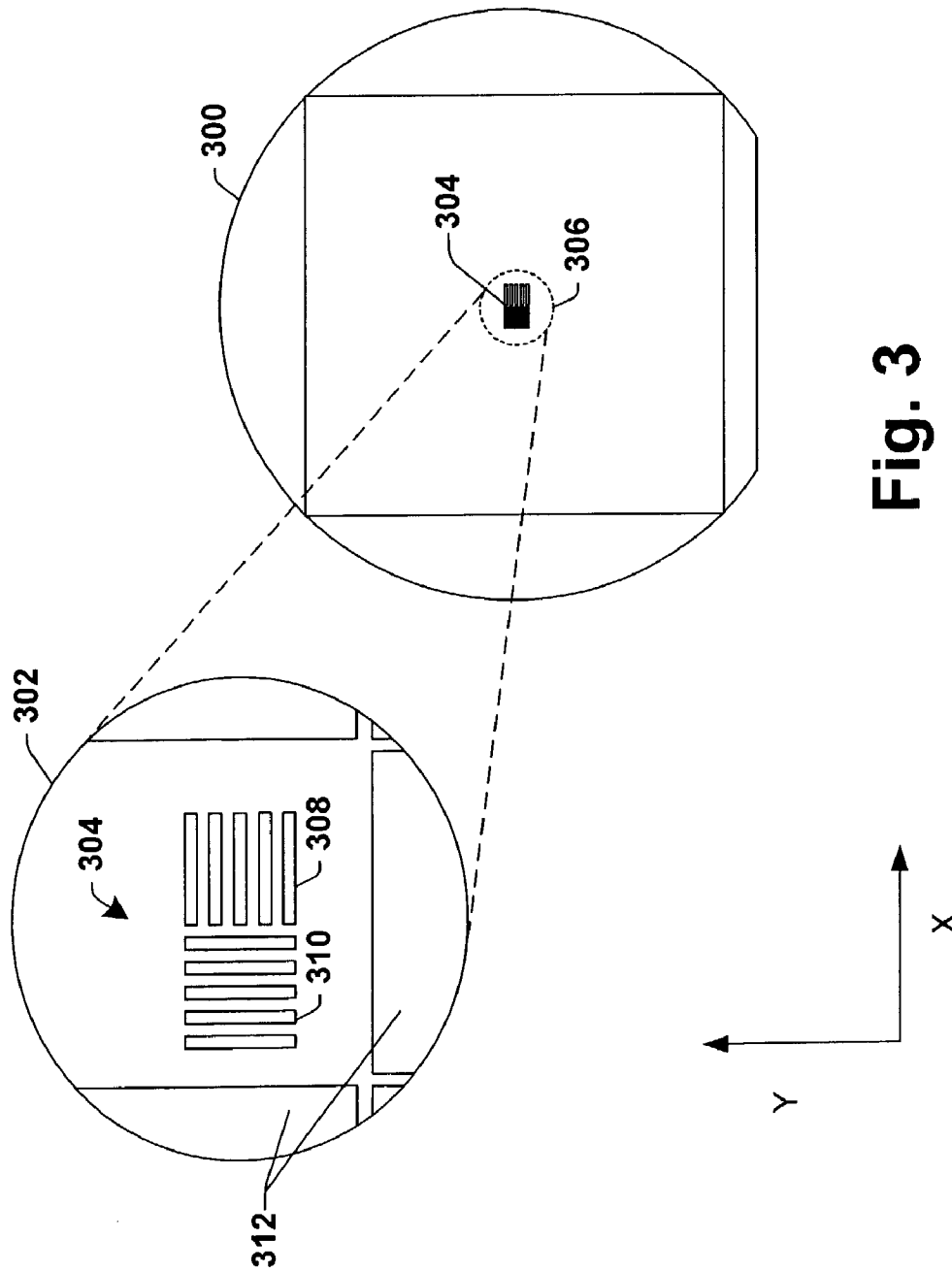


Fig. 3

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