EXHIBIT 17



(12) United States Patent Lyons et al.

(10) Patent No.: US 6,566,214 B1 (45) Date of Patent: May 20, 2003

(54)	METHOD OF MAKING A SEMICONDUCTOR
	DEVICE BY ANNEALING A METAL LAYER
	TO FORM METAL SILICIDE AND USING
	THE METAL SILICIDE AS A HARD MASK
	TO PATTERN A POLYSILICON LAYER

(34)	METHOD OF MAKING A SEMICONDUCTOR
	DEVICE BY ANNEALING A METAL LAYER
	TO FORM METAL SILICIDE AND USING
	THE METAL SILICIDE AS A HARD MASK
	TO PATTERN A POLYSILICON LAYER

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(*)	Notice:	Subject to any disclaimer, the term of this
. ,		patent is extended or adjusted under 35
		U.S.C. 154(b) by 0 days.

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(22)	Filed:	Jan. 17, 2002

(51)	Int. Cl. ⁷	H01L 21/3213; H01L 21/336
(52)	IIS CI	438/305· 438/592· 438/655·

		438/682; 438/683
(58)	Field of Search	438/301, 303,
` ′	438/306, 586, 593	2, 595, 648, 649, 655,
		682, 683, 305

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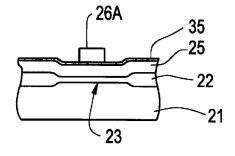
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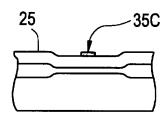
Primary Examiner—Carl Whitehead, Jr. Assistant Examiner-Stephen W. Smoot (74) Attorney, Agent, or Firm-Foley & Lardner

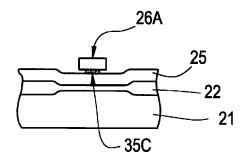
ABSTRACT

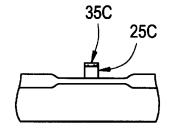
A method of making a semiconductor device is provided. A polysilicon layer is formed over a substrate and a metal layer is formed on the polysilicon layer. The metal layer and the polysilicon layer are annealed to form a metal silicide layer on the polysilicon layer. The metal silicide layer is patterned and the polysilicon layer is then patterned using the patterned metal silicide layer as a mask. The patterned metal silicide and polysilicon layers may be used as a gate electrode of a MOSFET.

28 Claims, 5 Drawing Sheets











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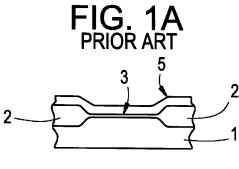


FIG. 1B PRIOR ART

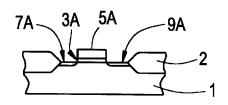


FIG. 1C PRIOR ART

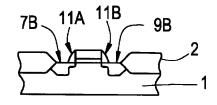


FIG. 1D PRIOR ART

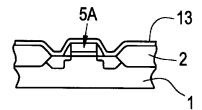
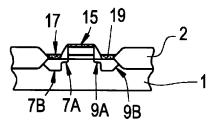


FIG. 1E PRIOR ART



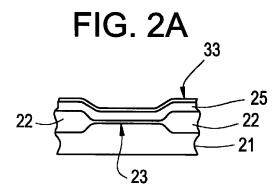


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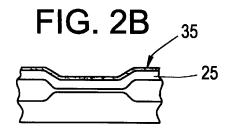


FIG. 2C

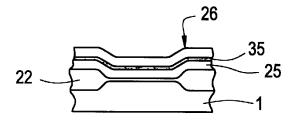


FIG. 2D

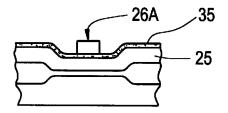
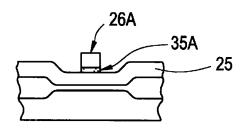


FIG. 2E





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FIG. 2F

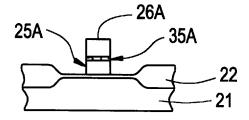


FIG. 2G

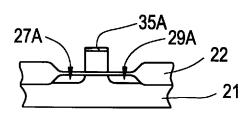


FIG. 2H

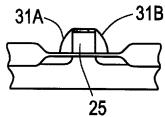


FIG. 21

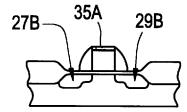
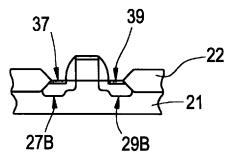


FIG. 2J





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