EXHIBIT 15

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Rangarajan et al.

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(54) **UV-ENHANCED SILYLATION PROCESS TO INCREASE ETCH RESISTANCE OF ULTRA THIN RESISTS**

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(52) **U.S. Cl.** **430/313**; 430/296; 430/328
(58) **Field of Search** 430/296, 311, 430/313, 315, 323, 324, 325, 328

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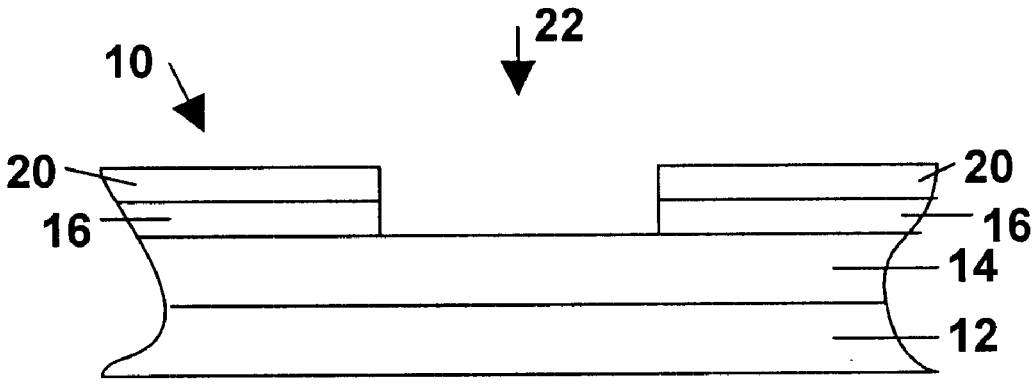
(57) **ABSTRACT**

In one embodiment, the present invention relates to a method of processing an ultrathin resist, involving the steps of depositing the ultra-thin photoresist over a semiconductor substrate, the ultra-thin resist having a thickness less than about 3,000 Å; irradiating the ultra-thin resist with electromagnetic radiation having a wavelength of about 250 nm or less; developing the ultra-thin resist; and contacting the ultra-thin resist with a silicon containing compound in an environment of at least one of ultraviolet light and ozone, wherein contact of the ultra-thin resist with the silicon containing compound is conducted between irradiating and developing the ultra-thin resist or after developing the ultra-thin resist.

19 Claims, 2 Drawing Sheets



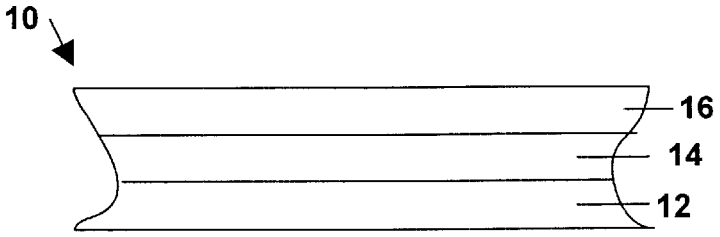


Fig. 1

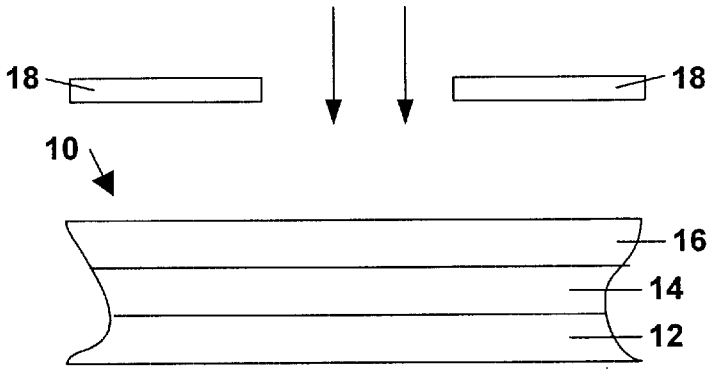


Fig. 2

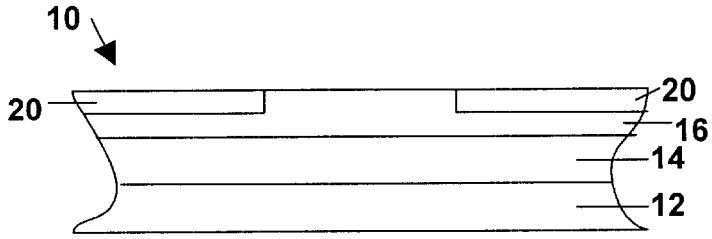


Fig. 3

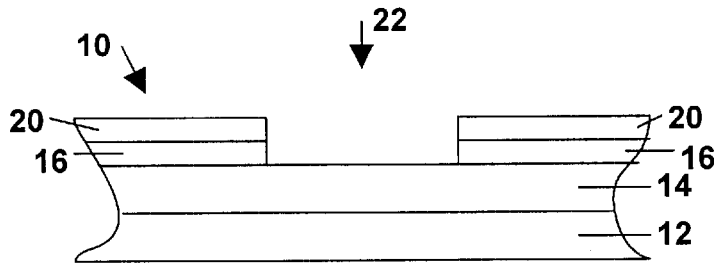


Fig. 4

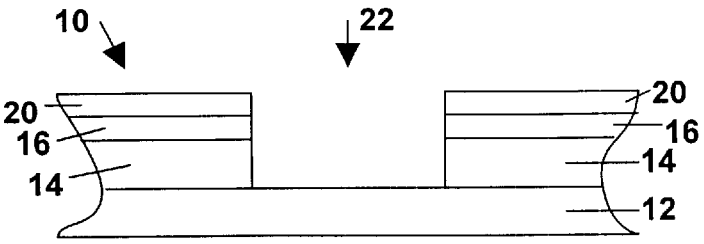


Fig. 5

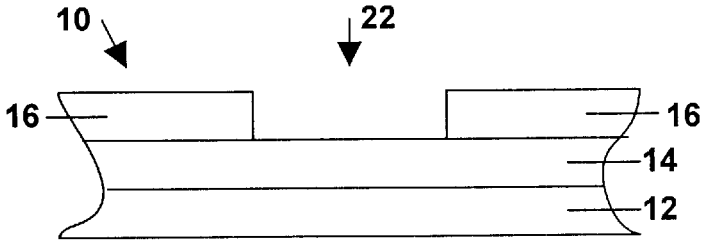


Fig. 6

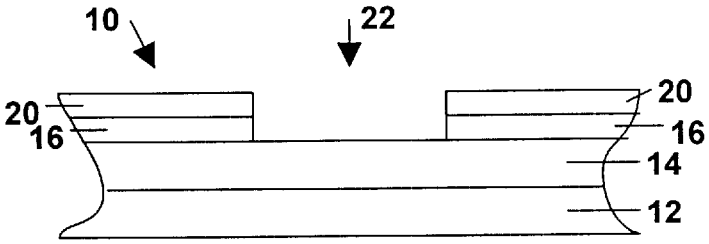


Fig. 7

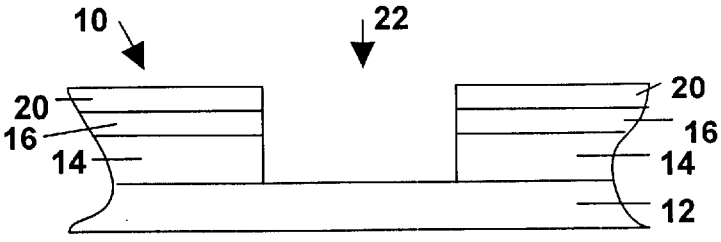


Fig. 8

UV-ENHANCED SILYLATION PROCESS TO INCREASE ETCH RESISTANCE OF ULTRA THIN RESISTS

TECHNICAL FIELD

The present invention generally relates to increasing the etch resistance of an ultra-thin resist. In particular, the present invention relates to silylating an ultra-thin resist which in turn increases its etch resistance.

BACKGROUND ART

In the semiconductor industry, there is a continuing trend toward higher device densities. To achieve these high densities, there has been and continues to be efforts toward scaling down the device dimensions on semiconductor wafers. In order to accomplish such high device packing density, smaller and smaller features sizes are required. This includes the width and spacing of interconnecting lines and the surface geometry such as corners and edges of various features. Since numerous interconnecting lines are typically present on a semiconductor wafer, the trend toward higher device densities is a notable concern.

The requirement of small features, such as metal lines, with close spacing between adjacent features requires high resolution photolithographic processes. In general, lithography refers to processes for pattern transfer between various media. It is a technique used for integrated circuit fabrication in which a silicon slice, the wafer, is coated uniformly with a radiation-sensitive film, the resist, and an exposing source (such as optical light, X-rays, or an electron beam) illuminates selected areas of the surface through an intervening master template, the photomask, for a particular pattern. The lithographic coating is generally a radiation-sensitized coating suitable for receiving a projected image of the subject pattern. Once the image is projected, it is indelibly formed in the coating. The projected image may be either a negative or a positive of the subject pattern. Exposure of the coating through the photomask causes a chemical transformation in the exposed areas of the coating thereby making the image area either more or less soluble (depending on the coating) in a particular solvent developer. The more soluble areas are removed in the developing process to leave the pattern image in the coating as less soluble polymer.

Projection lithography is a powerful and essential tool for microelectronics processing. However, lithography is not without limitations. Patterning features having dimensions of about 0.25 μm, 0.18 μm or less with acceptable resolution is difficult. This is because photoresist layers used in lithography typically have thicknesses on the order of 7,000 Å and higher. Such relatively thick photoresist layers are not conducive to making small patterned dimensions with good resolution.

Using relatively thin photoresists (such as less than about 5,000 Å) enables the patterning of smaller and smaller dimensions. However, insufficient etch protection during semiconductor processing is associated with using thin photoresists. The relatively thin patterned photoresists simply do not protect underlying surfaces during etch steps. For example, corner rounding of layers underneath relatively thin photoresists is caused by insufficient etch protection and results in poor definition/resolution. In many instances the relatively thin patterned photoresists are removed during an etch procedure. As a result, it is often necessary to employ the use of hardmasks when using thin photoresists in subtractive semiconductor processing techniques. Improved lithography procedures providing improved resolution and improved etch resistance are therefore desired.

SUMMARY OF THE INVENTION

The present invention generally provides methods that lead to improved etch resistance, improved critical dimension control and/or improved resolution in patterned ultra-thin resists. Since it is possible to enhance the etch resistance of ultra-thin photoresists, the present invention provides improved methods for etching layers underneath patterned ultra-thin photoresists including metal layers. The methods of the present invention make it possible to etch trenches, holes and other openings on the order of about 0.18 μm or less in size. The methods of the present invention also make it possible to avoid the use of hardmasks when using ultra-thin photoresists. As a result, the present invention effectively addresses the concerns raised by the trend towards the miniaturization of semiconductor devices.

In one embodiment, the present invention relates to a method of processing an ultra-thin resist, involving the steps of depositing the ultra-thin photoresist over a semiconductor substrate, the ultra-thin resist having a thickness less than about 3,000 Å; irradiating the ultra-thin resist with electromagnetic radiation having a wavelength of about 250 nm or less; developing the ultra-thin resist; and contacting the ultra-thin resist with a silicon containing compound in an environment of at least one of ultraviolet light and ozone, wherein contact of the ultra-thin resist with the silicon containing compound is conducted between irradiating and developing the ultra-thin resist or after developing the ultra-thin resist.

In another embodiment, the present invention relates to a method of increasing the etch resistance of an ultra-thin resist, involving the steps of irradiating the ultra-thin resist with electromagnetic radiation having a wavelength of about 250 nm or less, the ultra-thin resist having a thickness less than about 3,000 Å; developing the ultra-thin resist; and contacting the ultra-thin resist with a silicon containing compound to incorporate silicon atoms into the ultra-thin resist in at least one of under ultraviolet light and in an atmosphere comprising at least about 5% by weight ozone, wherein contact of the ultra-thin resist with the silicon containing compound is conducted between irradiating and developing the ultra-thin resist or after developing the ultra-thin resist.

In yet another embodiment, the present invention relates to a method of patterning a semiconductor layer on a semiconductor substrate, involving the steps of depositing an ultra-thin photoresist over the semiconductor layer, the ultra-thin resist having a thickness less than about 3,000 Å; irradiating the ultra-thin resist with electromagnetic radiation having a wavelength of about 250 nm or less; developing the ultra-thin resist thereby exposing a portion of the semiconductor layer through an opening in the ultra-thin resist; contacting the ultra-thin resist with a silicon containing compound in an environment of at least one of ultraviolet light and ozone, wherein contact of the ultra-thin resist with the silicon containing compound is conducted between irradiating and developing the ultra-thin resist or after developing the ultra-thin resist; and etching the exposed portion of the semiconductor layer thereby patterning the semiconductor layer.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1** illustrates in a cross-sectional view of a method according to one aspect of the present invention.

FIG. **2** illustrates in a cross-sectional view of a method according to one aspect of the present invention.

FIG. **3** illustrates in a cross-sectional view of a method according to one aspect of the present invention.

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