EXHIBIT 11

US006165695A

United States Patent [19]

Yang et al.

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[45] **Date of Patent:** **Dec. 26, 2000**

[54] **THIN RESIST WITH AMORPHOUS SILICON HARD MASK FOR VIA ETCH APPLICATION**

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[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **09/203,150**

[22] Filed: **Dec. 1, 1998**

[51] **Int. Cl.**^{7} **G03C 5/00**

[52] **U.S. Cl.** **430/314**; 430/316; 430/317; 430/967

[58] **Field of Search** 430/311, 313, 430/316, 314, 317, 967; 438/423, 424; 216/39, 47, 72

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[57] **ABSTRACT**

A method of forming a via structure is provided. In the method, a dielectric layer is formed on an anti-reflective coating (ARC) layer covering a first metal layer; and an amorphous silicon layer is formed on the dielectric layer. An ultra-thin photoresist layer is formed on the amorphous silicon layer, and the ultra-thin photoresist layer is patterned with short wavelength radiation to define a pattern for a via. The patterned ultra-thin photoresist layer is used as a mask during a first etch step to transfer the via pattern to the amorphous silicon layer. The first etch step includes an etch chemistry that is selective to the amorphous silicon layer over the ultra-thin photoresist layer and the dielectric layer. The amorphous silicon layer is employed as a hard mask during a second etch step to form a contact hole corresponding to the via pattern by etching portions of the dielectric layer.

32 Claims, 9 Drawing Sheets
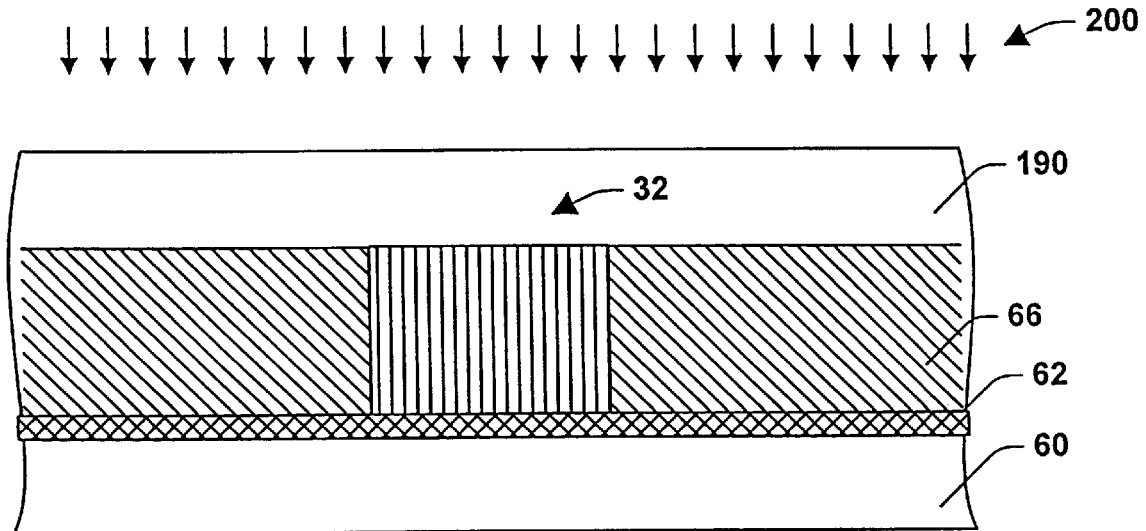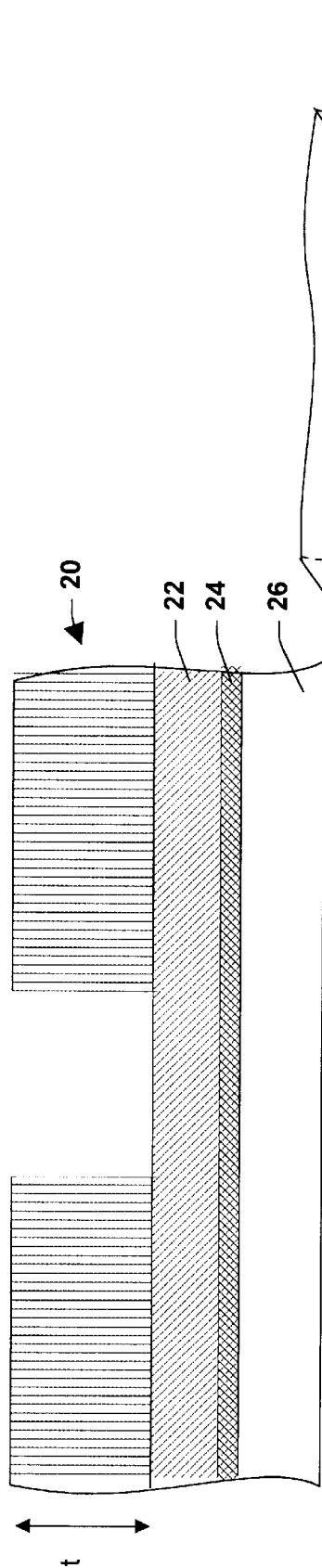
Fig. 2

Fig. 1
Prior Art
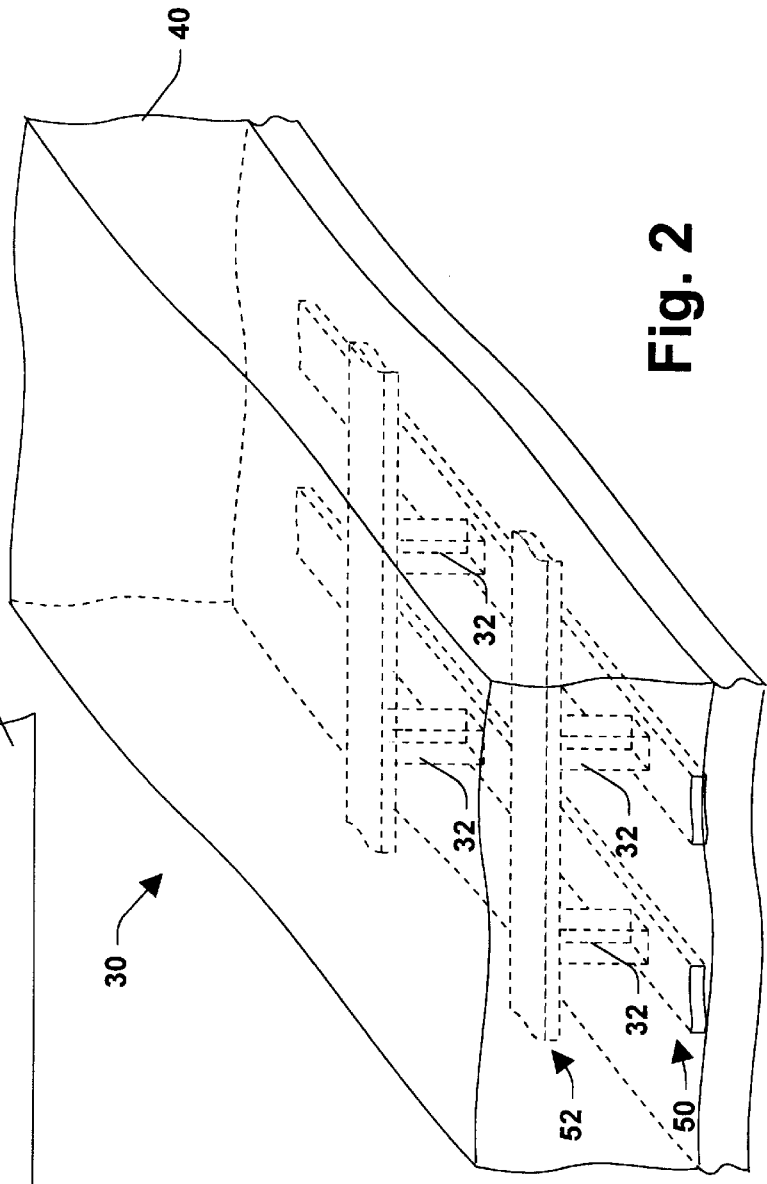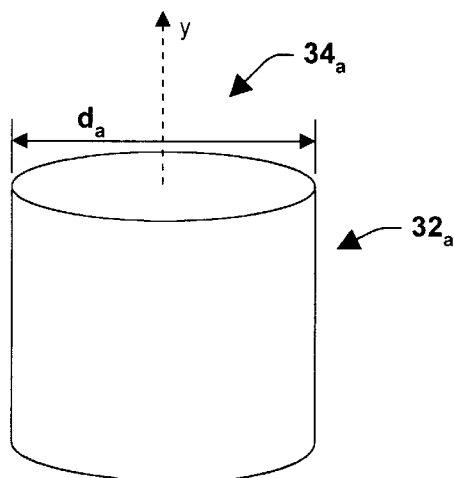
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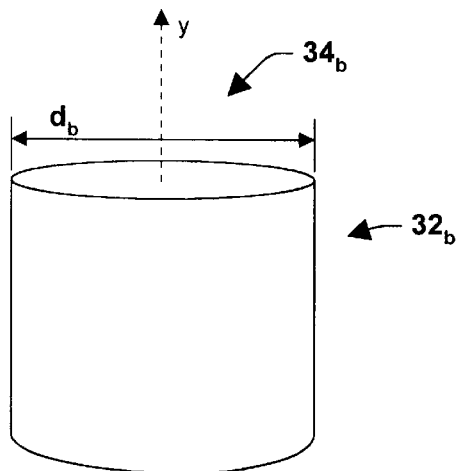
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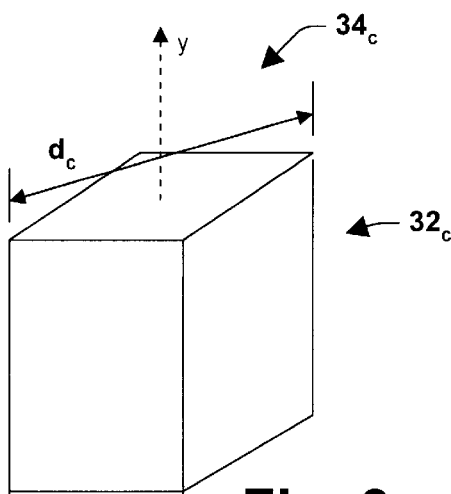
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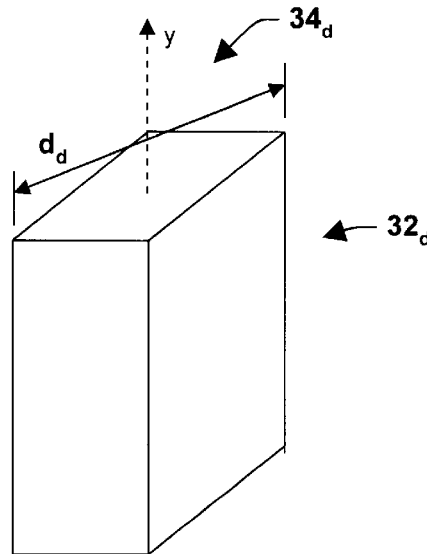
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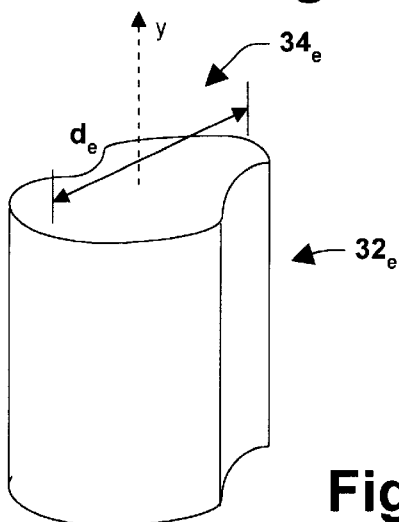
Fig. 3e

Fig. 4

Fig. 5

Fig. 6

DOCKET ALARM
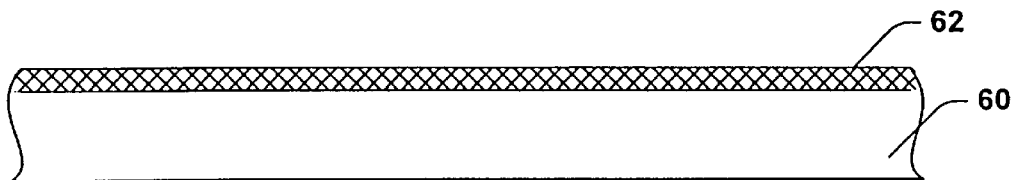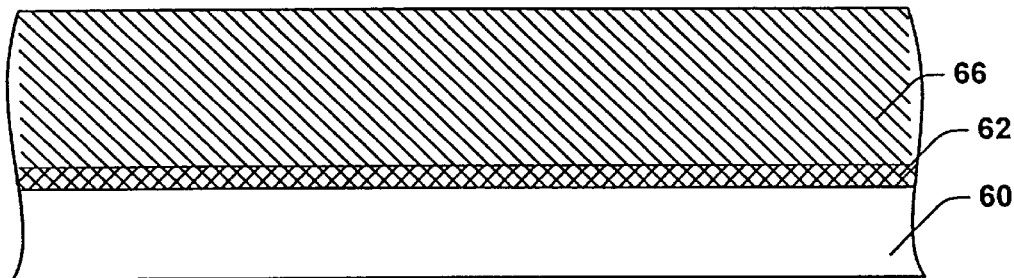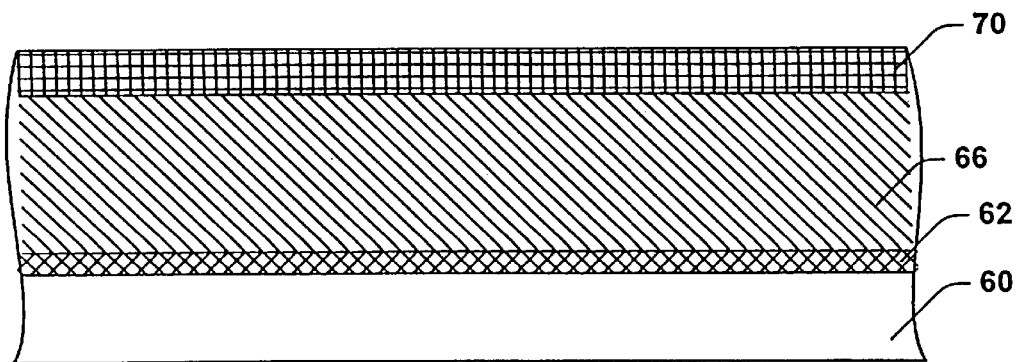
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