

EXHIBIT 1

(12) **United States Patent**
Pike et al.

(10) **Patent No.:** **US 6,420,097 B1**
(45) **Date of Patent:** **Jul. 16, 2002**

- (54) **HARDMASK TRIM PROCESS**
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- (73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)
- (*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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- (21) Appl. No.: **09/562,659**
- (22) Filed: **May 2, 2000**
- (51) **Int. Cl.⁷** **G03F 7/36**
- (52) **U.S. Cl.** **430/313; 430/317; 430/322; 430/328**
- (58) **Field of Search** **430/313, 317, 430/322, 328**

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Assistant Examiner—Amanda C. Walke
(74) *Attorney, Agent, or Firm*—Davis Chin

(57) **ABSTRACT**

An improved method of forming circuit structures having linewidths which are smaller than what is achievable by conventional UV lithographic techniques on ultra-thin resist layers is provided. The method includes a hardmask which is patterned using an ultra-thin resist layer and is then trimmed to reduce the width of the hardmask before etching the underlying gate conductive layer.

- (56) **References Cited**
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17 Claims, 3 Drawing Sheets

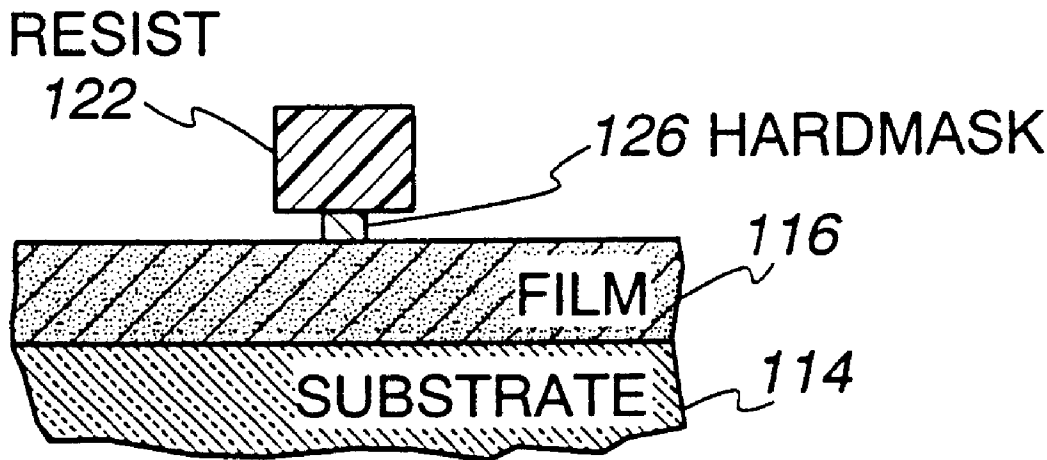


Fig. 1a
(Prior Art)

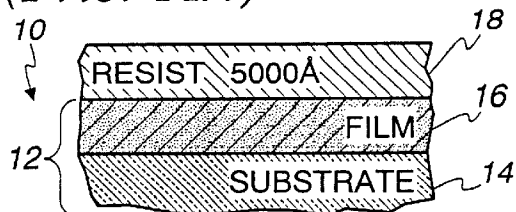


Fig. 2a
(Prior Art)

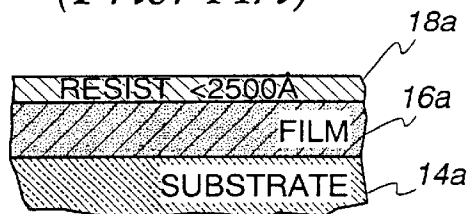


Fig. 1b
(Prior Art)

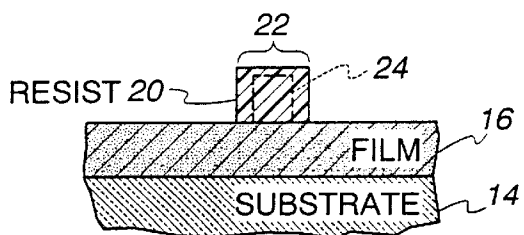


Fig. 2b
(Prior Art)

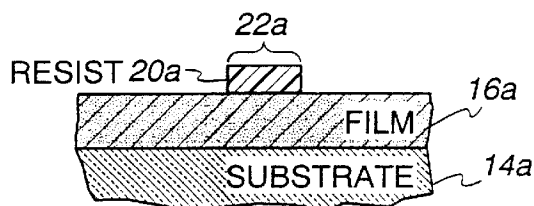


Fig. 1c
(Prior Art)

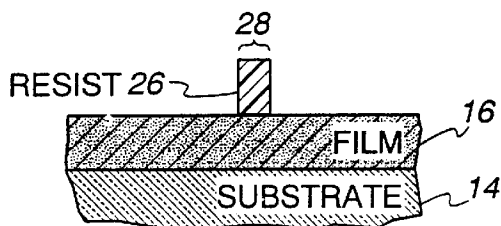


Fig. 2c
(Prior Art)

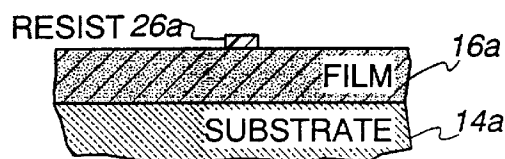


Fig. 1d
(Prior Art)

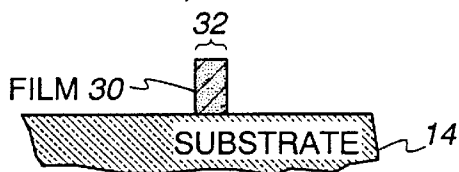


Fig. 2d
(Prior Art)

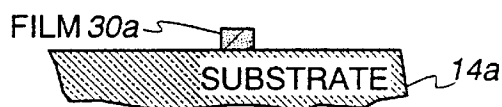


Fig. 3

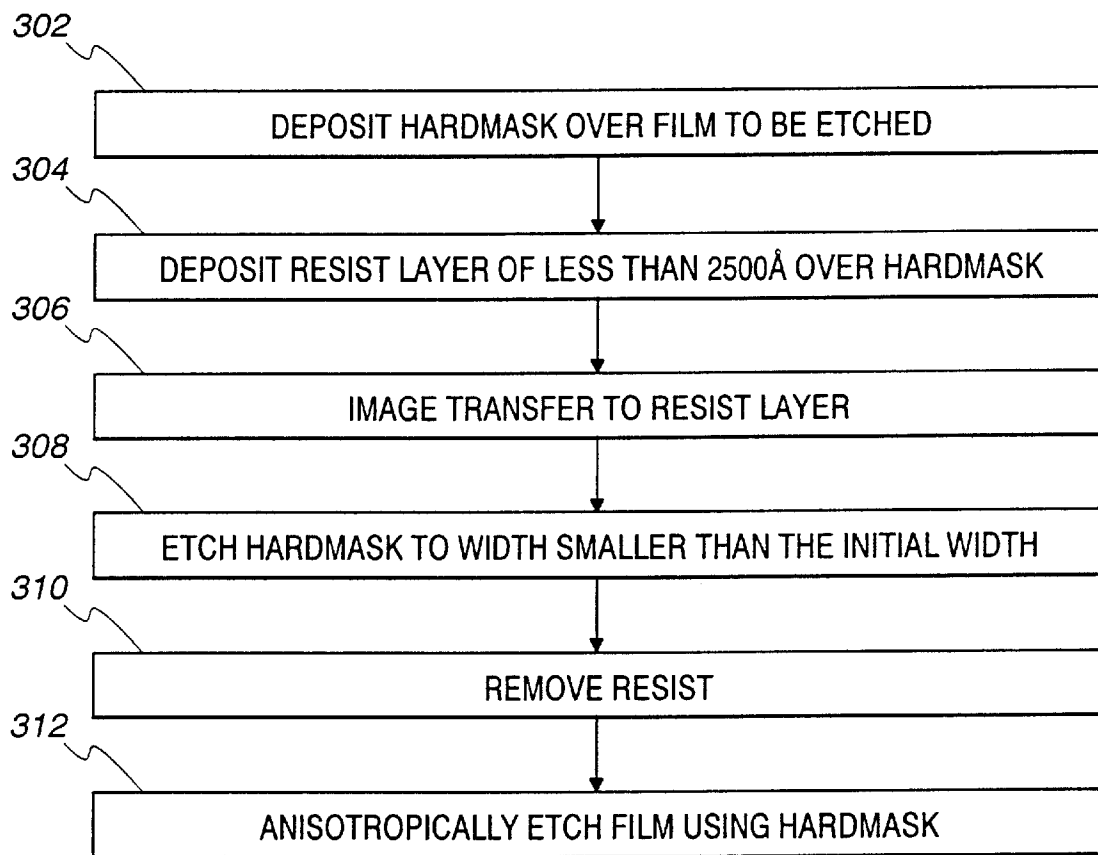


Fig. 4a

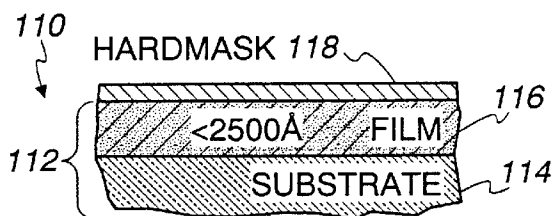


Fig. 4e

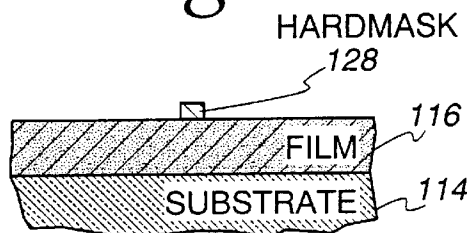


Fig. 4b

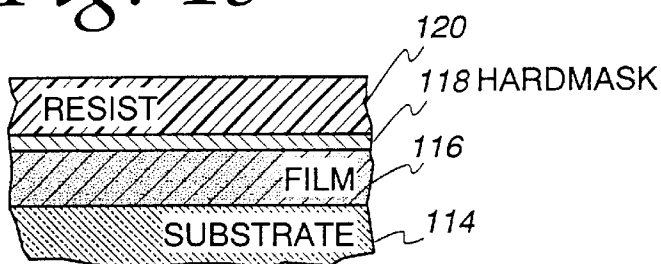


Fig. 4f

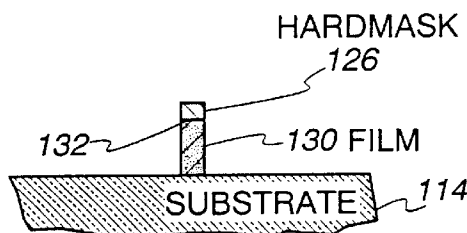


Fig. 4c

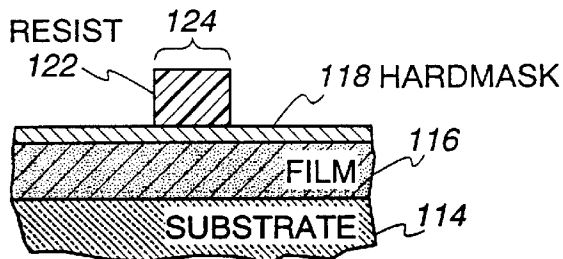
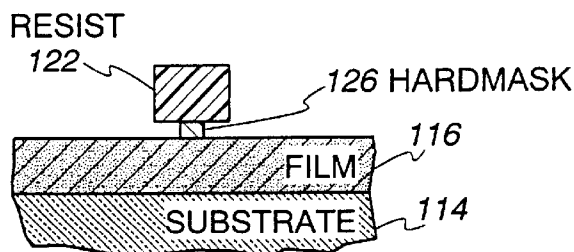


Fig. 4d



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