

EXHIBIT

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IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

PARKERVISION, INC.,
Plaintiff

-v-

INTEL CORPORATION,
Defendant

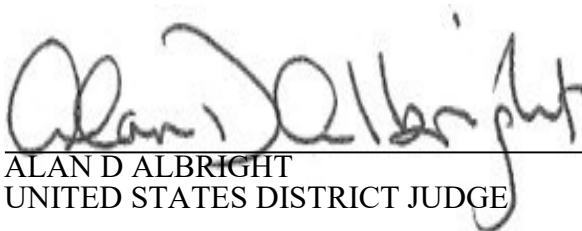
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W-20-CV-00562-ADA

CLAIM CONSTRUCTION ORDER

The Court held a *Markman* hearing on June 24, 2021 and July 22, 2021 . During those hearings, the Court provided its final constructions. The Court now enters those claim constructions.

SIGNED this 22nd day of July, 2021.


ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE

Term	Plaintiff’s Proposed Construction	Defendants’ Proposed Construction	Court’s
“under-sample” / “undersamples” / “under-sampling” ’706 patent, claims 1, 6, 7, 28, 34	“sampling at an aliasing rate” or “sampling at less than or equal to twice the frequency of the input signal”	“sample[s/ing] at less than or equal to twice the frequency of the input signal using negligible apertures (i.e., pulse widths) that tend towards zero time in duration”	“sampling or “sample equal to tw the input s
“storage module” ’706 patent, claims 105, 114, 164, 175, 179, 186, 190	“a module of an energy transfer system that stores non-negligible amounts of energy from an input electromagnetic signal for driving a low impedance load”	“a module that stores a non-negligible amount of energy from an input electromagnetic (EM) signal”	“a module transfer sy non-neglig energy fro electroma driving a
“switch” ’706 patent, claims 105, 164, 175, 186; ’108 patent, claim 1	“an electronic device for opening and closing a circuit as dictated by an independent control input”	“an electronic device for opening and closing a circuit”	Plain-and- wherein th meaning is device for a circuit as independe

Term	Plaintiff’s Proposed Construction	Defendants’ Proposed Construction	Court’s
<p>“a down-convert and delay module to under-sample an input signal to produce an input sample of a down-converted image of said input signal, and to delay said input sample”</p> <p>’706 patent, claims 1, 7</p>	<p>Plain and ordinary meaning</p>	<p>Function: under-sample an input signal according to a control signal to produce an input sample of a down-converted image of said input signal, and to delay said input sample</p> <p>Structure: the down convert and delay module 2624 in Fig. 26 and described at 26:1-27:21 and 28:2041, that includes the switches 2650 and 2654, and the capacitors 2652 and 2656; and equivalents thereof</p>	<p>Not subject to plain-and-ordinary meaning</p>
<p>“a frequency translator to produce a sample of a down-converted image of an input signal, and to delay said sample”</p> <p>’706 patent, claim 34</p>	<p>Plain and ordinary meaning</p>	<p>Function: produce a sample of a down-converted image of an input signal according to a control signal, and to delay said sample</p> <p>Structure: the down convert and delay module 2624 in Fig. 26 and described at 26:1-27:21 and 28:2041, that includes the switches 2650 and 2654, and the capacitors 2652 and 2656; and equivalents thereof.</p>	<p>Not subject to plain-and-ordinary meaning</p>

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's
<p>“said input sample”, “said sample”</p> <p>'706 patent, claims 1, 6, 7, 34</p>	<p>Plain and ordinary meaning</p>	<p>“the sample of the image that has been down-converted”</p>	<p>Plain-and-</p>
<p>“delay module to delay instances of an output signal”, “delay modules to further delay one or more of said delayed and down-converted input samples”</p> <p>'706 patent, claims 1, 7, 34, 140</p>	<p>Plain and ordinary meaning</p>	<p>Function: delay instances of an output signal / further delay one or more of said delayed and downconverted input samples</p> <p>Structure: structure including “first delay module 2628,” “second delay module 2630” shown in Fig 26, “delay module 3204” shown in Fig. 32 and described at 35:1-18; the sample and hold circuit 4501 and 4503 in Fig. 45 and described at 32:44-33:19; or an analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27; or equivalents thereof.</p>	<p>Not subject to Plain-and-</p>

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