EXHIBIT 15

TECHNICAL FEATURE

Subharmonic Sampling of Microwave Signal Processing Requirements

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Introduction

Modern microwave test instruments owe much of their capabilities to powerful microwave signal processing subsystems that employ high speed sampling circuitry. These sampling heads, as they are often called, can be found at the heart of the latest sampling oscilloscopes, frequency counters, time/frequency analyzers and vector network analyzers.[1-3] The sophistication at which these instruments analyze complex microwave signals is a testimony to the power of sampling techniques for use in extracting frequency, phase and vector information.[4]

Outside of the test equipment industry, sampling techniques have been employed by phase lock oscillator and synthesizer manufacturers for many years.[5] The emergence of commercially available sampling phase detectors is an indication of the need for these types of microwave signal processing components. Along with this demand comes the need for design and application information on microwave sampling hardware.

In this paper the theory behind subharmonic sampling is explored and the physics of the sample-and-hold process are examined when applied to microwave frequencies. Through time domain analysis, the criteria for optimum sampling hardware performance is established. harmonic sampling applications are presented.

Basis of Subharmonic Sampling

Subharmonic sampling as a microwave signal processing technique may be best understood by studying sampling theory. The basic premise of sampling theory states that when a signal f(t) of bandwidth β (Hz) is sampled at a rate of f_c, which is greater than or equal to twice the signal bandwidth or 2β, no information contained in the original signal is lost. Furthermore, taking the Fourier transform of the sampling function

$$fs(t) = f(t)S(t)$$

where S(t) is the periodic sampling function of pulse width τ and period $1/f_c$, the spectrum of the sampled signal may be derived. This results in a summation of individual Fourier transforms each centered at a positive and negative integer multiple of the sampling rate

$$Fs(\omega) = dF(\omega) + d\Sigma \sin \frac{(n\pi d)}{n\pi d * F} (\omega - n\omega c)$$

For all n = ±∞ except n = 0

If the sampled signal is a baseband signal center at 0, then the reconstructed signal will be centered at 0. The frequencies of the pled signal are centered at 0, $\pm f_c$. The succeeding replicas ($\pm n \times f_c$) decrease in amplitude at the rate of $(\sin n\pi d)/n\pi d$. This theory is well suited for such applications as digitized voice. For this application the subharmonic sampling of a microwave signal must be considered.

In compliance with the guidelines of the sampling theory, the spectrum that results from a bandlimited microwave signal f(t) of bandwidth β that is sampled at the rate f_c, where $f_c \geq 2\beta$ and is also a subharmonic of f(t), or $n \times f_c = f(t)$ is considered. In this case, the fundamental replicas of the sampled signal is centered at f(t) with succeeding replicas of this reconstructed signal appearing at $\pm n \times f_c$. The FFTs, shown in Figure 1a where k = 512, show the (sin X)/X amplitude response of the sampled spectrum. The expanded FFT of Figure 1a, where k = 154, shows more clearly how the sampled RF input is reconstructed at the original frequency. The succeeding replicas of the RF input as shown are converted up and down in frequency and separated in frequency by the sampling rate F_c(Hz).

In this sampling simulation, the RF input was sampled at a subharmonic rate of one-tenth f(t). This is evident in the fact that there are indeed 10 replicas of the sampled signal in either upper or lower sideband of F(t). Typically, the baseband replica

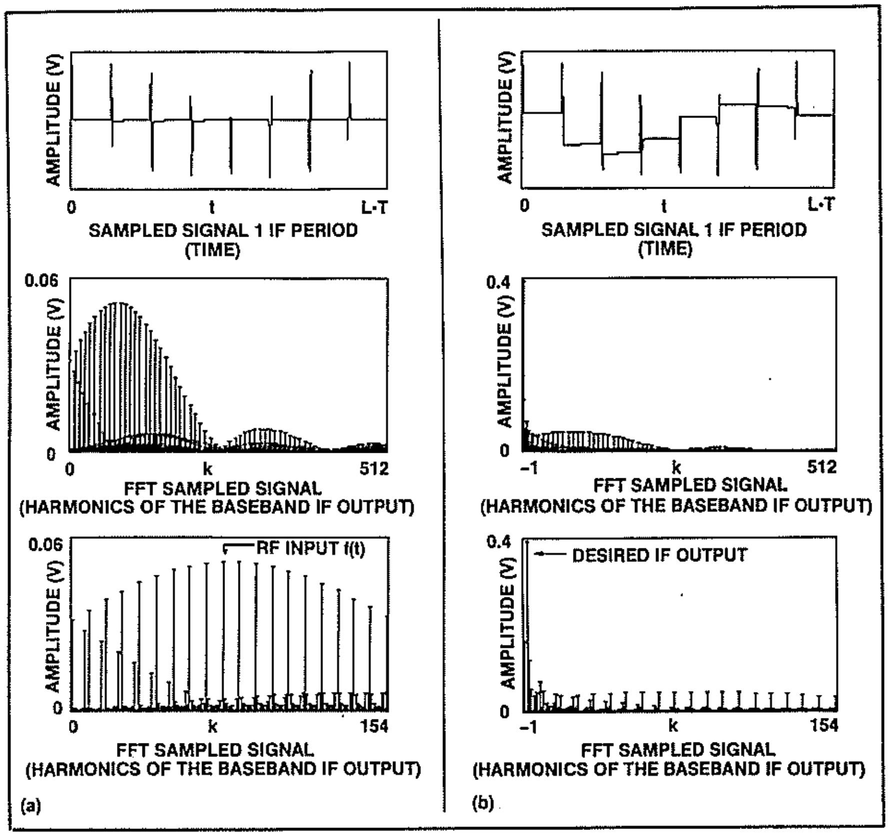

Fig. 1 Time domain analysis of the sampling process; (a) $fs(t) = f(t) \times S(t)$ periodic sampling, and (b) periodic sampling and hold into high impedance buffer.

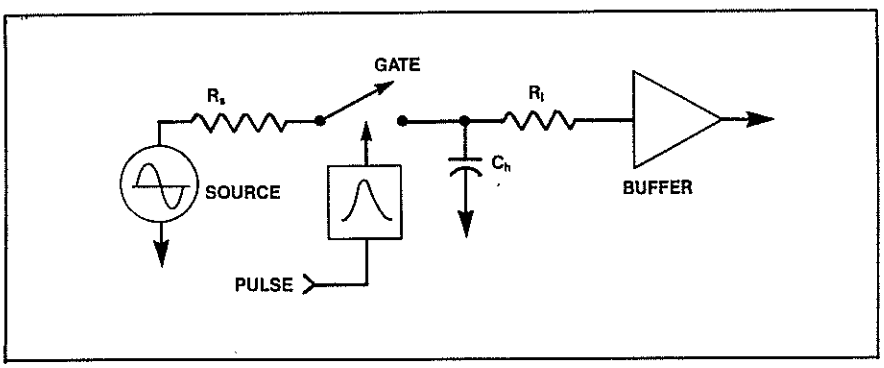

Fig. 2 An ideal subharmonic sampling model.

$f(t) - 10 \times f_c$, is the desired output signal. Extracting this baseband signal does require some circuit improvements.

Sample-and-Hold Circuit Offers Improvements Over Sampling

In order to perform sampling downconversion to baseband, the desired output of the FFT shown in Figure 1a would be the spectral replica at $f(t) - 10 \times f_c$. This is because the signal was sampled at the one-tenth subharmonic. All of the other spectral images in the FFT need to be rejected. To improve this situation, instead of multiplying F(t) by the periodic sampling function S(t), f(t) is sampled when S(t) is high and f(t) is held when S(t) is low. This logic statement allows emulation of the sample-and-hold process.

The output FFT spectrum of the defined subharmonic sample-and-hold process reveals its most significant property, which is the ability to downconvert a microwave or mm-wave signal to baseband with great efficiency and without loss of fidelity. Any loss in fidelity is due to the phase noise of the sampling clock degraded by 20 log of n. The Fourier transforms of Figure 1b show how the sample-and-hold process converts most of the sampled energy to the baseband spectral replica centered at $f(t) - n \times f_c$. This level of performance may be achieved in actual microwave and millimeter-wave subharmonic sample-and-hold circuitry when the circuit criteria are met.

Subharmonic Sample-and-Hold Circuit Modeling and Optimization

From the ideal subharmonic sample-and-hold model shown in Figure 2, parameters that must be considered during the design of a microwave sampling circuit may be defined. The source represents the microwave signal to be sampled. The source, defined by the function

$$f(s) = \sin(2\omega + \theta)$$

delivers a time variant voltage Vs of source impedance R_s Ω. During the sampling cycle, the source signal is applied to the hold capacitor C_h via the gate. The sampling aperture (t_a) is the time the gate is closed. The resistance of the gate (R_d) has been included in the total source impedance (R_s).

The parameters that come into play during the hold cycle include the hold capacitance (C_h) and the load impedance of the buffer amplifier R_l. The hold time is the period of the sampling rate (f_c) minus the sampling aperture (t_a).

During the sample cycle, the gate closes for the duration of the sampling aperture and a charge is imposed on the hold capacitor. The charge on the hold capacitor in coulombs can be expressed by

$$q = \int f(i)^{*}t \, dt$$

Because the value for Vs is a time variant function ($V(s) = \sin(\omega t)$), the integral becomes

$$q = \frac{(t_a - t_o)}{R_s} \int \sin(\omega t)^{*} e^{\left(-\frac{(t_a - t_o)}{(R_s{}^{*}C_h)}\right)} dt$$

over the interval of t_a through t_o

Integrating this function over the sampling aperture time for a given value of C_h and R_s yields the value for charge stored on the sampling capacitor in coulombs.

The value of the hold capacitor C_h is of significance as it is a parameter that the designer can easily control. Insight into the most judicious choice of sampling capacitance can be obtained by evaluating the

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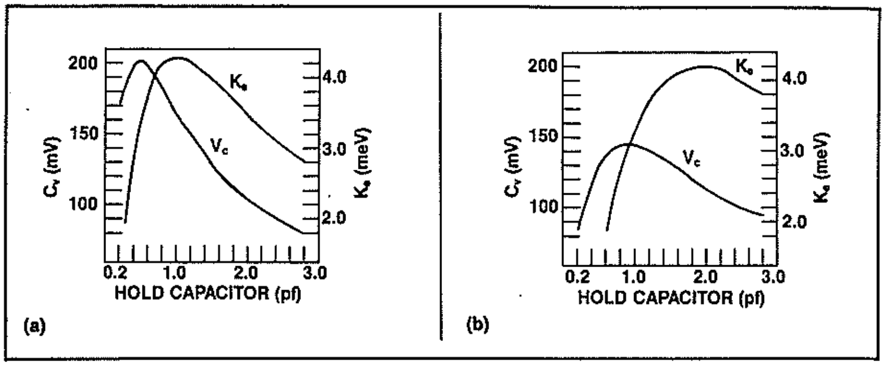

Fig. 3 Sampled voltage (Vc) and stored kinetic energy (K_e) per sample vs. hold capacitance; (a) source z transformer (50 to 25 Ω) and (b) source z transformer (50 to 12.5 Ω) with RF_{in} = 18.5 GHz @ 5 dBm and sampling aperture = 27 ps.

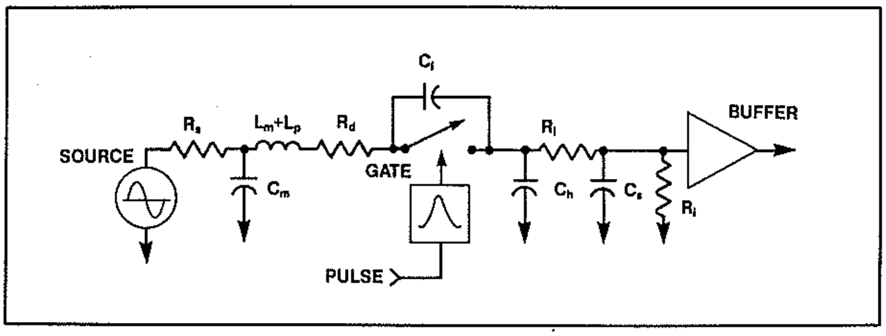

Fig. 4 An actual subharmonic sampling model.

kinetic energy stored during the sample cycle, which is equal to

$$K = \frac{(q^2)}{C_h}$$

The voltage stored on the capacitor is equal to

$$V_c = \frac{q}{C_h}$$

Figure 3 shows the effect of hold capacitance on the stored voltage V_c and the total kinetic energy for two values of R_s. The lower source impedance delivers the same kinetic energy to a larger hold capacitor that the higher impedance can only deliver to a small capacitance. The only difference for these two cases is the voltage (V_c), which decreases by the square root of the impedance ratio or by the square root of two. By increasing the incident power on the sampling circuit by 3 dB, the original voltage will be restored and the kinetic energy will be increased two fold. The hold circuit can achieve optimum performance with a larger capacitor.

Thus, it is important for the source

and-hold capacitor. In the actual sample-and-hold model, shown in Figure 4, the capacitor C_m has been included to demonstrate a matching structure that consists of C_m and L_m + L_p. This LC network makes convenient use of the series inductance of the bond wires in the sampling bridge diodes for the purpose of matching the 50 Ω source impedance to the 10 Ω gate impedance.

Output Buffer Amplifier Design Establishes IF Response

With R_s and C_h established to give maximum kinetic energy for a given sampling aperture, the effects of the buffer amplifier impedance on the stored voltage during the hold cycle are considered. An ideal sample-and-hold buffer circuit should be capable of measuring the voltage stored on the hold capacitor for the duration of the hold cycle without discharging the capacitor. The advantage of buffer circuitry, which can as nearly as possible meet this ideal requirement, is evident in the FFT of the ideal subharmonic sample-and-hold simulation, as shown in Figure 1b. Next, one may com-

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and-hold circuit that has a low impedance load, as shown in Figure 5.

The resulting poor hold duration manifests itself as an increasing inability of the sample-and-hold circuit to isolate the periodic sampling function discrete-line spectra from the output of the sample-and-hold circuit. On the other hand, if the buffer can be made to have a high impedance, the output signal will contain little harmonic energy and a much stronger baseband down-converted spectrum of the sampled signal.

Commercially available high impedance buffer amplifiers offer very impressive input impedances in the giga ohm ranges. However, these devices can have stray input capacitances of 3 pF. If connected in parallel with the hold capacitor, this capacitance would destroy the efficiency of the circuitry.

In a subharmonic sampling phase detector application, a 50 KΩ series input resistance connecting the hold capacitor to a high impedance op-amp with 3 pF of stray input capacitance would create a lowpass filter with a corner frequency at 1 MHz. This limited frequency response is adequate for phase lock loops that have bandwidths of less than 100 kHz. However, in microwave signal processing, where subharmonic sampling is used to extract information from a broadband modulated carrier or to downconvert a carrier to an IF frequency, the buffer amplifier will be required to have a frequency response as high as one-half the sampling rate. In this case, the buffer amplifier will need to have both high input impedance and very low input capacitance. A possible solution to this problem is to include the gate capacitance of a FET source follower into the total required value of hold capacitance.

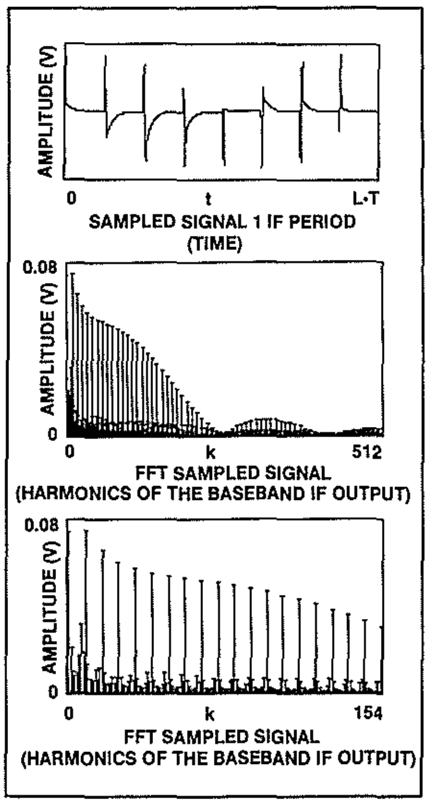

Fig. 5 Time domain analysis of periodic sampling and hold

Sampling Aperture Width Establishes Input RF Response

Maximum kinetic energy will be transferred to the hold capacitor when the sampling aperture is one-half the period of the frequency of the the sampled carrier. Sampling a

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