# Exhibit 4

Volume 6, Issue 2, 2008


# NANOCHIP

## TECHNOLOGY JOURNAL


*Serving Semiconductor Manufacturers Worldwide With Enabling Process Technology*

### In This Issue:

- Aerial Imaging, the Ultimate Defect Classifier
- New Cleaning Technology for Advanced Photomasks
- APC for 32nm Double Patterning
- Gridded Design Rules for Continued CMOS Scaling

# *Through-Silicon Via Technology — Challenges and Solutions*

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**Front Cover:** The industry is moving to 3-D packaging using through-silicon vias. Deep Reactive Ion Etch (DRIE) is the preferred technology for this etch application.

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# A Message from Ken MacWilliams

Vice President and General Manager of Applied Materials' Maydan Technology Center

One of the most exciting developments taking place in the IC industry is the work being done on through-silicon via (TSV) technology, an emerging solution for interconnecting 3-D chip stacks. This new approach promises better device performance, lower power consumption, reduced costs and the integration of heterogeneous devices. In this issue, we highlight the challenges and progress being made in TSV formation with an exclusive article featuring the viewpoints of some of Applied's leading technologists in this area.

Applied is working on several different TSV approaches at its Maydan Technology Center (MTC), where we are focusing on unit process robustness, cost-effectiveness and integration. This effort leverages Applied's broad range of process technologies and extends to several joint TSV projects with key industry partners and suppliers. Being able to use the MTC to leverage the broad range of Applied's process technologies, platforms and expertise gives us broader insight into overall manufacturability and the capability to deliver optimized and differentiated solutions.

Our research at the MTC on TSV etch processes is featured in an article that reviews both via-first and via-last applications. Since each of these have very different process requirements, the etch reactor must be flexible enough to handle both approaches. We introduce a new hardware and process scheme that provides excellent sidewall roughness without any trade-off in silicon etch rate.

Much of the other research discussed in this issue has also been conducted at the MTC, including the development of a new tantalum barrier process that addresses low k dielectric damage issues in advanced dual damascene interconnect structures and a demonstration of the use of integrated metrology to improve CD control in double patterning wafers.

Representing groundbreaking work in inspection technology, an article from our engineering team in Israel demonstrates that aerial imaging detection technology is the ultimate classifer between printing and non-printing defects, since it allows a very high detection rate without nuisance effects. This property can enable a simple migration from the 65nm node to beyond 32nm by tuning the detection limit.

In addition, we are pleased to present an article from Dr. Michael Smayling – an alum of Applied's MTC and now of Tela Innovations – on one-dimensional gridded design rules (GDR). This approach has been shown to have a number of advantages over two dimensional cells, including smaller area, better gate CD control and the elimination of hotspots. The MTC scientists have also demonstrated 22nm logic cells with Tela by leveraging the emerging Self-Aligned Double Patterning process scheme at this year's SPIE. Dr. Smayling predicts that 1-D GDR cells will enable continued simple scaling of CMOS logic to the 16nm node and beyond.

I hope that you enjoy this issue of the Nanochip Technology Journal and find the articles interesting and informative. Please feel free to contact me or the authors if you have any questions. We appreciate your comments and feedback.

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## contents

### Special Focus: TSV

PVD

# Novel Approach Extends PVD Ta

## Barrier Technology to 32nm and Below

*A new PVD tantalum (Ta) barrier process has been developed for 32nm and below copper/low k dual damascene interconnect structures. The novel process preserves the delicate low k trench integrity, while demonstrating excellent stability, manufacturability, electrical and reliability performance.*

*Keywords: Ta, PVD, Barrier Process*

The punch-through process involves the removal of barrier material from the via bottom during the etch/re-sputter step, intentionally gouging into the underlying copper (Cu) line. This process has been widely used in Cu back-end-of-line (BEOL) 65nm production because it produces high performance devices with superior reliability,[1-5] especially compared to non-punch-through processes.[6] However, the conventional punch-through process can cause physical damage to porous low k dielectrics, leading to reliability implications such as roughening of the trench bottom in dual damascene structures or microtrenching in the bottom of single trenches.

This article reports on the use of off-angular Ta neutral flux during the re-sputter process to improve the selectivity between the via and trench bottom. This protects the trench bottom and via bevel, while still allowing sufficient gouging into the underlying Cu line. In addition, the plasma density and ion energy are adjusted to further optimize selectivity and avoid micro-trenching. The result is a high deposit/etch selectivity PVD process, validated using TEM and electrical test results. This approach has extended the PVD Ta barrier process to at least the 32nm node.

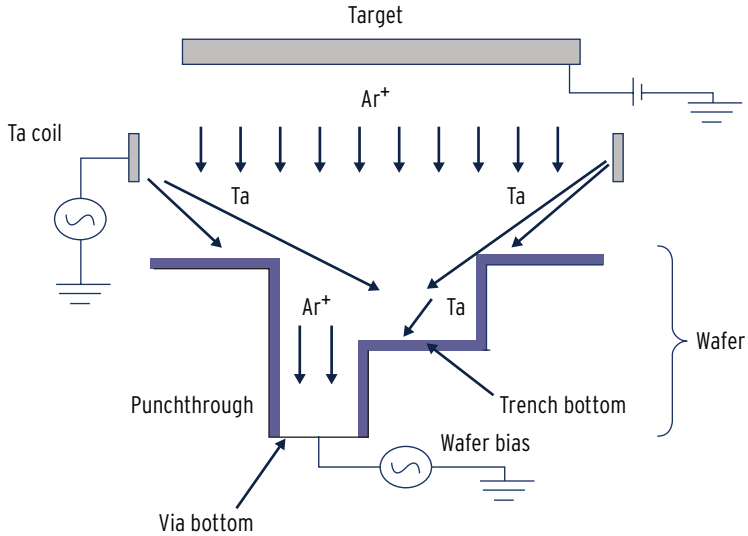


Figure 1. Diagram represents the new selective re-sputtering reactor and process. Increasing DC power on the Ta coil generates more off-angular neutral flux.

## Experimental Work

The structures used in this study were etched in a low k dielectric (k≈2.7) film. The structures contained dual damascene via chains and single trench lines with an approximate 2:1 aspect ratio. The structures were deposited with a TaN/Ta bilayer initially, followed by $Ar^+$ sputtering on the bilayer and a final barrier layer deposition step. The PVD reactor used was able to achieve high-ionization deposition and in situ $Ar^+$ sputtering capability. The step coverage performance was evaluated using TEM cross-section images and reliability was evaluated using electrical test wafers.

## Results and Discussion

Selectivity depends on the difference in

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