

**UNITED STATES DISTRICT COURT  
FOR THE WESTERN DISTRICT OF TEXAS  
WACO DIVISION**

SOLAS OLED LTD.,

v.

DELL INC.,

*Plaintiff,*

*Defendant.*

Case No. 6:19-cv-00514-ADA

SOLAS OLED LTD.,

v.

GOOGLE LLC,

*Plaintiff,*

*Defendant.*

Case No. 6:19-cv-00515-ADA

SOLAS OLED LTD.,

v.

APPLE INC.,

*Plaintiff,*

*Defendant.*

Case No. 6:19-cv-00537-ADA

SOLAS OLED LTD.,

v.

HP INC.,

*Plaintiff,*

*Defendant*

Case No. 6:19-cv-00631-ADA

**JOINT CLAIM CONSTRUCTION STATEMENT**

Under the scheduling orders in the four above-captioned cases, Plaintiff Solas OLED LTD. (“Solas”) and Defendants Dell Inc. (“Dell”), Google LLC (“Google”), Apple Inc. (“Apple”), and HP Inc. (“HP”) submit this Joint Claim Construction Statement. The four cases are consolidated for claim construction proceedings with the hearing scheduled for August 14, 2020.

The four cases involve a total of five asserted patents: U.S. Patent Nos. 6,072,450 (“’450 patent”), 7,446,338 (“’338 patent”), 7,573,068 (“’068 patent”), 7,499,042 (“’042 patent”), and 7,663,615 (“’615 patent”). Specifically:

- The ’450 patent is asserted in *Solas v. Dell* (6:19-cv-00514-ADA), *Solas v. Google* (6:19-cv-00515-ADA) and *Solas v. Apple* (6:19-cv-00537-ADA);
- The ’338 patent is asserted in *Solas v. Google* (6:19-cv-00515-ADA) and *Solas v. Apple* (6:19-cv-00537-ADA);
- The ’068 patent is asserted in *Solas v. Apple* (6:19-cv-00537-ADA) and *Solas v. HP* (6:19-cv-00631); and
- The ’042 and ’615 patents are asserted in *Solas v. HP* (6:19-cv-00631).

The following are the parties’ agreed and proposed claim constructions.

## I. AGREED CLAIM CONSTRUCTIONS

### A. ’450 patent

Claim Term / Asserted Claim(s)	Agreed Construction
“active elements” (claims 1, 4)	circuit elements that have gain or that direct current flow, e.g., transistors
“light lays [sic] in a first wavelength range pass through said at least one filter selectively when	Plain and ordinary meaning. “lays [sic]” means and should be replaced with “rays”

<b>Claim Term / Asserted Claim(s)</b>	<b>Agreed Construction</b>
incident light rays in a second wavelength range including said first wave length range enter said at least one filter”  (claim 12)	

**B. '338 patent**

<b>Claim Term / Asserted Claim(s)</b>	<b>Agreed Construction</b>
“the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate”  (claim 1)	the pixel electrodes are arrayed along the interconnections and located between the interconnections, and the pixel electrodes are on the surface of the transistor array substrate
“write current”  (claim 1)	pull-out current

**C. '068 patent**

<b>Claim Term / Asserted Claim(s)</b>	<b>Agreed Construction</b>
“feed interconnections”  (claims 1, 13)	conductive structures in a different layer or layers than the supply line that also provide connections to a source that supplies voltage and/or current
“patterned together [with]”	“patterned to fit together [with]” wherein “patterning” may consist of one of more fabrication steps <sup>1</sup>

<sup>1</sup> Solas, Apple, and HP filed a joint motion adopting this construction, while also preserving the right of Apple and HP to appeal the construction based on the positions, record, and arguments

Claim Term / Asserted Claim(s)	Agreed Construction
(claims 1, 13)	

**D. '615 patent**

Claim Term / Asserted Claim(s)	Agreed Construction
“gradation” (claims 11, 13)	level
“light emission control section” (claim 11)	drive transistor

**II. DISPUTED TERMS FOR CONSTRUCTION**

**A. '338 patent**

Claim Term / Asserted Claim(s)	Solas’s Construction	Defendants’ Construction
“transistor array substrate” (claim 1, 4)	layered structure upon which or within which a transistor array is fabricated	a layered structure composed of a bottom insulating layer through a topmost layer on whose upper surface pixel electrodes are formed, which contains an array of transistors
“project from a surface of the transistor array substrate” (claim 1)	extend from an external surface of the transistor array substrate	extend above the upper surface of the transistor array substrate

made in *Solas OLED Ltd. v. LG Display Co., Ltd. et al.*, 6:19-CV-00236-ADA (W.D. Tex.), which the court granted. Dkt. 47, 49.

**B. '068 patent**

<b>Claim Term / Asserted Claim(s)</b>	<b>Solas's Construction</b>	<b>Defendants' Construction</b>
“supply lines” (claims 1, 13)	conductive lines supplying current or voltage	conductive lines, each supplying a driving current or voltage to a plurality of pixel circuits
“signal lines” (claims 1, 13)	conductive lines supplying signals	conductive lines carrying data
“formed on said plurality of supply lines along said plurality of supply lines” (claim 1)	formed on said plurality of supply lines over the length or direction of said plurality of supply lines	stacked on or making multiple contacts with said plurality of supply lines over the length of each supply line
“connected to said plurality of supply lines along said plurality of supply lines” (claim 13)	connected to said plurality of supply lines over the length or direction of said plurality of supply lines	stacked on or making multiple contacts with said plurality of supply lines over the length of each supply line
“source” (claims 1, 5, 12, 13, 17)	Plain and ordinary meaning	source electrode  Alternatively: “the patterned conductive film that is connected to one end of the TFT channel region through a doped semiconductor region.”
“drain” (claims 1, 5, 12, 13, 17)	Plain and ordinary meaning	drain electrode  Alternatively: “the patterned conductive film that is connected to one end of the TFT channel region through a doped semiconductor region.”

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