EXHIBIT 13

Case 1:20-cv-00765-DAE Document 40-13 Filed 10/17/22 Page 2 of 8 Specification Volume 1

Specification of the Bluetooth System

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BLUETOOTH SPECIFICATION Version 1.0 B

page 128 of 1082

Baseband Specification

Bluetooth...

The address input consists of 28 bits, i.e., the entire LAP and the 4 LSBs of the UAP. In **CONNECTION** state, the address of the master is used. In **page** substate the address of the paged unit is used. When in **inquiry** substate, the UAP/LAP corresponding to the GIAC is used. The output constitutes a pseudorandom sequence, either covering 79 hop or 23 hops, depending on the state.



Figure 11.1: General block diagram of hop selection scheme.

For the 79-hop system, the selection scheme chooses a segment of 32 hop frequencies spanning about 64 MHz and visits these hops once in a random order. Next, a different 32-hop segment is chosen, etc. In case of the **page**, **page scan**, or **page response** substates, the same 32-hop segment is used all the time (the segment is selected by the address; different units will have different paging segments). In connection state, the output constitutes a pseudo-random sequence that slides through the 79 hops or 23 hops, depending on the selected hop system. For the 23-hop systems, the segment size is 16. The principle is depicted in Figure 11.2



Figure 11.2: Hop selection scheme in CONNECTION state.

BLUETOOTH SPECIFICATION Version 1.0 B

page 129 of 1082

Baseband Specification

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11.2 SELECTION KERNEL

The hop selection kernels for the 79 hop system and the 23 hop system are shown in Figure 11.3 on page 129 and Figure 11.4 on page 129, respectively. The X input determines the phase in the 32-hop segment, whereas Y1 and Y2 selects between master-to-slave and slave-to-master transmission. The inputs A to D determine the ordering within the segment, the inputs E and F determine the mapping onto the hop frequencies. The kernel addresses a register containing the hop frequencies. This list should be created such that first all even hop frequencies are listed and then all odd hop frequencies. In this way, a 32-hop segment spans about 64 MHz, whereas a 16-hop segment spans the entire 23-MHz.



Figure 11.3: Block diagram of hop selection kernel for the 79-hop system.



Figure 11.4: Block diagram of hop selection kernel for the 23-hop system.

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Case 1:20-cv-00765-DAE Document 40-13 Filed 10/17/22 Page 5 of 8

BLUETOOTH SPECIFICATION Version 1.0 B

page 130 of 1082

Baseband Specification

Bluetooth

The selection procedure consists of an addition, an XOR operation, a permutation operation, an addition, and finally a register selection. In the remainder of this chapter, the notation A_j is used for bit i of the BD_ADDR.

11.2.1 First addition operation

The first addition operation only adds a constant to the phase and applies a modulo 32 or a modulo 16 operation. For the page hopping sequence, the first addition is redundant since it only changes the phase within the segment. However, when different segments are concatenated (as in the channel hopping sequence), the first addition operation will have an impact on the resulting sequence.

11.2.2 XOR operation

Let Z' denote the output of the first addition. In the XOR operation, the four LSBs of Z' are modulo-2 added to the address bits A_{22-19} . The operation is illustrated in Figure 11.5 on page 130.



Figure 11.5: XOR operation for the 79-hop system. The 23-hop system is the same except for the Z'_4/Z_4 wire that does not exist.

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