EXHIBIT 30

EXHIBIT 10

Version 1.10 26-Jul-2011   MIPI Alliance Specification for RFFE

MIPI® Alliance Specification for RF Front-End Control Interface

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Further technical changes to this document are expected as work continues in the RF Front-End Control Working Group

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4 Architecture and Operations Overview

85   This section is intended to convey an overview of the architecture and operational details of the RFFE interface.

4.1 Overview

86   RFFE is a two-wire, serial interface intended to be used to connect Radio Frequency ICs (RFIC) of a mobile terminal to their related Front-End Modules (FEM). The RFFE interface enables systems to efficiently control various FEMs in next generation mobile terminals with increased complexity of performance supporting multi-mode, multi-band and multiple antennas, all with a minimum number of wires and pins using a single RFFE bus. It is designed to support existing 3GPP standards such as LTE, EGPRS, UMTS, HSPA, etc. and also other, non-3GPP air interfaces. The RFFE interface is based on *MIPI Alliance Specification for System Power Management Interface (SPMI)* [MIPI03]. The RFFE interface is intended to be efficient, flexible, and extensible, accommodating many variations in the overlying system design, while providing interoperability at the interface level between compliant RFICs and FEMs. The ability to design one common control interface which may be reused for all of these modules helps reduce front-end complexity, and hence speed up the time-to-market for these terminals.

87   Within the mobile terminal, the RFIC is the Master and the FEMs are the Slaves on the RFFE bus. Command Sequences on the bus may only be initiated by the Master. A Slave shall not initiate Command Sequences on the bus. This specification defines the operating states, the Command Sequence set, the physical interface, and the protocol for data communication between RFFE devices on an RFFE bus to insure the compatibility of control and data transfers. The RFFE Command Sequence set includes Slave addressing, control of the Slave operating state, register read from and register write to Slaves, as well as Command Sequences supporting the use of Device Descriptor Block [MIPI05].

88   The key pillars of the RFFE design include the following considerations:

89   •   Minimize the wiring effort in the front-end of a mobile terminal
90   •   Minimize pin count
91   •   Ease and optimize control flow
92   •   Ensure minimal EMI contributions due to RFFE bus
93   •   Minimize complexity for the Slave
94   •   Add flexibility and scalability, allowing use of multiple receivers and transmitters simultaneously

95   The basic configuration of the RFFE interface and its bus structure are shown in Figure 1. As RFFE is based on the SPMI interface it shall have two signals, one serial bidirectional data signal (SDATA) and one clock signal (SCLK) controlled by the Master. Any additional signals present on an RFFE device shall not change the behavior of the RFFE interface protocol or prevent the operation of the RFFE bus described in this specification.

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