

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

GODO KAISHA IP BRIDGE 1,	§	
	§	
Plaintiff,	§	
	§	
v.	§	No. 2:17-CV-00676-RWS-RSP
	§	
INTEL CORPORATION,	§	
	§	
Defendant.	§	

CLAIM CONSTRUCTION OPINION AND ORDER

This lawsuit concerns eight United States patents relating to semiconductor technology: U.S. Patents 6,197,696; 6,346,736; 6,387,824; 6,602,802; 6,709,950; 6,967,409; 7,279,727; and RE 41,980. The parties have agreed to constructions for certain terms from six of these patents. *See Part II infra.*

Terms from three of the patents remain disputed. The '736 Patent, titled "Trench Isolated Semiconductor Device," discloses a device with a dielectric film between the wiring and substrate of a semiconductor to reduce the capacitance between them. The '824 Patent and '802 Patent teach methods of forming wiring structures using a porous film between the wiring, which also reduces internal capacitance of the device. The lower the capacitance between the wiring and the substrate (in the case of the '736 Patent) and the wiring in the devices (in the case of the '824 and '802 Patents), the higher the operating speed.

I. GENERAL LEGAL STANDARDS

A. Claim Construction

“[T]he claims of a patent define the invention to which the patentee is entitled the right to exclude.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc). As such, if the parties dispute the scope of the claims, the court must determine their meaning. *See, e.g., Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 390 (1996), *aff’g*, 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc); *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1317 (Fed. Cir. 2007).

When construing claims, “[t]here is a heavy presumption that claim terms are to be given their ordinary and customary meaning.” *Aventis Pharm. Inc. v. Amino Chems. Ltd.*, 715 F.3d 1363, 1373 (Fed. Cir. 2013) (citing *Phillips*, 415 F.3d at 1312–13). Courts must therefore “look to the words of the claims themselves . . . to define the scope of the patented invention.” *Id.* (citations omitted). The “ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.” *Phillips*, 415 F.3d at 1313. This “person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.” *Id.*

Intrinsic evidence is the primary resource for claim construction. *See Power-One, Inc. v. Artesyn Techs., Inc.*, 599 F.3d 1343, 1348 (Fed. Cir. 2010) (citing *Phillips*, 415 F.3d at 1312). For certain claim terms, “the ordinary meaning of claim language as understood

by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words.” *Phillips*, 415 F.3d at 1314. But for claim terms with less-apparent meanings, courts consider “those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean . . . [including] the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.” *Id.*

II. AGREED CONSTRUCTIONS

The parties agree to the following constructions, which the Court hereby adopts. Joint Cl. Constr. & Prehearing Statement [Dkt. # 85] at 2–3; Notice of Supplement to Joint Cl. Constr. Statement [Dkt. # 103].

Claim Term	Agreed Construction
using the [first resist pattern/second resist pattern and the mask pattern/patterned third insulating film] as a mask (’696 Patent, cl.13)	using the [first resist pattern/second resist pattern and the mask pattern/patterned third insulating film] to define areas for etching
step order (’696 Patent, cl.13)	steps (a)–(k) must be performed in the order listed.
interlayer insulating film (’980 Patent, cl.18, 33, 35, 50)	an insulating film located between but not within layers
small dielectric constant (’980 Patent, cl.18, 35)	a dielectric constant not greater than that of silicon dioxide

said bonding pad in said opening and said second dielectric film of said surface protecting film completely cover said first dielectric film so as not to expose said first dielectric film ('980 Patent, cl.18)	the bonding pad and the second dielectric film each covers a portion of the first dielectric film, and the bonding pad and the second dielectric film collectively cover the first dielectric film so that it is not exposed to above
wherein said bonding pad covers said opening ('980 Patent, cl.35)	plain and ordinary meaning
a surface protecting film ('980 Patent, cl.18, 35)	plain and ordinary meaning
a conductor pad which is provided on the gate interconnect part ('727 Patent, cl.10)	plain and ordinary meaning
wherein the gate contact is in contact with the conductor pad ('727 Patent, cl.10)	wherein the gate contact is physically touching the conductor pad
a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region ('736 Patent, cl.6, 7, 11, 13, 14, 16)	plain and ordinary meaning
resistor film ('736 Patent, cl.13, 14, 16)	plain and ordinary meaning
forming . . . on ('950 Patent, cl.1, 17)	forming . . . directly or indirectly on
formed on ('409 Patent, cl.1, 25, 26, 64)	formed directly or indirectly on

III. CONSTRUCTION OF DISPUTED TERMS

A. “dielectric film” (’736 Patent, cl.6–8)

Godo Kaisha’s Proposed Construction	Intel’s Proposed Construction
plain and ordinary meaning	a dielectric film for reducing the capacitance between the wire and the substrate

FIG. 19 of the ’736 Patent (see below) shows a prior-art trench-isolated semiconductor device having an active region (6) of a silicon substrate (1), a gate electrode (4), and source/drain regions (5). An isolation region (7) surrounds the active region (6) and includes multiple trench portions (8), each filled with a silicon oxide film. Semiconductor portions (9) are between the trench portions (8). A polysilicon wire (10) is on one trench portion (8). A gate oxide film (2) and gate electrode (4) are on the substrate (1) over the active region (6). An interlayer insulating film (12) covers the surface of the substrate (1), and a metal wire (13) is on the insulating film (12). ’736 Patent at 1:35–51.

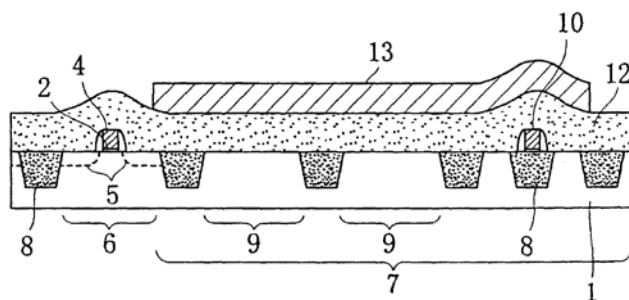


FIG. 19 of the ’736 Patent

Generally, these types of trench-isolation techniques improve some operating characteristics relative to other devices, but tend to increase the wire-to-substrate capacitance because of the smaller distances between the wire (13) and substrate (1) in the regions

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