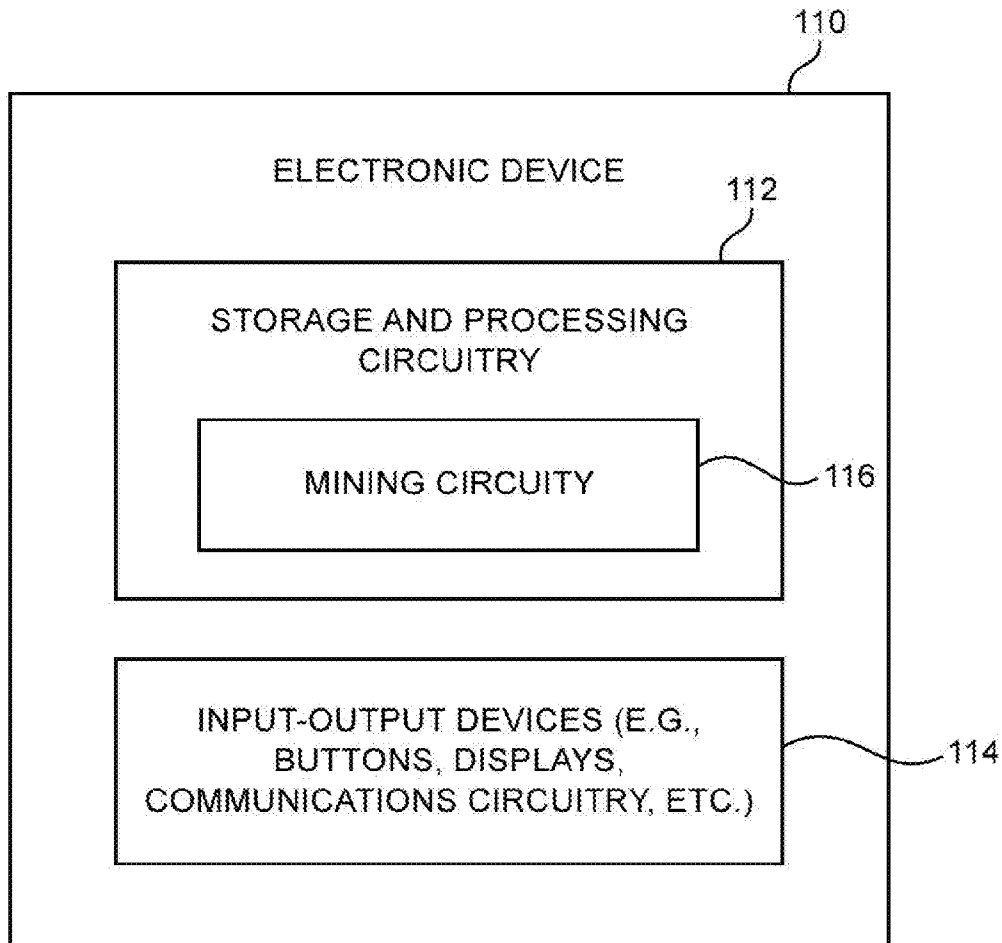




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Kheterpal et al.(10) **Pub. No.: US 2016/0125040 A1**(43) **Pub. Date: May 5, 2016**(54) **DIGITAL CURRENCY MINING CIRCUITRY
HAVING SHARED PROCESSING LOGIC**(52) **U.S. Cl.**
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(2013.01); *G06Q 20/06* (2013.01)(71) Applicant: **21, Inc.**, San Francisco, CA (US)(72) Inventors: **Veerbhan Kheterpal**, Santa Clara, CA
(US); **Daniel Firu**, San Jose, CA (US);
Nigel Drego, San Francisco, CA (US)(21) Appl. No.: **14/866,102**(22) Filed: **Sep. 25, 2015****Related U.S. Application Data**(60) Provisional application No. 62/073,522, filed on Oct.
31, 2014.**Publication Classification**(51) **Int. Cl.**
G06F 17/30 (2006.01)
G06Q 20/06 (2006.01)(57) **ABSTRACT**

An integrated circuit may be provided with cryptocurrency mining capabilities. The integrated circuit may include control circuitry and a number of processing cores that complete a Secure Hash Algorithm 256 (SHA-256) function in parallel. Logic circuitry may be shared between multiple processing cores. Each processing core may perform sequential rounds of cryptographic hashing operations based on a hash input and message word inputs. The control circuitry may control the processing cores to complete the SHA-256 function over different search spaces. The shared logic circuitry may perform a subset of the sequential rounds for multiple processing cores. If desired, the shared logic circuitry may generate message word inputs for some of the sequential rounds across multiple processing cores. By sharing logic circuitry across cores, chip area consumption and power efficiency may be improved relative to scenarios where the cores are formed using only dedicated logic.



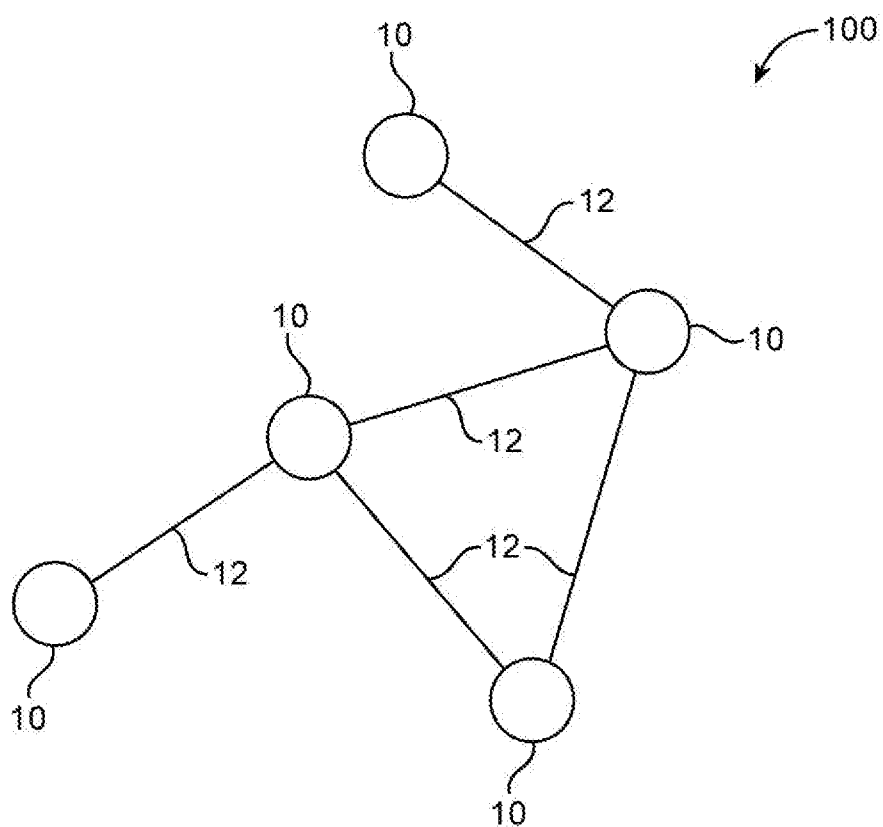


FIG. 1

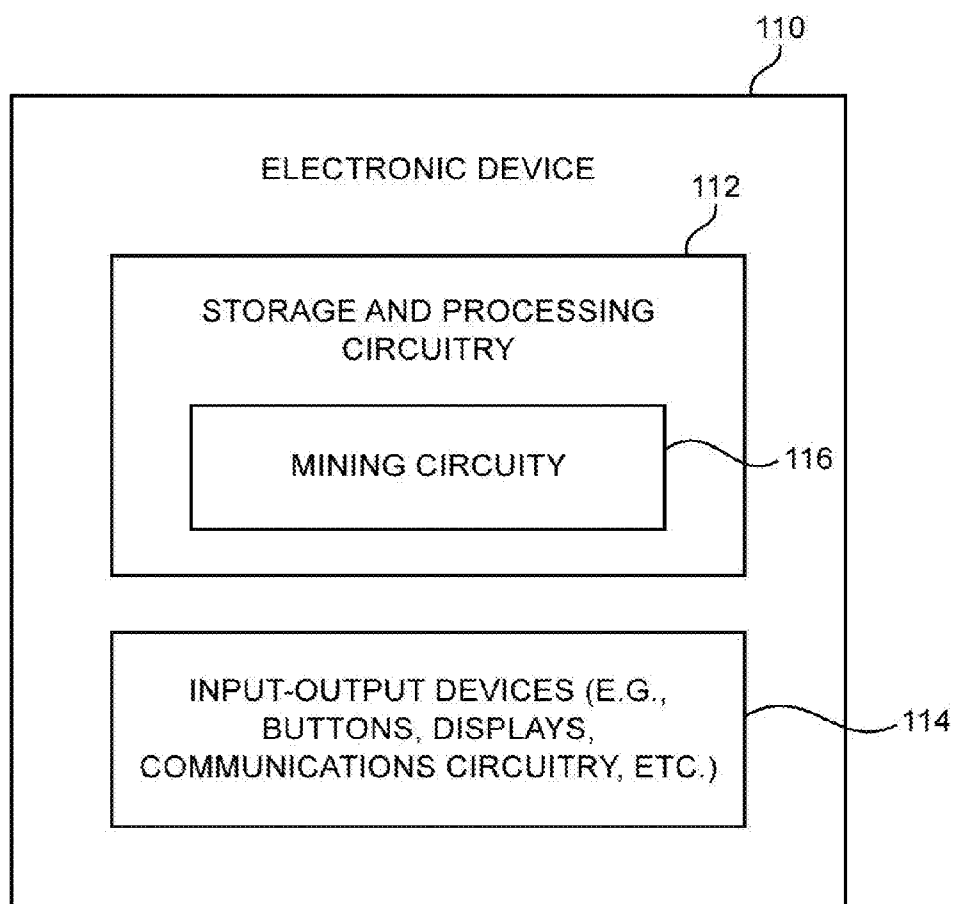
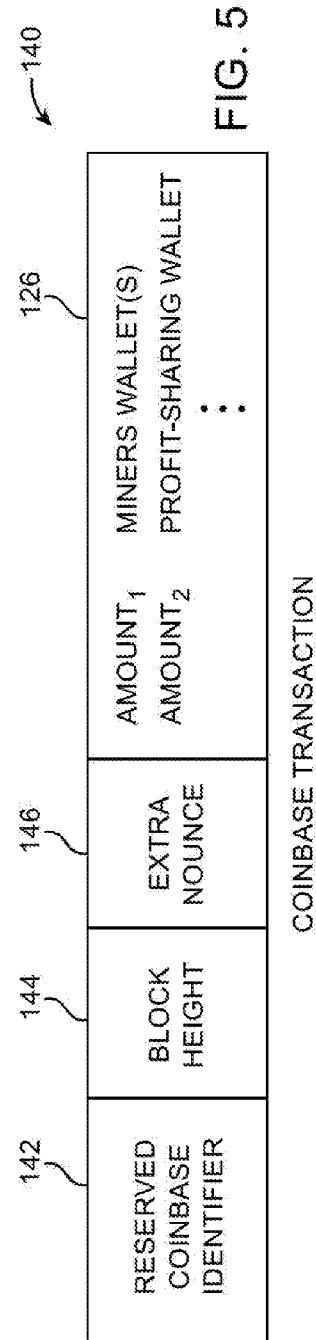
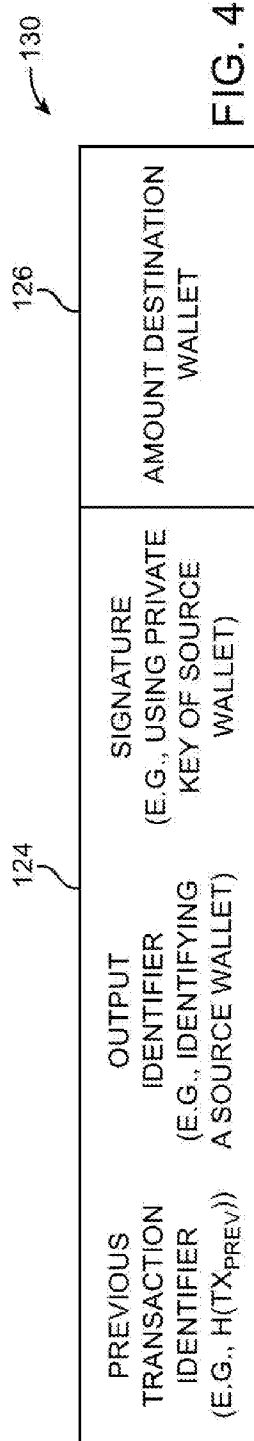
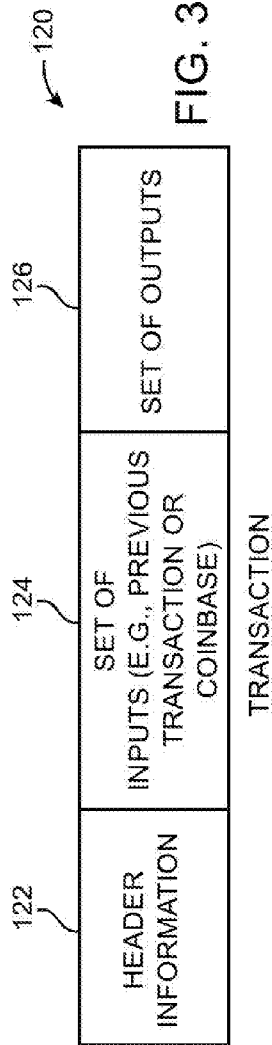


FIG. 2



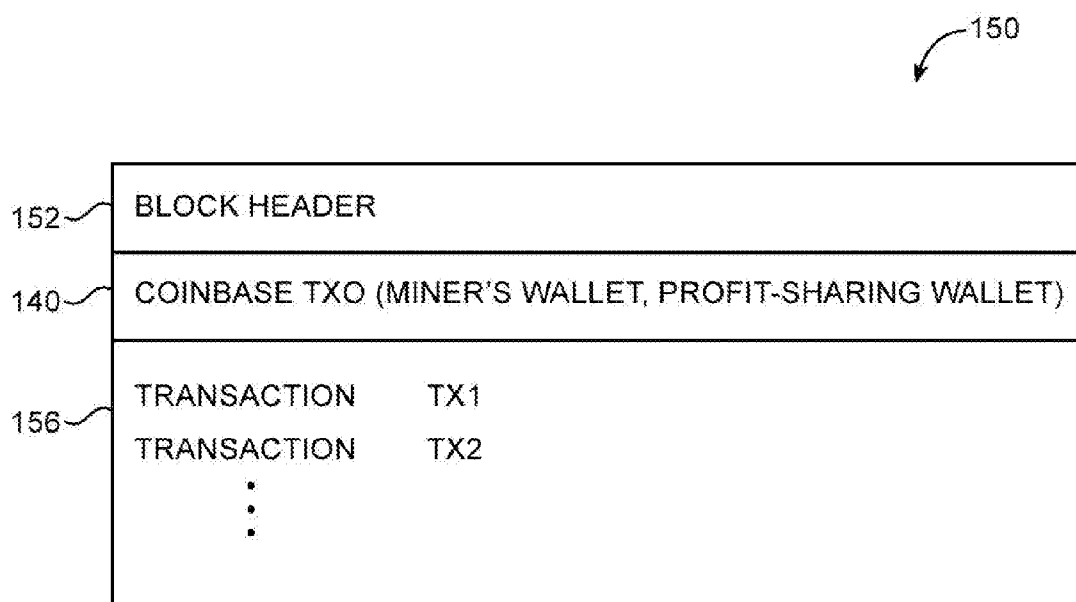


FIG. 6

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