UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AVX CORPORATION
Petitioner
v.

SAMSUNG ELECTRO-MECHANICS CO., LTD.
Patent Owner

Case No. PGR2017-00010
Patent No. 9,326,381

DECLARATION OF MICHAEL RANDALL IN SUPPORT OF PATENT OWNER'S RESPONSE TO PETITION

TABLE OF CONTENTS

I. INTRODUCTION

1. I am a consultant in electronic materials and processing, ceramic dielectric materials and processes, passive electronic components, and surface mount technology, including with respect to ceramic capacitors.

2. I have been retained in this matter by Samsung Electro-Mechanics Co., Ltd. ("SEM") to provide opinions regarding the instituted grounds of review of the Petition for Post-Grant Review (the "Petition") of U.S. Pat. No. 9,326,381 (Ex. 1001, the "'381 patent") filed by AVX Corporation ("AVX").

3. I am being compensated for my work in this matter. My compensation in no way depends upon the outcome of this proceeding. I have no financial interest in SEM or the '381 patent.

4. I am not a patent attorney. My understanding of legal principles regarding patent validity and claim construction is based on information provided to me by SEM's counsel, which I have relied on in forming my opinions set forth in this declaration.

5. It is my opinion that challenged claims 1–4, 6–11, and 13–19 of the '381 patent are not rendered obvious based on the instituted grounds.

II. QUALIFICATIONS AND PRIOR TESTIMONY

6. A copy of my curriculum vitae is attached as Exhibit A, and it details

my qualifications and experience, as well as listing my publications and prior testimony. I have been involved in the field of Electronic Materials and Processing, Ceramic Dielectric Materials and Processes, Passive Electronic Components, and Surface Mount Technology, for more than 25 years and have experience in the design and manufacture of ceramic capacitors, as detailed in my curriculum vitae (Ex. A). I am an inventor on several patents in these areas.

7. I earned a Bachelor of Science degree in ceramic engineering from the NYSCC at Alfred University, Alfred NY in 1985. I earned a Master of Science degree in Materials Science and Engineering from the University of Florida, Gainesville, FL in 1987. I earned a Ph.D. in Materials Science and Engineering from the University of Florida in 1993 as well. I earned a Master of Business Administration from Webster University in 1995.

8. From 1992 to 1997, I was employed by AVX Corporation. My positions at AVX Corporation included Manager of Ceramic Capacitor Research and Development, during which I was responsible for planning and oversight of multi-layered ceramic capacitor and materials development.

9. From 1997 to 1999, I was employed by Ferro Corporation. My positions at Ferro Corporation included Director of Research and Development, during which I was responsible for planning, direction, and oversight of division

level research and development, and new product development, including Low Temperature Cofired Ceramic Systems and Multilayer Materials Systems.

10. From 1999 to 2008, I was employed by KEMET Electronics. My positions at KEMET Electronics included Director of Ceramic Technology, during which I was responsible for the direction of teams providing technology solutions for multilayer ceramic capacitor development needs. My positions at KEMET also included Director of Ceramic Technical Marketing and New Business Development, during which I was responsible for identification and management of ceramic capacitor technical marketing, including multilayer ceramic capacitors, and associated product lines. My positions at KEMET also included Director of Advanced Ceramic Technology, during which I was responsible for new product development for advanced ceramic products, including various capacitor types, and resulting in several inventions.

11. Since 2003, I have been an independent consultant with Almegacy LLC in a variety of electronic device and material projects, including electronic component selection and sourcing for capacitors. I have served as an expert witness in the subject area of capacitors, including matters before the United States District Court, including the Central District of California, the Southern District of California, the Eastern District of Texas, and the Eastern District of NY. I have also served as an expert witness in the subject area of capacitors and electronic

components before the International Trade Commission. And I have served as an expert witness in the subject area of capacitors for matters considered by the United States Patent and Trademark Office regarding nine different patents.

12. This report and my opinions are based upon my own qualifications and experience and my personal knowledge.

III. MATERIALS CONSIDERED

13. In forming my opinions, I considered the Petition and its associated exhibits (including the '381 patent (Ex. 1001), its file history (Ex. 1002), the cited prior art, and its attached declarations (see the List of Documents Reviewed, the List of Exhibits, as well as this Report)), as well as SEM's preliminary response and its exhibits (see the List of Documents Reviewed, the List of Exhibits, as well as this Report)), as well as the Patent Trial and Appeals Board ("Board")'s institution decision and any other exhibits or literature cited in this declaration or cited in the associated List of Exhibits or List of Documents Reviewed. My opinions are based upon my education, my related research and experience, as well as my investigation and the study of relevant materials. I may rely upon these materials and/or additional materials to counter arguments raised by the Petitioner. I may also consider additional information and documents, including information and documents that may not yet have been provided to me, in forming any necessary opinions.

14. My analysis of relevant materials produced is ongoing and I will continue to review any new material as it is provided. This declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided or on new materials provided.

IV. BACKGROUND OF THE TECHNOLOGY

A. Overview

15. I have been informed by counsel that during a post-grant review, the Board construes claim terms according to their broadest reasonable construction in light of the specification of the patent in which they appear. (37 C.F.R. § 42.200(b)). Taking this into consideration, it is my opinion that the scope of background technology of the '381 patent includes certain types of multilayer ceramic capacitors.

16. The '381 patent relates to a multilayer ceramic capacitor and a board having the same mounted thereon. ('381 at 1:15-16). The '381 patent does not mention varistors, or thermistors, such as PTCR (positive temperature coefficient of resistance) thermistors, and those are outside the scope of the '381 patent. Additionally, one skilled in the art would have understood that the scope of the technology related to the '381 patent does not include all capacitors.

17. To explain, there are numerous types of capacitors. The primary major

discriminator between capacitors is whether they are electrostatic or electrolytic. Electrolytic capacitors utilize an electrolyte to facilitate charge transfer and are not within the scope of the '381 patent. A person of skill in the art (POSITA) would have understood that the '381 patent does not pertain to electrolytic capacitors. A POSITA also would have understood that the '381 pertains only to a specific type of electrostatic capacitors.

18. To explain, electrostatic capacitors utilize solid state conductors (e.g., metal electrodes) as a means to facilitate charge (e.g., electron) transfer. A POSITA further would have understood that a subset of electrostatic capacitors is multilayer capacitors, and that traditional single layer capacitors are also excluded from the scope of the subject matter of the '381 patent as they have a different electrode configuration than multilayer ceramic capacitors.

19. Additionally a POSITA would have understood that the '381 patent does not pertain to all multilayer capacitors. For example, a POSITA would have understood that multilayer capacitors that are made from non-ceramic dielectric materials, such as organic film capacitors, and the like, are outside the scope of the '381 patent.

20. A POSITA further would have understood that the scope of the art of the '381 patent includes only certain ceramic dielectric materials, but not all ceramic dielectric materials, as an objective of the '381 patent is to reduce or minimize

acoustic noise ('381 at 9:9-13:23). Since acoustic noise is insignificant for many types of dielectric ceramics (e.g., non-ferroelectric dielectrics, such as linear dielectrics or Class 1 dielectrics, as well as intergranular barrier layer capacitors (IBLC) materials, which utilize a ceramic material that is comprised of semiconducting grains between insulating barriers at each grain boundary), a POSITA would have understood that the scope of the subject matter of the '381 patent is limited to multilayer ceramic capacitors that are made with ceramic dielectric materials that are ferroelectric or that otherwise exhibit electrostrictive or piezoelectric characteristics or characteristics that cause displacement of the dimensions of the dielectric material when said material is placed under an electric field as discussed below. Thus, a POSITA would have understood that the '381 patent pertains not to multilayer ceramic capacitors comprised of linear ceramic dielectric materials, and not to multilayer ceramic capacitors comprised of intergranular barrier layer materials (IBLC). A POSITA would also have understood that the '381 patent pertains only to multilayer ceramic capacitors comprised of ferroelectric ceramic dielectrics, or other ceramic dielectric materials that exhibit significant mechanical displacement when said material is placed under an electric field as discussed below.

21. A POSITA also would have understood that the '381 patent pertains to "reverse geometry" multilayer ceramic capacitors (MLCC). The term "reverse

geometry" refers to a reversal in the length (L) and width (W) dimensions of the MLCC (e.g., reversal of length and width dimensions from 1206 (0.126"L x 0.63"W) to 0612 (0.063"L x 0.126"W)) as illustrated below. The reverse geometry of the MLCC device results in internal electrodes that are wider and shorter than the internal electrodes of a traditional MLCC since conductors that have increased cross sectional area, combined with shorter current path length exhibit reduced inductance or ESL. Thus, the reverse geometry configuration exhibits reduced inductance or reduced equivalent series inductance (ESL) compared to a standard MLCC of the same peripheral size. For example, the inductance of a standard MLCC has been measured to be approximately double (1250 pH) that of a reverse geometry MLCC (610 pH) when comparing traditional 1206 MLCCs to reverse geometry 0612 MLCCs.[1]

Standard MLCC vs. Reverse Geometry MLCC[2]

[1] Ex. B: J. Cain, "Parasitic Inductance of Multilayer Ceramic Capacitors," AVX Technical Information, p. 4/4, June 1997. https://www.avx.com/docs/techinfo/CeramicCapacitors/parasitc.pdf

[2] Source: Vishay, Capacitors-Ceramic-Surface Mount: https://www.vishay.com/capacitors/ceramic/surface-mount/, Source: Digi-Key Electronics, Product Index-Capacitors-Ceramic Capacitors- AVX Corporation 06125C104MAT2A: https://www.digikey.com/product-detail/en/avx-corporation/06125C104MAT2A/478-2901-1-ND/776677

22. Reduced inductance in an MLCC is generally preferable for increased frequency applications (e.g., ca. 100 KHz and above) as relatively low inductance reduces device impedance as described below. Simply put, impedance in alternating current (AC) circuits is analogous to resistance for direct current (DC) circuits. Reduced impedance in AC circuits results in less power loss in transmission (generally preferable), which aids in the performance of myriad applications such as high speed decoupling and the like. Realizing this, the inventors on the '381 patent embraced the objective of creating a low inductance MLCC device, having high capacitance density and low acoustic noise emission as explained herein. They also embraced the objective of designing the accompanying circuit board, to which said devices would be mounted, such that the benefits of low inductance and low acoustic noise emission exhibited by the MLCC device(s) are not sacrificed, but remain improved or are further improved.

23. The '381 patent mentions inductance or equivalent series inductance (ESL) at least 10 separate times:

1. "In the case of a multilayer ceramic capacitor, as equivalent series inductance (hereinafter referred to as "ESL") increases, performance of an electronic product may deteriorate." (*Id*. at 1:22-25).
2. "In addition, in a case in which an electronic component is miniaturized and capacitance thereof is increased, the influence of an increase in ESL on deterioration in performance of the electronic product has relatively increased." (*Id*. at 1:25-28).

3. “A so-called "low inductance chip capacitor (LICC)" is to decrease inductance by decreasing a distance between external terminals to shorten a current flow path.” (*Id*. at 1:29-31).
4. “Since the distance between the first and second external electrodes **131** and **132** is shortened, the current path may be shortened, resulting in a reduction in inductance.” (*Id*. at 6:1-3).
5. “The first and second internal electrodes **121** and **122** are alternately exposed to the first or second side surface S5 or S6, such that a reverse geometry capacitor (RGC) or low inductance chip capacitor (LICC) may be obtained as described below.” (*Id*. at 5:17-21).
6. “In this case, when an alternative current (AC) voltage is applied to the external electrodes, a current path is relatively long, whereby an intensity of an induced magnetic field may be increased, resulting in an increase in inductance.” (*Id*. at 5:25-30).
7. “In this case, since a distance between the first and second external electrodes **131** and **132** is relatively short, the current path may be reduced, resulting in a reduction in inductance.” (*Id*. at 5:35-40).
8. “As described above, the multilayer ceramic capacitor, in which the first and second external electrodes **132** are formed on the first and second side surfaces **5** and **6** of the ceramic body **110**, may be a reverse geometry capacitor (RGC), or low inductance chip capacitor (LICC).” (*Id*. at 6:4-9).
9. “Inductance of the multilayer ceramic capacitor may be reduced by controlling the length and the width of the ceramic body to satisfy $0.5L \leq W \leq L$.” (*Id*. at 6:54-56).
10. “Therefore, low inductance may be implemented in the multilayer ceramic electronic component according to the exemplary embodiment of the present disclosure, whereby electric performance may be improved.” (*Id*. at 6:54-56).

24. Thus, a POSITA would have understood that low inductance or ESL is a key objective of the '381 patent. Inductance (L or ESL) of a capacitor device contributes to the impedance (Z) of said device through the relation:

$$Z = \sqrt{ESR^2 + (X_L - X_C)^2}$$

where:

Z is impedance in Ohms (Ω)
ESR is equivalent series resistance in Ohms (Ω)
X_L is inductive reactance = $2\pi fL$ in Ohms (Ω)
X_C is capacitive reactance = ($1/(2\pi fC)$) in ohms (Ω)
f is frequency in Hertz (H)
L is inductance in Henries (H)
C is capacitance in Farad (F)

25. Additionally, the self-resonance frequency of a capacitor occurs where the capacitive and inductive reactances are equal, and is determined through the relation:

$$F_r = \frac{1}{2\pi\sqrt{LC}}$$

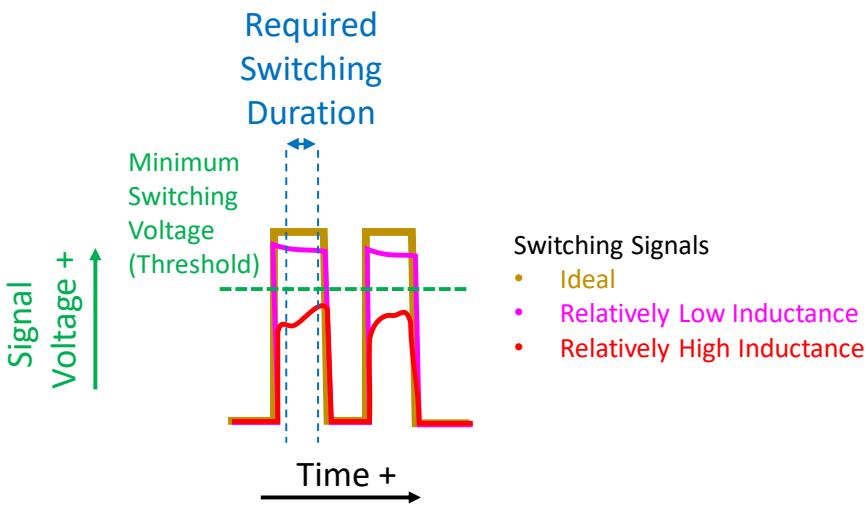
where:

F_r is self-resonance frequency (SRF) in Hertz (Hz)
L is equivalent series inductance (ESL) in Henry (H)
C is capacitance in Farads (F)

26. Above the self-resonance frequency (F_r), the inductive reactance of the capacitor device ($2\pi fL$) dominates the capacitive reactance, and the inductance

or ESL (equivalent series inductance) of the device, becomes the dominant factor in determining impedance (*Z*).

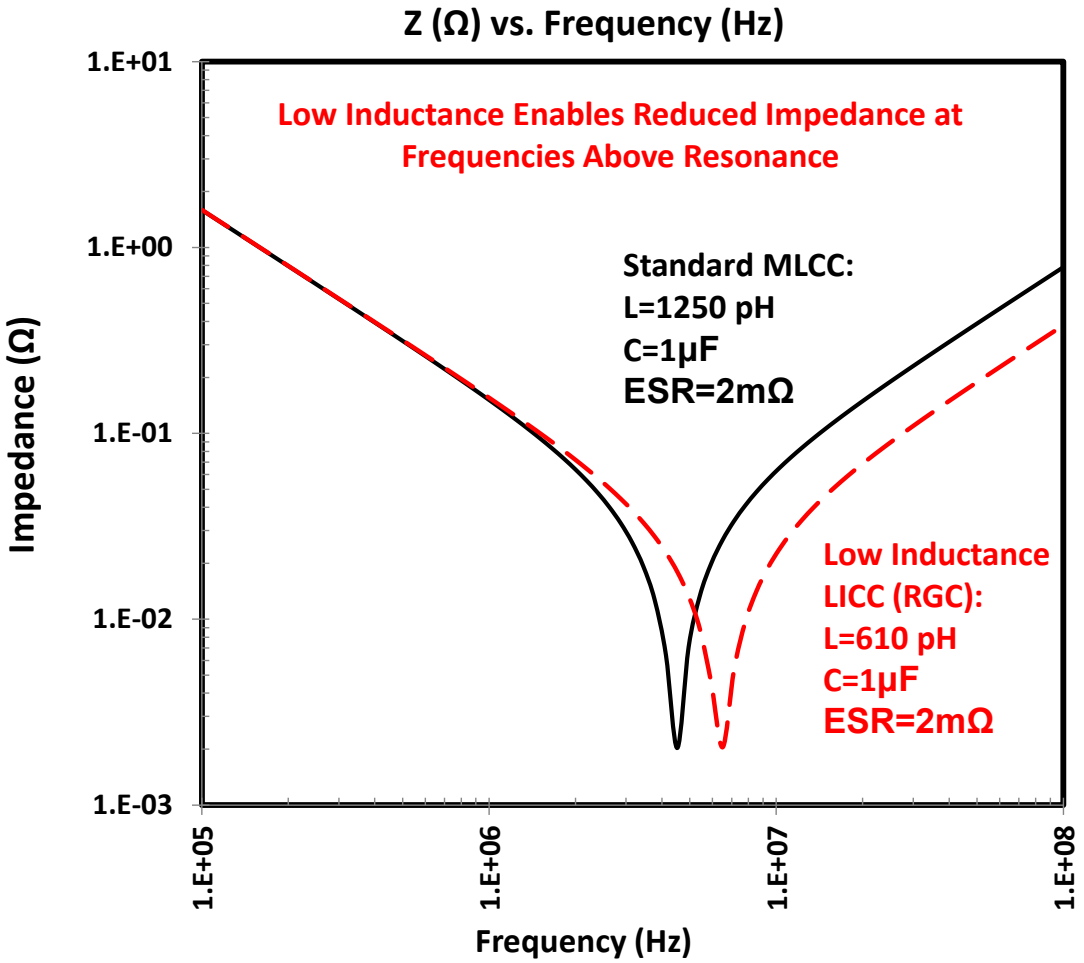
27. Low ESL (inductance) is important in applications that require low impedance (*Z*), such as decoupling, and the like, as discussed herein. In these applications low inductance results in low impedance, thus reducing "voltage droop" thereby improving signal integrity, etc., such that signals sent to each switching element in, for example, an integrated circuit (IC), are proper and are not significantly compromised by said "voltage droop," or the like. Thus switching errors are avoided as illustrated below.



- The Signal Voltage must Exceed The Switching Threshold for The Required Duration in Order for the Switching Element to Properly to Switch
- An Ideal Signal Voltage is Shown, Resulting in No Switching Errors
- Using Low Inductance MLCC, a Good (Usable) Voltage Signal is Achieved and No Switching Errors Occur
- Using MLCC With Too High of an Inductance Results in Switching Errors as Switching Threshold and/or Duration are insufficient

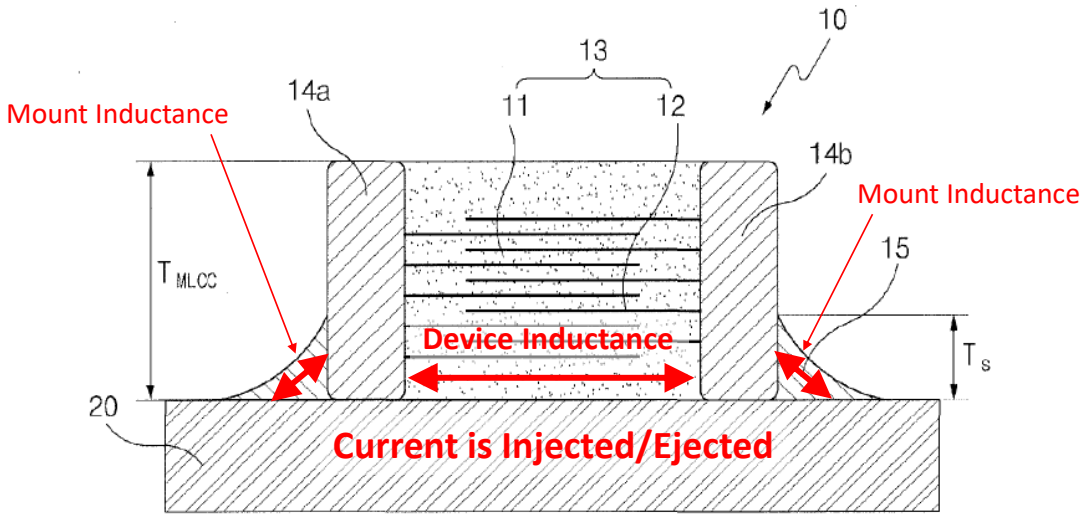
Switching with Low and High Inductance MLCC for Decoupling

28. An impedance (Z) versus frequency (f) curve of a low inductance MLCC versus a standard MLCC is shown below in order to illustrate this effect. Therefore, achieving a low inductance MLCC device is an important objective of the '381 patent.



Impedance versus Frequency for Standard MLCC Compared to Low Inductance MLCC (LICC)

29. Further, the inventors of the '381 patent realized that it is necessary but insufficient, when pursuing low inductance circuits, that the MLCC device of interest have low inductance. Since the low ESL device is connected to the circuit in a series configuration (i.e., a first connection to a first polarity and a second connection to a second polarity, which results in at least 3 parasitic inductances as illustrated below), it is important that the connections of the MLCC device to the circuit board or printed circuit board (PCB) also have low inductance, so that the entire configuration has relatively low inductance or ESL.



Inductances add together when device is connected in series (always for capacitor as it only works when polarity at each terminal is relatively opposite to the other terminal), in this case:

$$ESL_{Mounted} = ESL_{MLCC} + 2ESL_{MOUNT}$$

Inductance of each of the solder connections (2 or more) depends upon the relative cross-sectional area of the connection in combination with the length of the connection

- Short, wide, high (large cross sectional area) exhibit lower inductance
- Long, narrow, short (small cross-sectional area) exhibit higher inductance

Inductance of a Mounted MLCC (adapted from Ahn)

30. Additionally inductance or ESL has two components:

1. Self-inductance: the inductance of a conductor that is due to the magnetic field that is generated due to current flowing through the conductor itself.
2. Mutual inductance: the inductance imposed on a conductor that is due to the magnetic field that is generated by current flowing through a neighboring conductor.

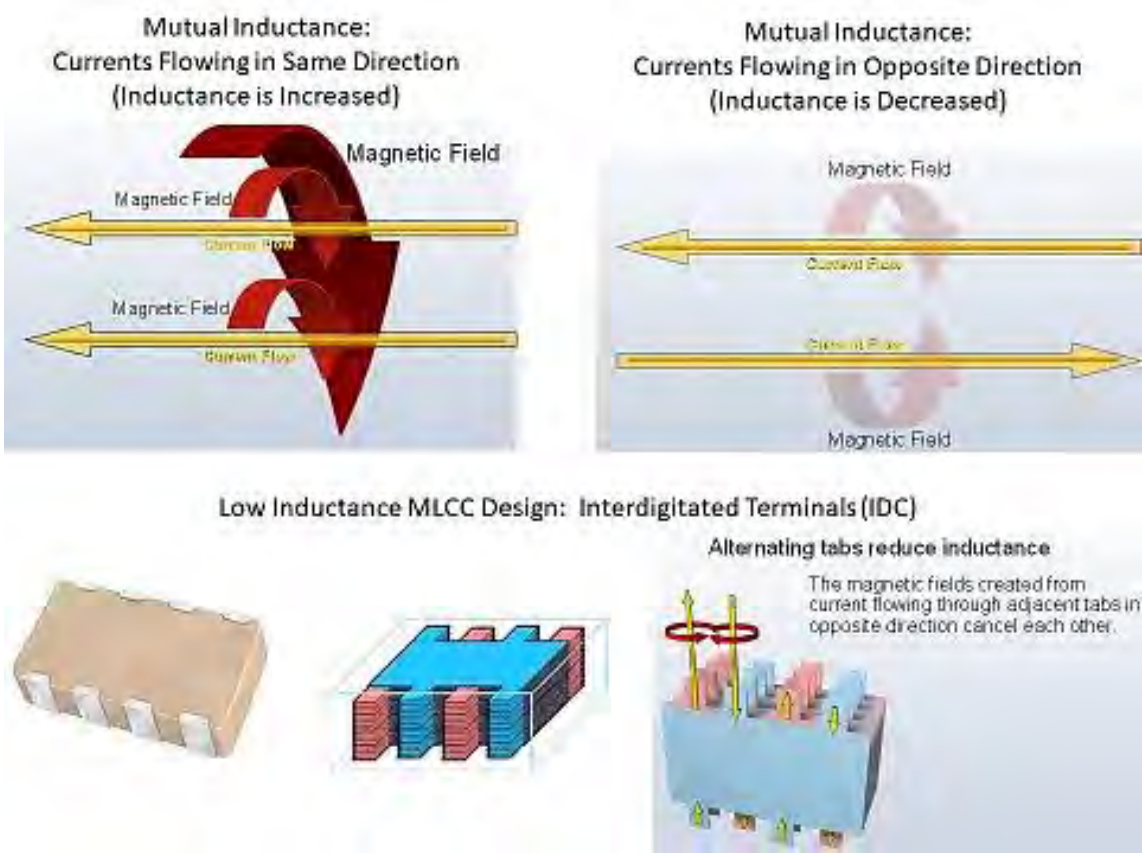
These two inductance components combine to provide an overall inductance that a conductor or component exhibits. Self-inductance is explained above, and is due to the magnetic field that develops clockwise with respect to the direction of current flow (i.e., the "Right Hand Rule"). Mutual inductance is the inductance that is impressed upon a given conductor by the magnetic field(s) of neighboring conductors. When the current in neighboring conductor(s) flows in the same direction as the current in the subject conductor, the magnetic fields are also in the same direction and combine to increase inductance as described and illustrated herein. When the current in the neighboring conductor(s) flows in the opposite direction of the conductor of interest, the magnetic fields run in counter directions and the net magnetic field is reduced, thereby reducing the overall inductance of the subject conductor.

31. Subsequently, when the current flow in a conductor of interest ceases or reverses direction, the energy stored in said magnetic field (that is due either to self-inductance or to the net combination of self and mutual inductances), resists said

change in current flow, which effectively slows down these current changes and results in "voltage droop" in the associated circuit. Thus, in inductive circuits, the current change lags the voltage change. This lag can result in highly undesirable events, such as erroneous switching events in active circuits, such as for example if a switching element in an integrated circuit (IC) does not switch when it is supposed to due to this "voltage droop" (i.e., due to insufficient switching voltage in the signal to the IC, as described above, or the like). These undesirable events occur, for example, when the associated capacitor has unacceptably high inductance (ESL) for the switching speed requirements of the circuit associated with said decoupling application. Thus, in these types of applications, lower inductance (ESL) is required and high inductance (ESL) is not acceptable. Realizing this, the inventors on the '381 patent embraced the objective of creating a low inductance MLCC device, having high capacitance density and low acoustic noise emission as explained herein. They also embraced the objective of designing the accompanying circuit board, to which said devices would be mounted, such that the benefits of low inductance and low acoustic noise emission exhibited by the MLCC device(s) are not sacrificed, but are further improved.

32. In a "nutshell," wide, thick, short conductors exhibit relatively low self-inductance, while narrow, thin, long conductors exhibit relatively high self-inductance. As discussed above, when two closely placed conductors conduct

electrical current in the same direction, the effect of mutual inductance of one conductor upon the other conductor is to increase the inductance of the other conductor. And when two closely placed conductors conduct electrical current in the opposite direction, the effect of mutual inductance of one conductor upon the other conductor is to decrease the inductance of the other conductor; the latter is used by designers and engineers, etc., to reduce inductance of ceramic capacitors by using interdigitated electrode design MLCCs, for example, as illustrated below.



Mutual Inductance: Effect on Overall Inductance

33. These same phenomena work with electrode pads or mounting pads and associated circuitry on circuit boards (PCBs) as well. Thus, placing mounting pads of the same polarity, that conduct current in the same direction into or out of a mounted component such as an MLCC, will increase the mutual component of inductance and thus the overall inductance of the mounted MLCC. A POSITA would have understood that use of this configuration ***works against*** the objective of achieving low overall inductance. Further, a POSITA would have understood that use of a plurality of spaced mounting pads and associated solder attach on a circuit board where said pads are much narrower, and/or said solder is thinner in height than a single, full width mounting pad for a terminal of the component will increase the self-inductance of each of the solder mounts between the PCB and the component (MLCC in this case). If this increase in inductance, as well as the increase in mutual inductance as described above, is not overcome by the parallel nature of the mounts, the overall inductance of the mounted component configuration will increase. Again this ***works against*** the objective of the '381 patent of achieving low overall inductance of the mounted component.

34. Thus, a POSITA would have understood that prior art that discloses narrower, thinner, multiple electrode pads or circuit traces per terminal mount, and/or that discloses thinner associated solder mount material height, and/or that are closely spaced and flow current in the same direction ***all work against*** the objectives

of the ‘381 patent (i.e., a low inductance MLCC device, having high capacitance density and low acoustic noise emission, and an accompanying circuit board, to which said devices mount, that minimizes any additional inductance or noise emission of the overall mounted configuration). Thus, a POSITA would have been dissuaded from using multiple, narrow mounting pads for one MLCC external electrode, as taught by United States Published Patent Application US2012/0152604 (Ahn) for example, as discussed in further detail below. And thus, a POSITA would have also been dissuaded from using relatively thin solder mount material between the mounted MLCC and the electrode mounting pad as is also taught in (Ahn) for example.

35. The inventors of the ‘381 patent also had the objective of reducing or minimizing acoustic noise emission of the subject MLCCs. To explain, certain dielectric materials physically distort when they are placed within an electric field. This phenomenon is due to the crystal chemistry of the dielectric comprising the MLCC as explained below, and is significant in ferroelectric type or similar type ceramic dielectrics that are used as the dielectric material in high capacitance density MLCCs, such as the subject MLCC devices of the ‘381 patent.

36. To explain, a major driving factor for the design of certain MLCCs (those that pertain to the ‘381 patent) is the amount of capacitance provided by the device, as well as the amount of capacitance exhibited by a given volume (unit

volume), called "*C/V"* and also known as the capacitance density of said capacitor device. A POSITA would have understood that, for these applications, it is important to maximize *C/V* in the subject MLCCs of the '381 patent. In an MLCC, the capacitance is determined by the relation:

$$C = \frac{n\varepsilon_0\varepsilon' A}{t}$$

where:

C is capacitance in Farads (F)
n is the number of actives within the MLCC device
ε_0 is the dielectric permittivity of free space (8.854 x 10^{-12} F/m)
ε' is the dielectric constant of the material comprising the actives
t is the thickness of each dielectric layer comprising the actives (m)

37. In order to simplify the math, the device construction of the MLCC device of interest is often simplified such the MLCC is defined to be marginless, and to have no cover layer volume, and to have no internal or external electrode volume. With these simplifications in place, the volume of the MLCC (i.e., the length x the width x the thickness) may be defined as:

$$V = LWT \propto nAt$$

where:

V is the volume of the MLCC (m^3)
L is the length of the MLCC (m)
W is the width of the MLCC (m)
T is the thickness of the MLCC (*T = n x t*)
A is the area of each of the marginless active(s) (*A = L x W*), (m^2)
n is the number of actives within the MLCC device
t is the thickness of each dielectric layer comprising the actives (m)

38. Using the above simplification, volumetric efficiency or capacitance density is equal to the capacitance divided by the volume (*C/V*). And using the above simplification leads to the relation:

$$C/V \propto \frac{n\varepsilon_0\varepsilon' A}{nAt^2} \propto \frac{\varepsilon_0\varepsilon'}{t^2} \propto \frac{1}{t^2}$$

39. Thus, a POSITA would have understood that, in order to maximize capacitance density, it is important to maximize ε' (the dielectric constant) as well as to minimize *t* (dielectric thickness), which not only increases *C*, but allows for higher *n*, thus leading to the effect that *C/V* increases proportionally to the inverse of the square of the dielectric thickness (t). For example, a POSITA would have understood that if dielectric thickness can be reduced by a factor of 10, capacitance density may be increased by as much as a factor of 100. A POSITA would have understood these factors and would understand that a major driving force in the MLCC industry is (and has been) to maximize *C/V* by increasing ε' and by decreasing *t*, thereby enabling increased *n* as well.

40. Subsequently, considerable effort has been devoted to developing dielectric ceramic materials that exhibit increased dielectric constant (ε') and that are capable of enabling very thin dielectric layers in MLCCs. Ferroelectric materials, typically comprised of formulations that include barium titanate ($BaTiO_3$ or BT) are, by far, the material of choice for these applications since the crystal

structure of BT enables very high values of ε'. Said formulations are optimized to provide acceptably and stable ε' over a broad range of temperature. For example, an X5R dielectric is designated as a Class 2 dielectric (ferroelectric or similar) that exhibits a relatively high ε' over the temperature range from -55C to +85C. In this example ε' cannot deviate more than +/-15% from the room temperature (RT) value of ε' over the temperature range from -55°C to +85°C and still achieve the X5R classification. Using BT, X5Rs exhibiting ε' values exceeding 3,000-5,000 may be achieved. This enables an increase in *C* by a factor of ~30X to ~50X when compared to MLCCs made with non-ferroelectric or similar materials (e.g., Class 1 or linear dielectric materials, which typically exhibit ε' values of ~100 or less). These ferroelectric or similar Class 2 dielectric materials, which exhibit very high dielectric constant values (ε') also are formulated and engineered to enable very thin dielectric layers as discussed below. Since these materials exhibit high dielectric constant (ε'), combined with enablement of very thin dielectric thickness (*t*), and thus high active count (*n*), these ferroelectric or similar ceramic dielectric materials, are by far, the best capacitance solution for a range of applications requiring small devices of maximized *C/V*, which are enabled solely by this technology.

41. It is important to note that none of the ferroelectric or similar ceramic dielectric materials as described above are boundary layer-type materials. It is also important to note that, due to the commercial success of the above thin layer (*t*) Class

2 type ferroelectric or similar dielectric ceramic based MLCCs, there are no commercially successful MLCCs employing boundary layer-type ceramic dielectric materials. Further, due to the success of said materials, there were no commercially successful MLCCs employing boundary layer-type dielectric materials by the time of the invention of the '381 patent either.

42. As mentioned above, these Class 2 dielectric materials, when properly formulated, engineered and processed, enable very thin dielectric thickness (i.e., to below ~1 μm). This further enables high capacitance density MLCCs as discussed above. For example, an MLCC device utilizing 1 μm thick dielectric layers could have as much as ~640 times the capacitance of an MLCC device utilizing dielectric layers that are 1 mil (25.4 μm) thick. Again, this has enabled the success of ferroelectric or similar MLCC capacitors over the past few decades relative to other types of capacitors such as IBLC dielectric MLCCs. The extent of this success, relative to certain other types of capacitors, has been so large that, for example, multilayer intergranular barrier layer capacitors (IBLCs) are not commercially viable and were not commercially available by the time of the '381 patent. Thus, a POSITA would have understood that the subject materials of the '381 patent are ferroelectric-type or similar ceramic dielectric materials that enable very thin dielectric thickness layers, not IBLC dielectrics.

43. The dramatic increase in dielectric constant (ε') exhibited by

ferroelectric or similar type ceramic dielectric materials comes with certain compromises, however. The crystal chemistry that enables very high ε' in these specialized formulations (i.e., a special type of perovskite exhibiting 4 different crystal structures over a relatively small temperature range, and at relatively low temperatures, and which are typically based upon BT), also exhibit significant electrostriction or piezoelectric response when placed within an electric field. If the field varies (such as in an alternating current (AC) signal or the like), the changing field, results in changing dimensions of the dielectric, which leads to vibration that is similar in frequency to said signal or a multiple thereof, and is also proportional in intensity to the amplitude of the signal or field placed across said dielectric.

44. If the vibrations explained above are within the audible range (i.e., ~20Hz to ~20KHz), said vibrations may be heard by humans as acoustic emissions or noise. This can be disconcerting to a user of electronic devices (i.e., cellphones, tablets, laptops, computers and the like). The intensity of the acoustic noise may be measured using a sound meter or dB (Decibel) meter or the like, where a dB (Decibel) is a unit of sound intensity and is determined through the relation:

$$I(dB) = 10 Log_{10}\left[\frac{I_i}{I_0}\right]$$

where:

I is the relative sound intensity (noise) in dB
Log_{10} is the base 10 logarithm operator
I_i is the intensity of the sound of interest
I_0 is the intensity of a reference (e.g., ambient, hearing threshold, etc.)

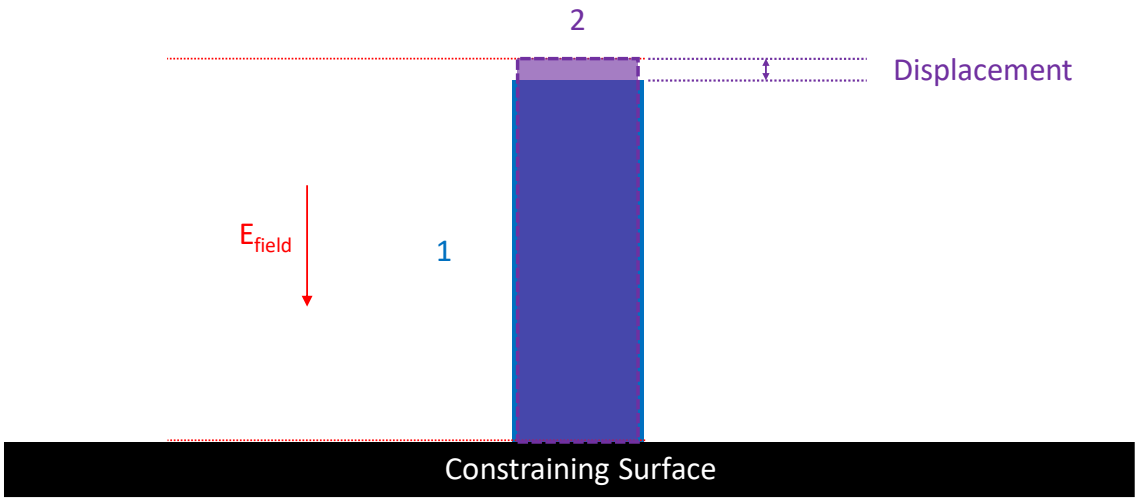
45. In general, higher intensities of noise that are in the audible frequency range are more noticeable, and thus more annoying to the device operator, and potentially to others that are in the vicinity of the emitting device. The phenomenon has been referred to as "singing capacitors"[3,4,5] and is generally undesirable. Certain factors, such as one or more of the value(s) of numerous piezoelectric or electrostrictive coefficient(s) as explained herein, the signal field intensity, shape and frequency, the number of "singing" devices "in concert", the type and design of circuit board that said devices are mounted to, and how mechanically stiff or rigid their associated mounting is to said circuit board are all important factors in determining the relative intensity (*I*) of the sound emitted from the "singing capacitors."

46. When multiple Class 2 (ferroelectric ceramic dielectric or the like) MLCCs are mounted stiffly to a circuit board (PCB) that is compliant and shaped appropriately for amplification (e.g., a large compliant plane), and an appropriate electric signal is applied, the acoustic noise that is emitted from the "singing capacitors" can be unacceptably annoying. Mitigation of acoustic emission of

[3] Ex. C: TDK, "Frequently Asked Questions Regarding: Singing Capacitors (Piezoelectric Effect)," December, 2006. https://product.tdk.com/en/contact/faq/31_singing_capacitors_piezoelectric_effect.pdf
[4] Ex. D: NIC Components Corporation, Piezoelectric Noise: "MLCC Ringing – Singing," REV. May 2015. http://www.niccomp.com/resource/files/ceramic/MLCC-Ringing-Singing-NSPH-SMT-FilmCapacitors-May2015.pdf
[5] Ex. E: KEMET Electronics Corporation, "Piezeoelectric Effects Ceramic Chip Capacitors (Singing Capacitors)," Arrow Asian Times, 2006-08, J. Prymak. http://www.kemet.com/Lists/TechnicalArticles/Attachments/88/2006%2007%20ArrowAsiaTimes%20-%20MLC%20Noise.pdf

MLCCs due to these factors has received considerable attention in the industry (see e.g., Ex. C, D, E). Thus, an objective of the invention of the '381 patent is an MLCC device exhibiting low inductance (ESL) that is achieved via reverse device geometry, that also emits low acoustic noise, has a high *C/V*, and that is reliable. Further, the '381 patent teaches how said device should be mounted so as to further mitigate undesirable acoustic noise.

47. The intensity of the acoustic noise that a single MLCC emits depends upon one or more of numerous piezoelectric coefficient(s) or electrostrictive coefficient(s) of the ceramic dielectric material used between internal electrodes of opposite polarity. For example, with regard to piezoelectric effect, in its simplest form, the piezoelectric coefficient (d) is the amount of displacement that results from the application of a given amount of electric field across the dielectric as illustrated below. Prior to the application of electric field, a piezoelectric material (shown below in blue) has a given set of dimensions. After application of an electric field (shown in purple), the piezoelectric material increases in length and is reduced in width, for example as illustrated below. The amount of displacement in length depends upon the amount of electric field applied as well as the piezoelectric coefficient (d). The coefficient (d) generally scales with the amount of polarization per unit volume that the material of interest exhibits, as does the dielectric constant ε' of said material, and materials that exhibit higher ε' also tend to exhibit higher d.

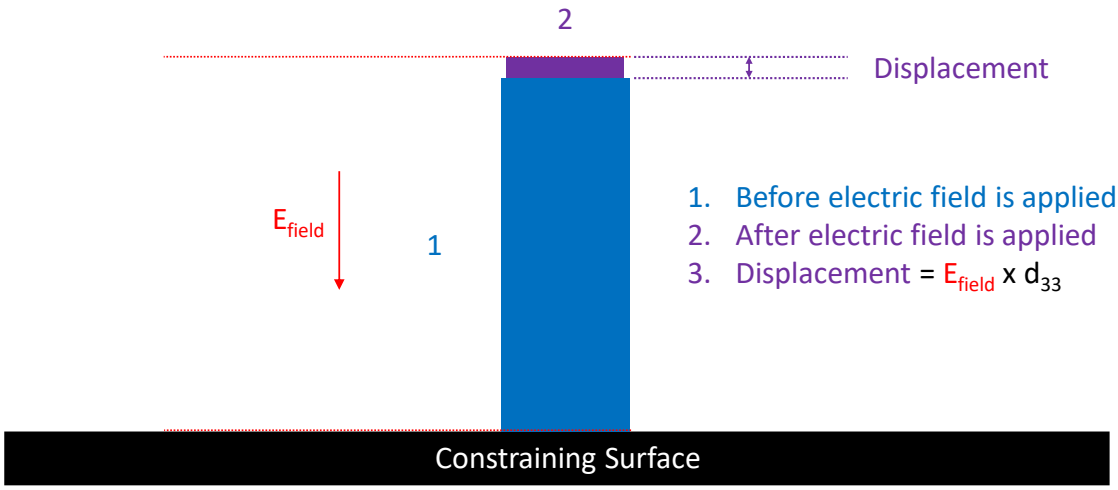


1. Before electric field is applied
2. After electric field is applied
3. Displacement = E_{field} x d (Piezoelectric Coefficient)

Basic, Simplified Piezoelectric Displacement

48. More realistically, because d depends upon a complex combination of crystal chemistry, crystallographic alignment, and crystal morphology (e.g., whether the material is single crystal or polycrystalline) of the material of interest, the piezoelectric coefficient has directionality and the d coefficient generally is specified in several directional displacements with respect to displacement as well as to the direction of the application of electric field. This results in a nomenclature for piezoelectric displacement that is generally in the form of d_{AB}, where A denotes the direction of applied electric field and B denotes the direction of induced strain by said applied field per the illustration below. For example, d_{33}, d_{31}, and d_{15} are defined

as illustrated below. Other piezoelectric coefficients are also defined in a directional manner, similar to those illustrated below.

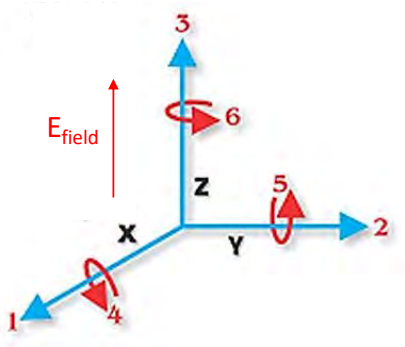


Examples

d_{33} is induced strain in direction 3 per unit electric field applied in direction 3

d_{31} is induced strain in direction 1 per unit electric field applied in direction 3

d_{15} is induced shear strain about direction 2 per unit electric field applied in direction 1



Dimensionality of the Piezoelectric Effect[6]

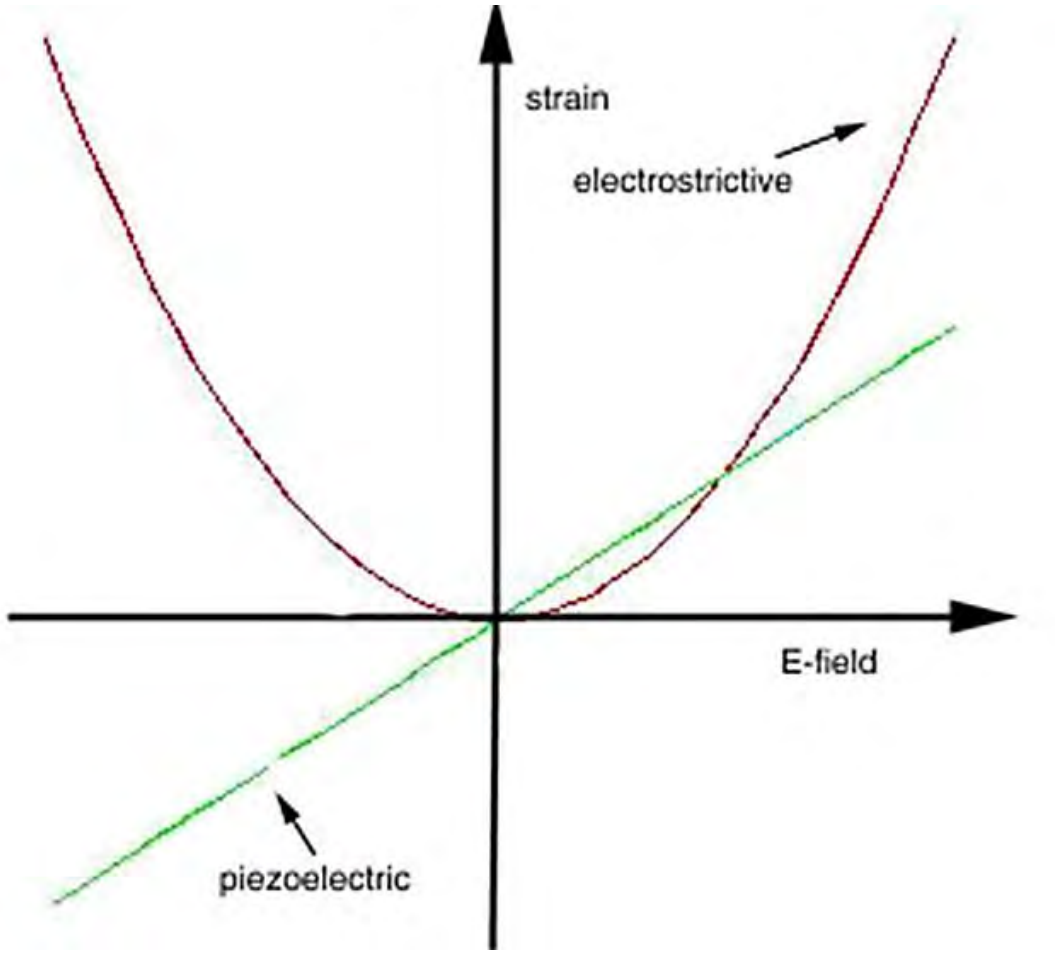
49. The d_{33} coefficient is usually the largest of the piezoelectric coefficients, and the piezoelectric effect (and thus emission of acoustic noise) is increased as d_{33} increases. Generally, d_{33} increases as all of the crystals within the grains of the polycrystalline ceramic dielectric align in the Z-direction (i.e.,

[6] Adapted with: APC International, Ltd., Knowledge Center-Piezo Theory-Piezoelectric Constants: https://www.americanpiezo.com/knowledge-center/piezo-theory/piezoelectric-constants.html

orthogonal to the applied field) within the MLCC. Thus, dielectric materials having well developed, consistent grains that are aligned in a consistent direction are generally not preferred when reduction of acoustic noise is a goal, as they tend to exhibit maximized d_{AB} (d_{33} in this case). Thus, a POSITA would have understood that, from the standpoint of piezoelectric effect, it is generally best that the ceramic dielectric within the MLCC be polycrystalline, with little or no crystallographic orientation when reduction or minimization of acoustic noise is a goal.

50. Electrostriction is somewhat analogous to piezoelectric effect in that application of electric field leads to displacement of the crystal structure in a manner that is somewhat similar to the description of the piezoelectric effect above. This again results in strain exhibited by the ceramic dielectric material. In the case of electrostriction, however, the displacement is proportional to the square of the applied electric field, as opposed to being directly proportional to the applied electric field as is characteristic of the piezoelectric effect. Also, electrostrictive effect is different from piezoelectric effect as the displacement (d or d_{AB}) coefficients for electrostrictive effect tend to be somewhat smaller than the displacement (d or d_{AB}) coefficients for the piezoelectric effect. Additionally electrostriction does not result in negative displacement, but only in positive displacement, contrary to the piezoelectric effect. Further, the displacement of electrostrictive materials occurs at twice the frequency of the applied electric signal for the electrostrictive effect, while

the piezoelectric effect occurs at the same frequency as the applied electric signal. A generic comparison of the basic longitudinal displacement of a piezoelectric material vs. an electrostrictive material as a function of applied electric field (polarization) is illustrated below.



Comparison of Electrostrictive Effect and Piezoelectric Effect: Mechanical Strain vs. Applied Electric Field[7]

[7] Ex. F: J.C. Tucker, "Actuation for Mobile Micro-Robotics," North Carolina State University, https://www.ece.ncsu.edu/erl/microrobotics/actuation/actuation.html

51. As with the piezoelectric effect, emitted noise increases as electrostriction increases, and the electrostrictive effect also tends to increase as ε' increases. Additionally, electrostrictive displacement tends also to be largest in the "33" direction as explained above, and thus generated acoustic noise is generally greatest in the direction parallel to the applied electric field (i.e., orthogonal to the electrode plates). And as with piezoelectric dielectric ceramics, materials having well developed, consistent grains are generally not preferred when reduction of electrostrictive effect and thus acoustic noise emission is a goal. And although electrostriction is a phenomenon different from piezoelectricity, it is also generally favorable, from the standpoint of electrostriction, that the ceramic dielectric within the MLCC be polycrystalline, with little or no crystallographic orientation, when reduction or minimization of acoustic noise is a goal. Thus, as with piezoelectric effect, a POSITA would have understood that, from the standpoint of electrostrictive effect, it is generally best that the ceramic dielectric within the MLCC be polycrystalline, with little or no crystallographic orientation when reduction or minimization of acoustic noise emission is a goal.

52. Thus, use of ferroelectric effect or similar dielectric materials in MLCCs leads to tradeoffs. While the very high ε' associated with the ferroelectric effect or similar materials enables very high capacitance per unit volume (C/V), and while these materials are formulated and engineered specifically for very thin (t)

dielectric layers, further enabling very high active count (n) and further enabling high C/V, these materials also exhibit significant piezoelectric or electrostrictive effect which can lead to unacceptable emission of acoustic noise in certain applications. The invention of the '381 patent is directed toward minimization of that noise emission while maintaining high C/V in a low inductance MLCC design and associated circuit board for mounting of said device(s).

53. Again it should be noted that neither piezoelectric effect nor electrostrictive effect are significant in electrolytic capacitors, or in general film electrostatic capacitors, or in Class 1 dielectric MLCCs, or in boundary layer devices such as intergranular barrier layer capacitors (IBLCs). Additionally, it should be noted that boundary layer-type capacitor devices, such as IBLCs, are generally only single layer type capacitors, as the benefit from these devices occurs only when the grain size of the material within the device is prohibitively large in comparison to the dielectric thickness (t) range that is relevant to high C/V MLCC as discussed herein. It is further important to note that boundary layer devices, such as IBLCs, do not rely upon the ferroelectric effect or similar mechanisms, but upon the space charge effect to create high ε' and thus capacitance, so they do not exhibit significant piezoelectric or electrostrictive effect, and thus do not emit significant levels of acoustic noise and thus are not relevant to the subject matter of the '381 patent. It should also be noted that, piezoelectric and electrostrictive effects that result in

significant levels of emission of acoustic noise as described above, are generally only significant in high ε' ceramic dielectric MLCCs that rely upon the ferroelectric effect or similar effect to produce the combination of high ε' while enabling small *t*, high *n*, and thus high *C/V*. (see e.g., Exs. C, D, E). Again, this combination is not demonstrated by boundary layer devices as discussed herein, and thus, these devices are not relevant to the subject matter of the '381 patent.

54. Other factors affecting the emission level of acoustic noise from high *C/V* MLCCs are design factors, such as those with regard to cover layer thickness. For example, MLCCs of the type described above, having thinner cover layers that are oriented toward the circuit board during mounting exhibit lower acoustic noise emission than those having thicker cover layers oriented toward the circuit board during mounting. Again, this is a tradeoff as use of too thin of a cover layer may adversely affect device reliability as disclosed in '381.

55. Additionally, the gap between device terminations may affect the level of emission of acoustic noise from a device. Smaller gaps tend to result in lower emitted noise. However, as the gap is reduced to relatively very small levels, the incidence of shorts may increase, indicating another tradeoff as disclosed in '381.

56. As described above, piezoelectric and/or electrostrictive effect(s) that result in vibration leading to emission of acoustic noise may be amplified by mounting one or more ferroelectric effect or similar high ε', high *C/V* capacitors to

a circuit board. The amount of amplification from mounting to the circuit board depends upon several factors, such as the number of devices mounted that experience the same signal, the location of the mounted parts with respect to the center of the circuit board, the orientation of the parts with respect to where the terminations of the device are located (i.e., on the long or short side of the MLCC device), the extent of mechanical coupling of the mounted device(s) to the circuit board (based upon the mounting conductor material and the amount or thickness of said material used, as well as upon the relative size, number and alignment of the mounting pads per mounted device). Further, the amount of acoustic noise emission may depend upon the shape and material of the circuit board to which the device(s) are mounted.

57. Realizing the factors discussed above and herein, the inventors of the '381 patent had the objective of creating a low inductance MLCC device, having high capacitance density (*C/V*) and with low acoustic noise emission. They also embraced the objective of designing the accompanying circuit board, to which said devices would be mounted, such that the benefits of low inductance and low acoustic noise emission exhibited by the MLCC device(s) are not sacrificed, but are held in check or even further improved upon.

58. Boundary layer devices that have been argued in this matter include IBLC capacitors, varistors, and positive temperature coefficient of resistance

(PTCR) thermistors. IBLCs are discussed above and are quite different from the MLCCs that are the subject matter of the '381 patent. Varistors, or variable resistors, or voltage dependent resistors, are electronic devices that are used to prevent circuit overvoltage. Varistors are typically used in a shunt configuration, connecting a voltage to ground. At normal voltages, the varistor acts as a low capacitance (*C*) value decoupling capacitor, and charges to the supply voltage of the device, providing somewhat of a voltage smoothing function. However, when a certain voltage (typically a few multiples of the design supply voltage) are experienced, the varistor begins to conduct at a much higher rate as voltage is increased (e.g., as in the case of a voltage transient or spike, or the like). This is typically known as the onset voltage or the "turn on" voltage.

59. A varistor typically conducts current as a function of voltage according to the relation:

$$I \propto KV^{\alpha}$$

where:

I is current in Amperes (A)
K is a constant based upon the ceramic type used for the varistor
α is the non-linearity coefficient (alpha value)

60. In the case of the varistor, *K* helps to establish the onset voltage, above which the varistor begins to conduct significantly. The α (alpha) value is always greater than 1 and is a figure of merit for the varistor. The higher the value of α, the

more current the varistor will conduct to ground as the supply voltage is increased, once past the onset voltage, and consequently the better the level of circuit protection.

61. When the varistor functions as a capacitor (i.e., below the onset voltage), the varistor acts as an intergranular boundary layer capacitor (IBLC). IBLCs are different from normal capacitors in that they utilize a dielectric that is characterized by semiconducting grains combined with insulating grain boundaries. This enables a relatively high dielectric constant (ε') combined with low piezoelectric and electrostrictive effect, resulting in negligible acoustic noise emission. However, these are very large grained devices, with relatively large dielectric thicknesses (t), and due to economic as well as technical limitations such as limited C/V, they are not used in place of low cost, high C/V MLCCs, such as those that are the subject matter of the '381 patent. They are also not used in place of low inductance MLCCs such as those that are the subject matter of the '381 patent. They also do not exhibit appreciable piezoelectric or electrostrictive effect, and thus are not of concern with regard to acoustic noise emission as are the MLCCs of the '381 patent.

62. Thus, a POSITA would have understood that boundary layer devices such as varistors and IBLCs are very different from standard ferroelectric or similar mechanism dielectric based MLCCs. For example, as mentioned above and herein,

neither the varistor nor the IBLC capacitor exhibit significant piezoelectric or electrostrictive effect during operation and thus these devices do not exhibit significant emissions of acoustic noise, and thus are not relevant with respect to the '381 patent.

63. PTCR thermistors are also boundary layer devices. They are important in that they may be used to provide over-temperature protection to electrical devices such as electric motors and the like. They function basically as a temperature sensitive switch and are placed in series with the device to be protected. When the temperature exceeds a certain level, the resistivity (or resistance) of the PTCR thermistor device increases dramatically (orders of magnitude), thereby limiting current to the electrical device that is overheating to the extent that the device shuts off and can no longer overheat. As the device cools back down, the resistance is reduced such that the device can turn back on. Thus, a PTCR can function as a self-resetting fuse or the like.

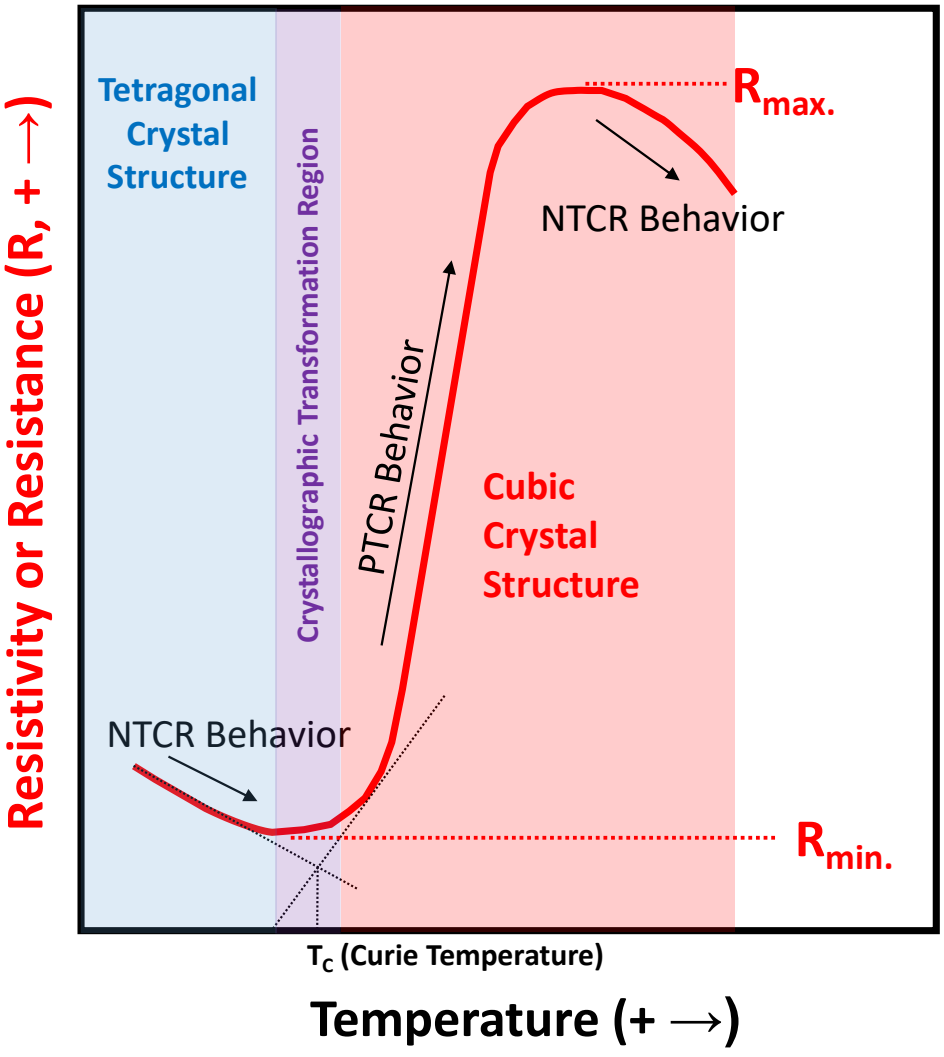
64. The material that is typically utilized to make PTCR thermistors is comprised of semiconducting grains and boundary layers at each grain, similar to a varistor. In the case of a PTCR the material used is heavily doped polycrystalline barium titanate ($BaTiO_3$ or BT) and the boundary layers are Schottky barriers which are sensitive to the dielectric constant (ε') of the semiconducting grains. Thus, this boundary layer material has the property that its resistivity begins to rise suddenly

at a certain critical temperature, which is the curie temperature of the boundary layer material. This is quite different from the insulating grains and grain boundaries that are used in high *C/V* MLCCs as disclosed in the '381 patent.

65. The Curie temperature (T_C) is the temperature at which the heavily doped BT grains, having a tetragonal crystal structure below T_C, begin to transform to a cubic crystal structure. While in its low resistivity state (i.e., at temperatures below T_C), the material comprising the device has a low resistivity (resistance). This is because the material is in its tetragonal crystal state, and the BT grains are ferroelectric, having a relatively high dielectric constant (ε'). The high dielectric constant of the BT when below T_C prevents the formation of relatively high potential barriers (Schottky barriers) between the crystal grains at the boundary layers of each of the grains. Thus, the material is in a low resistivity state below the Curie temperature (T_C). In fact, in the region below the Curie temperature the device has a small and negative temperature coefficient (NTC) or resistivity that is typical of a semiconductor material, as illustrated below.

66. At and above T_C, the crystal structure of the heavily doped BT begins to change from tetragonal to cubic and the dielectric constant (ε') drops significantly, thus resulting in the formation of a high level of potential barriers (Schottky barriers) at the boundary layers on the periphery of each grain. Subsequently, the resistivity (or resistance) increases sharply with increasing temperature (e.g., several orders of

magnitude per 10ºC temperature increase) after the Curie temperature (T_C) is exceeded. At temperatures that are well beyond the Curie temperature, the material reverts back to NTC-like behavior typical of a semiconductor, albeit at a higher base resistivity.

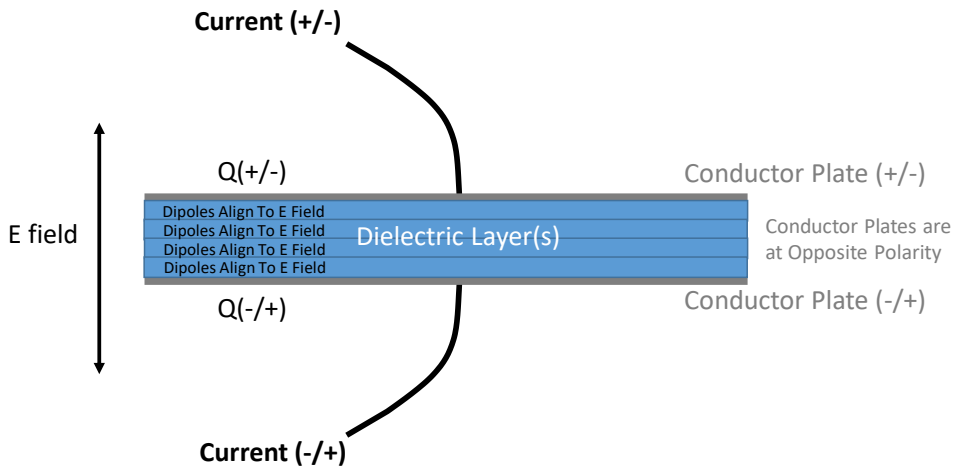


PTCR Resistance vs. Temperature[8]

[8] Adapted from: Sensors and Transducers, All About It, Thermistors: https://sensorsandtransducers.wordpress.com/2012/02/07/thermistors/

As is evident from the discussion above, PTCR devices are boundary layer devices that are not capacitors and thus are not relevant to the '381 patent as they are not relevant to the objective of the '381 patent (i.e., a low inductance MLCC device, having high capacitance density and low acoustic noise emission, and an accompanying circuit board, to which said devices can be mounted, that maintains or furthers the benefits of low inductance and low acoustic noise emission exhibited by said MLCC device(s)).

67. With regard to an electrostatic capacitor, a dielectric layer is one or more layers of dielectric material that is placed between two conductor plates that are capable of opposite polarities. The electric field that is generated between the conductor plates of opposite polarity is used to store energy in the form of charge as illustrated below. The illustration shows that the relative amount of charge that may be stored per unit of electrical potential between the conductor plates (V) increases as the capacitance of the device increases. As discussed in detail above, the capacitance increases as the dielectric constant (ε') of the material that comprises the dielectric layer, or as the dielectric constant(s) (ε') of the material(s) that comprise each of the multiple single dielectric layers that combine to achieve said dielectric layer between the conductor plates is/are increased.



- When conductor plates are at opposite polarity, an electric field (E field) forms
  - Dipoles within the dielectric layer(s) align with the E field, binding charge to the conductor plates
  - Electrical energy (E) is stored in the form of charge (Q): $Q=CV$, $E=1/2(CV)^2=1/2Q^2$
    - Q=Stored Charge (Coulombs)
    - C=Device Capacitance (Farads), increases as the number of operant dipoles per unit volume increases, increases as dielectric constant (ε') increases
    - V=Voltage (Volts)
  - The stored energy is released as the E field is reversed

Electrostatic Capacitor

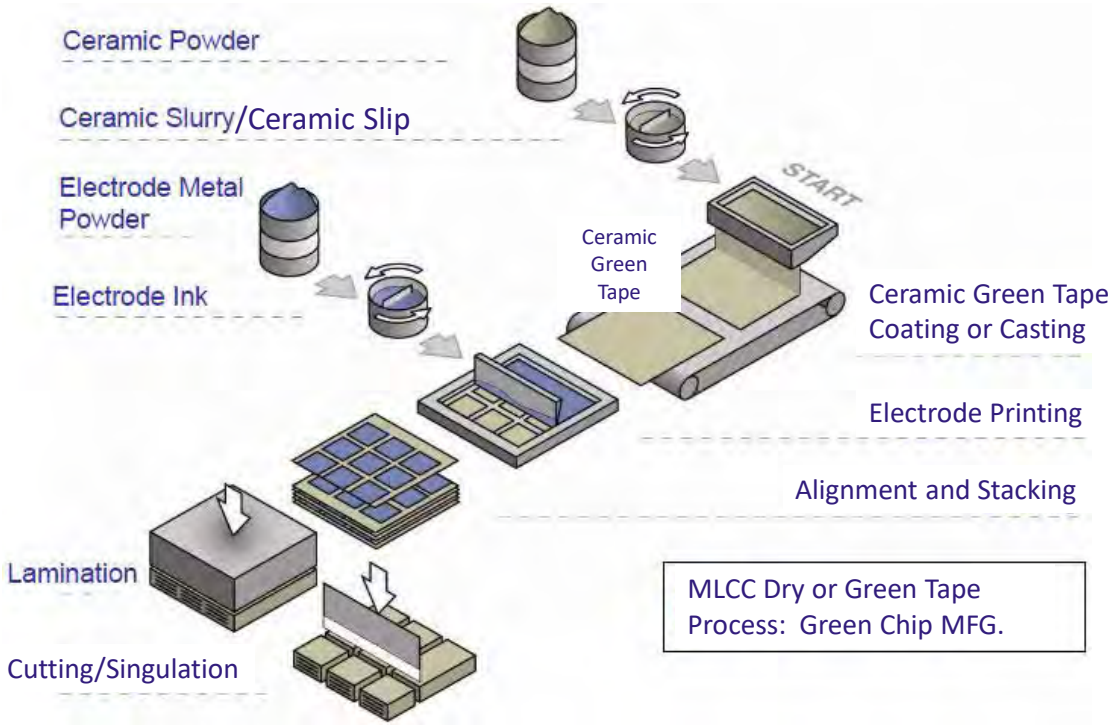
68. As shown above, the dielectric material between the conductor plates may be comprised of more than one layer or stratum. A POSITA would have understood that multiple single dielectric layers (i.e., strata) are sometimes used between conductor plates for numerous purposes, such as to increase the dielectric breakdown voltage of the device, or to reduce the incidence of shorting between the conductive plates or the like.

69. In an electrostatic capacitor, the placement or deposition of multiple single dielectric layers between conductor plates is enabled using standard MLCC

fabrication technology. Said technology is usually accomplished either by way of a dry (green tape) process, or by a wet build up process. Either method enables multiple single dielectric layers (i.e., several stratum) within a dielectric layer or strata as detailed below.

70. The green chip processing portion of the green tape process is illustrated below and involves first batching of ceramic powders, then mixing said powders with additives and dispersing the powders and additives in a liquid medium to form a suspension. The suspension of ceramic powders and additives is then milled in order to further disperse the powder particles as well as to comminute said powders to the appropriate particle size. Once a satisfactory dispersion is achieved having the appropriate particle size, the dispersion or slurry is transformed into a material called slip by adding binder and other additives to said dispersion or slurry so as to achieve the appropriate rheology, surface tension and materials properties for coating the slip onto a carrier. The slip is then further processed and then cast or coated onto a carrier, then dried to achieve green tape. In the case of thicker green tape (i.e., green tape thickness of greater than ~0.5mils or ~12.5μm), the ceramic green tape may be removed from the carrier for further processing, and is thus called free standing tape. In the case of thinner green tape (i.e., green tape thickness less than ~0.5mils or ~12.5μm), the ceramic green tape is coated onto a disposable carrier and stays on the carrier until removed later in the process as it is not mechanically

strong enough to be processed further without said carrier in contrast to free standing tape. After the green ceramic tape is produced, it is a thin, continuous, supple film.



Dry (Ceramic Green Tape) Green Chip MLCC Manufacturing Process[9]

71. Next the green tape is printed with an electrode ink in a precisely patterned and metered fashion, typically by a screen printing process. The electrode ink is comprised of metallic powder particles that are dispersed in a solvent with organic binders and other materials. The solvent is carefully selected in order to not dissolve the binder in the ceramic green tape or otherwise damage said tape. After

[9] Adapted from: Johanson Dielectrics, Basics of Ceramic Chip Capacitors, J. Maxwell, 12/2007. http://www.johansondielectrics.com/basics-of-ceramic-chip-capacitors

printing, the electrode ink is dried.

72. After the electrode ink printing process, the printed ceramic green sheets are then aligned, stacked and laminated under high pressure as well as moderately increased temperature in order to create a laminated green pad. During this process, unprinted ceramic green tape layers may be placed between printed ceramic green tape layers to achieve multiple single dielectric layers between each set of electrodes. These layers may be coated with one or more additional binder layers in order to promote adhesion, or to impede or prevent grain growth, etc., between single dielectric layers (stratum). However, this practice is typically avoided as it leads to further cost and complication of the process, and also may lead to cracking in the resulting device, leading to device failure or other compromises in device reliability as discussed below.

73. Also during the alignment, stacking and lamination process, multiple single layers (stratum) of ceramic green sheet are added to the top and bottom of the laminated pad in order to fabricate the top and bottom cover layers (strata). Again, these layers may be coated with one or more additional binder layers in order to promote adhesion, or to impede or prevent grain growth, etc., between single dielectric layers (stratum). Again, this practice is typically avoided as it leads to further cost and complication of the process, and also may lead to knit lines between each of the single dielectric layers that are placed between each electrode pair which

may lead to cracking, thereby compromising device reliability.

74. As a result of the lamination process, each ceramic green tape layer, and each printed ceramic green tape layer in the "build up" is compressed in the Z-axis or thickness direction. The amount of compression for thin dielectric layer applications is generally ca. 25% - 45% in the thickness or Z-axis direction.

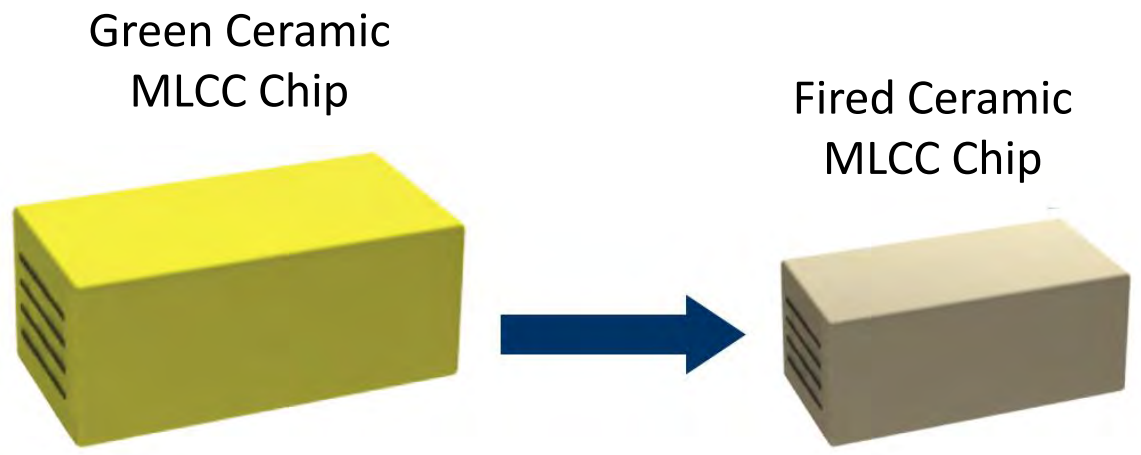
75. The resulting output of this portion of the green chip process is a pad or bar of precisely aligned stacked and laminated green ceramic sheets (some printed, some not printed), that is typically on the order of about 8" x 8" in size. The pad or bar is also affixed to a carrier plate that is typically made of metal or glass.

76. The laminated pad or bar on carrier plate, is then singulated into multilayer ceramic green chips using a precisely aligned dicing blade. The dicing blade may be a saw blade, or a guillotine type blade or other suitable singulation method. From the laminated pad or bar, tens of thousands of individual ceramic green chips may be created, depending upon the size of each individual green ceramic chip. The singulated chips are then released from the carrier plate and the individual ceramic green chips are sent to thermal processing.

77. After green chip processing is complete, the singulated ceramic green chips are then thermal processed. The first step of thermal processing is to "burn out" or remove the organic materials present in each green chip. This is done at relatively low temperatures for relatively long times.

78. The burned out MLCC chips are then fired at higher temperature in order to sinter the particles together, thereby densifying the packed particles within each burned out chip into a dense structure, having ceramic grains of the appropriate chemistry, crystal chemistry, and size.

79. The effect of the firing or sintering process is to shrink the exterior dimensions of the MLCC chip as illustrated below. During this process, the metallic particles in the electrode ink also densify into a continuous, patterned conductor to form the internal electrodes of each MLCC device.



Green vs. Fired MLCC Chips

80. Additional heat treatment may be used to grow the densified ceramic grains in order to achieve preferred properties, such as increased dielectric constant (ε') and commensurate crystallographic orientation, but this is generally avoided as

it is generally preferable to keep grain size small in very thin dielectric layer MLCCs so as to enable thin (ca. 1 μm) dielectric layers (*t*), which enable high active counts (*n*) and high *C/V* as described above and as disclosed in the '381 patent.

81. As mentioned above, during the firing stage of thermal processing, each green MLCC chip shrinks as the powder particles that comprise said chip sinter together. The firing stage may be separated into several sub-stages, known as the stages of sintering. During these stages, the heat from the atmosphere of the furnace imparts thermal energy to the packed particles.

82. In the initial stage of sintering the packed particles first react to "neck" together without densification. In the intermediate stages of sintering, densification begins as the mass transport mechanisms from the interior of each particle begin to dominate the process, so as to further reduce surface energy, transforming the green structure to a densified structure. Additionally, the pores existing within the material start to take a more circular shape and begin to close off, isolating each pore, one from another.

83. At the end of the final stage of sintering, the material has fully densified and pores have completely closed off and have been mostly, if not completely, removed. At this point, the sintering (densification) process is complete and the device has been reduced in dimension approximately 15%-25% in each linear dimension, compared to the green chip state (i.e., a volume % reduction of ca. 39V%

- 58V% from green MLCC to fired MLCC).

84. Combining the shrinkage of the green ceramic tape in the thickness or Z-axis direction with the shrinkage of the ceramic in all dimensions during thermal processing, the green ceramic tape shrinks ca. 35% - 60% in the thickness or Z-axis direction throughout the entire process (i.e., from green ceramic tape fabrication, through lamination and through thermal processing) during the manufacture of thin dielectric layer MLCCs such as those disclosed in the '381 patent. Thus, a POSITA would have understood that an MLCC, made with ca. 2 μm ceramic green tape, and having a single ceramic green tape layer (stratum) between each set of opposing internal electrodes, would result in a final dielectric thickness (*t*) of ca. 1 μm.

85. After firing, the densified MLCC chips may be subjected to a reoxidation heat treatment at significantly lower temperature than the firing temperature in order to increase the insulation resistance of the ceramic dielectric comprising the MLCC. This is typically reserved for MLCCs having base metal internal electrodes (BME MLCC) as they are typically fired in a reducing atmosphere in order to prevent oxidation of the base metal internal electrodes during thermal processing.

86. After firing, the densified ceramic chips are corner rounded, then finished, typically by standard termination and plating processes. The termination process typically involves precisely dipping of each of the edges of the MLCC

having exposed internal electrodes, into a precisely metered thick film or termination paste.

87. The termination paste is typically comprised of a relatively large amount of metal conductor particles (such as Silver or Copper) in sphere and/or flake particulate form. The termination paste also includes a small amount of glass and/or other bonding agent, as well as other inorganic additives, as well as select organic materials; such as binder, film former, resin, solvent, and the like.

88. The MLCC chip is precisely aligned in a fixture, and is then dipped into the metered termination paste. The paste is then dried onto the chip, and the chip is realigned and the termination is deposited onto the second edge of the chip having exposed internal electrodes, in the same manner as above. The chips are then termination fired in a termination kiln, typically at temperature and time that are significantly lower than the firing temperature and time for the MLCC chips.

89. The terminated MLCCs are then finished. This is typically done by applying two conductive metal coatings; one to provide a barrier layer against dissolution by molten solder during the surface mount solder reflow and/or wave solder or similar processes, and the second layer is typically a highly solderable layer, that is also relatively unreactive to the atmosphere. The purpose of the second layer is to impart solderability to the outside surface of the termination of the finished MLCC for a relatively long duration (e.g., typically 18 months or more), thereby

imparting an acceptable shelf life to the finished MLCC.

90. Chip finishing is typically accomplished using barrel plating, medialess plating or a combination or the like. One or more of these methods are generally used to deposit the plated finish layers onto the fired termination in order to finish the MLCC. As discussed above, typically (but not always) two plated layers are used. As discussed above, the interior finish layer (typically a Nickel-based layer) is usually used as a barrier layer that prevents molten solder from dissolving the termination during the solder attach process that is typically used to attach the MLCC to the circuit board or PCB. The exterior finish layer (typically Tin-based or Lead/Tin-based) is usually used so as to be a relatively stable finish, with respect to storage environment, that promotes and preserves solderability of the finished MLCC part over an acceptably long period of time (e.g., ca. 18+ months shelf life).

91. The finished chips are typically then inspected and tested, then packaged, typically in tape and reel type packaging, and are then ready for shipment to the customer.

92. The wet green ceramic chip build up process is similar to the dry process, described above, with the exception that green tape is not utilized in the wet process. During the wet build up process, the ceramic slip is wet deposited onto a previously deposited and dried layer using a doctor blade, or similar method. This method is advantageous since no carrier film is used.

93. Depending upon the design, each wet deposited, then dried ceramic green layer may then be printed with an internal electrode ink. The cover layer portions of the build are typically are not printed with electrode ink between layers, while the active portion is generally printed with internal electrode ink between each deposited and dried ceramic green layer or a multiple thereof. Each printed internal electrode ink layer is also dried prior to deposition of the next layer (ceramic green layer) upon the green "build up."

94. As with the ceramic green tape or dry process, multiple green ceramic layers (strata) may be deposited, then dried between each electrode print in order to form a multi-stratum dielectric layer.

95. However, the wet green chip build up method is disadvantaged in that it is typically not used for fired dielectric thickness (*t*) less than ca. 4 μm. This is because the incidence of shorting between internal electrodes, and poor device reliability increases when fired dielectric thickness (*t*) is less than ca. 4 μm. Thus, yield and reliability issues become prohibitive at these thicknesses and below. The reason for this is that it is not possible to pre-inspect prints or dielectric layers prior to the green chip build up process using the wet process. Therefore, defective layers are not removed from the build. Additionally, degradation of the base substrate (i.e., the previous layer of dried green ceramic and/or dried printed internal electrode ink) may occur throughout the build, resulting in fatal flaws (e.g., shorts, etc.) to the

resulting MLCCs at an unacceptably high level when thin dielectric layer designs are pursued.

96. The wet build up method is further disadvantaged in that the drying process is incorporated into the green chip build up process, thereby increasing build up time. For these reasons, the wet build up process is generally not used for manufacture of MLCCs having very thin (i.e., ca. 1 μm) fired dielectric thickness (*t*) or for the manufacture of MLCCs having very high (i.e., ca. 200++) active counts (*n*), both of which are disclosed as key elements of the high *C/V* MLCCs of the '381 patent.

97. As with the dry ceramic green tape process, the wet build-up process enables the use of multiple single layers (stratum) between each set of electrode layers. To do this, multiple wet dielectric passes (i.e., deposit, then dry, then deposit, then dry…) are made between each electrode print and dry. As with the ceramic green tape process, these additional individual ceramic dielectric layers may also be coated with one or more additional binder layers in order to promote adhesion, or to impede or prevent grain growth, etc., between each single dielectric layer (stratum). However, as with the dry green tape process, this practice is typically avoided as it leads to further cost and complication of the process, and also may lead to knit lines between each of the single dielectric layers that are placed between each electrode pair, and which may become cracks, thereby compromising device reliability.

98. Further, during the wet build up process, multiple single layers (stratum) of green ceramic dielectric are also added to the top and bottom of the wet build up or pad in order to fabricate the top and bottom cover layers (strata). Again, each of these single dielectric layers (stratum) may be coated with one or more additional binder layers in order to promote adhesion, or to impede or prevent grain growth, etc., between single dielectric layers (stratum). Again, this practice is typically avoided, as it leads to further cost and complication of the process, and also may lead to knit lines between each of the single dielectric layers which may become cracks, thereby compromising device reliability.

99. Once the wet build-up pad is fabricated, the multiple green chip containing pad is then singulated into green ceramic MLCC chips, then subjected to thermal processing (i.e., burnout, firing and possibly re-oxidation), then corner rounding, termination and chip finishing, in a manner similar to that described above for ceramic dielectric MLCC chips manufactured via the dry tape process.

B. U.S. Patent 9,326,381 ('381)

100. United States Patent 9,326,381 (the '381 patent) having inventors B.H. Lee, et al., and assigned to Samsung Electro-Mechanics Co. Ltd., (SEM) is directed toward a "multilayer ceramic capacitor" (MLCC) with specified dimensions (external and internal) in order to reduce acoustic noise resulting from vibration of

the low ESL, high *C/V* MLCC device, as a result of one or more of piezoelectric or electrostrictive effects that occurs when an electric field is placed across electrode pairs of opposite polarity. (*Id*. 1:32-53, 1:60-3:34, 4:34-41, 6:24-49, 6:61-7:7, 7:13-41, 9:11-12:67).

101. As described above, when an electrical signal, such as an AC (alternating current) signal, is induced across electrodes of opposite polarity, the ferroelectric (or similar) dielectric material used in the MLCCs taught in the '381 patent expand and contract as the signal changes. This is due to one or more of the piezoelectric or electrostrictive properties of the dielectric material used to form the active layer of the device, and causes the MLCCs taught in the '381 patent to vibrate and create pressure waves in the air. As discussed above, if that vibration is within the audible range, it will result in the emission of sound or acoustic noise. The emission gets more intense as the signal strength is increased.

102. An objective of the '381 patent is to reduce or minimize said acoustic emissions in low ESL, high *C/V* MLCC devices made with ferroelectric type or similar materials that exhibit piezoelectric and/or electrostrictive effect(s) or the like, through application of the device design principals taught in said patent. Additionally, the '381 patent pertains to said MLCC devices that are mounted on a circuit board or PCB, having specified characteristics, so as to limit or reduce emitted acoustic noise as well. (*Id*. at 13:1-29). The '381 patent discloses that said vibrations

may be transferred to the circuit board or PCB on which the multilayer ceramic capacitor is mounted, by mechanical coupling through the solder used to mount said device in a manner such that the entire printed circuit board may become an acoustic reflection surface to transmit the sound of vibrations as noise. (*Id*. at 1:42-46).

103. Importantly, the '381 patent differentiates a "single layer," from a "layer" in that the layer may be comprised of multiple single layers. For example, the '381 patent mentions an active layer portion of the MLCC numerous times where the active layer is clearly comprised of multiple active single layers (see e.g., *Id*. at 2:46-51, 4:23-30, 6:14-18, Figs. 2-4). Additionally, a POSITA would have understood that the '381 patent describes cover layers that are comprised of multiple single ceramic green tape or green sheet layers. Further the '381 patent equates each single ceramic green sheet layer with a single dielectric layer, either in a cover layer or in the active layer of the device: (see e.g., *Id*. at 8:27-29, 8:52-59, 9:11-12:67).

> "In the method of manufacturing the multilayer ceramic capacitor according to the exemplary embodiment of the present disclosure, first, slurry containing powder such as barium titanate ($BaTiO_3$) powder, or the like, may be applied to carrier films and dried to prepare a plurality of ceramic green sheets, thereby forming dielectric layers." (*Id*. at 8:9-14).

104. Thus, a POSITA would have understood that use of the terminology "single dielectric layer" in the '381 patent has a meaning that is different from the terminology "dielectric layer" in the '381 patent. For example, each time that the

average number of ceramic grains across a dielectric layer is mentioned in the '381 patent, the measure is specified as the average number of dielectric grains across a "single dielectric layer." (*Id*. at Abstract, 2:12-14, 2:61-63, 4:39-41, 7:13-16, 7:16-19, 7:19-22, 7:39-41, 7:41-45, 7:57-59, claims 1-19).

105. From the intrinsic record, a POSITA would have understood that there is an important difference between "single dielectric layer" and "dielectric layer." A POSITA would have understood that the dielectric layer interposed between the first and second electrodes in the MLCC, as disclosed in the '381 patent, is comprised of one or more single dielectric layers. (see e.g., *Id*. at 1:32-36, 1:65-2:1, 2:47-51, 4:25-27, 5:13-16, 6:15-18, claims 1-19). The '381 patent distinguishes between a single dielectric layer (or green tape layer or stratum) and a dielectric layer which is comprised of one or more single dielectric layers. Any other interpretation would not make sense to a POSITA.

106. Further, a clear aspect of the invention of the '381 patent is "***an average number of dielectric grains in a <u>single dielectric layer</u> in a thickness direction thereof is 2 or greater***" (see e.g., *Id*. at Abstract, 2:12-14, 2:61-63, 4:39-41, 7:13-16, 7:17-20, claims 1-19, emphasis added). Thus, a POSITA would have understood that an aspect of the invention of the '381 patent is an average of at least two or more dielectric grains across each single dielectric layer (stratum) in the thickness direction of said each single dielectric layer (stratum).

C. U.S. Patent 7,808,770 (Itamura)

107. United States Patent 7,808,770 having inventors Itamura, et al., and assigned to Murata Manufacturing, Co., Ltd., (Itamura) pertains to monolithic ceramic capacitors having reverse LW geometry, as described herein, so as to achieve low inductance or ESL. Further, the devices of the invention of Itamura have external terminal electrodes that include a resistor component so as to increase the equivalent series resistance (ESR) of said MLCCs, while not adversely affecting the low inductance (ESL) of the reverse LW geometry design of said disclosed MLCCs. (*Id*. at Abstract, 1:5-9, 2:1-3, 2:9-39, 5:64-6:3).

108. The devices disclosed in Itamura are low inductance MLCC devices having elevated ESR. A POSITA would understand that use of any modifications to the MLCC of Itamura, or to the mounting pads on the circuit board to which said MLCC devices mount, that increases the inductance or ESL of the mounted configuration, would work against Itamura's objective of low inductance.

109. Itamura's MLCC is otherwise a standard multilayer ceramic capacitor (MLCC). Itamura also makes no mention of the average number of grains in a single dielectric layer in the thickness direction.

D. U.S. Patent 5,134,540 (Rutt)

110. United States Patent 5,134,540, having inventor T. Rutt and being

assigned to AVX Corporation (Rutt), pertains to varistors (e.g., see *Id*. at title, abstract, and numerous references throughout specification), intergranular barrier layer capacitors (IBLCs), (*Id.* at 1:14-16, 2:35-41, 10:8-15) or positive temperature coefficient of resistance (PTCR) thermistors (*Id*. at 10:16-22). These devices were all known to a POSITA as boundary layer devices, and are different from the MLCC devices taught in Itamura as discussed below and herein.

111. As described herein, boundary layer devices are devices wherein the ceramic dielectric used is typically a two phase structure comprised of semiconducting grains and insulating boundary regions at the periphery of each ceramic grain. In the case of a varistor, the semiconducting grains are typically zinc oxide (ZnO) and the insulating boundary layers are typically comprised of bismuth oxide or more complex compounds that segregate to the boundary region during thermal processing (firing to achieve density, then firing to achieve grain growth and segregation of said insulating materials to said grain boundary regions). These boundary regions are formed so as to enable the appropriate onset or "turn on" voltage range for the device of interest. The number of boundaries across the thickness of the active portion of the device establishes the onset or "turn on" voltage for the entire device. Since varistors are not used as high *C/V* MLCC they are not relevant to the scope of the '381 patent as discussed herein.

112. In the case of an IBLC (intergranular barrier layer capacitor),

semiconducting grains are used to enable conduction of conducting species within each grain. The conducting species are kept from moving from grain to grain by insulating boundary regions that are formed around the periphery of each grain similar to the method described for varistors above. Since this is a relatively effective polarization mechanism, a high dielectric constant (ε') may be achieved.

113. However, this mechanism is effective only at relatively low frequencies and since it requires relatively very large grains to be effective, it typically is not used to make high *C/V* MLCC as explained herein as the dielectric layers in these high *C/V* devices are typically too thin to accommodate the large grains required for barrier layer devices.

114. PTCR thermistors are also boundary layer devices as described in detail above. Again, they are typically comprised of semiconducting grains having insulating boundary regions around the periphery of each grain that can be, in effect, turned on when a certain temperature (e.g., T_C) is exceeded. In these devices, the ceramic formulation and thermal process are carefully optimized in order to control the semiconductor properties of the grains and the insulating properties of the switchable boundary layer regions at the periphery of each grain. PTCR thermistors are not used as capacitors and are not pertinent to the scope of the '381 patent.

115. For the above reasons, a POSITA would be dissuaded from combining the teachings of Rutt with any other references to achieve the disclosed devices of

the ‘381 patent.

116. The Rutt patent teaches the use of multiple single green layers of ceramic material, each a stratum, to make a combined ceramic layer (strata) that may act as a dielectric layer when placed between electrodes of opposite polarity. Rutt teaches the use of at least two single dielectric layers or strata of material per dielectric layer in all cases. (see e.g., *Id*. at Abstract, 2:42-3:20, 4:27-41, 5:4-10, Examples I-VI, claims 1-4).

117. Further, Rutt teaches that each stratum must be separated by a boundary layer which resists grain growth across the boundary between each respective stratum. (see e.g., *Id*. at Abstract, 2:42-60, 5:4-10, 5:21-23, Examples I-VI, Fig. 2). Said boundary may be comprised of an organic material, such as an organic binder or the like that is removed during thermal processing, but leaves an artifact boundary that prohibits grain growth between strata (see e.g., *Id*. at 2:42-3:20, Fig. 2, and Examples I-IV, and VI), or the boundary may be comprised of a nonvolatile chemistry such as lanthanum carbonate, or other, at least a portion of which remains as part of the final device (see e.g., *Id*. at Example V, 10:37-40).

118. Rutt teaches that each stratum is essentially discrete due to the applied boundary layer (see e.g., *Id*. at 3:7-14, Fig. 2: 30A-E and 31A-D). Rutt explains that “The invention is predicated in large measure on the discovery that ceramic grain growth is inhibited by the higher binder concentrations present at the upper surface

of a green ceramic tape or stratum" (*Id*. at 2:42-45). A POSITA would have understood such binder concentrations on the upper surface of a ceramic tape or stratum to be a result of binder segregation (see e.g., 5:49-55), and that insufficient binder segregation will not effectively inhibit grain growth across a boundary between two strata (see e.g., *Id.* at 9:2-4, 9:8-10). A POSITA also would have understood that this amount of binder segregation required to inhibit grain growth between strata would result in "knit lines" or "light dielectric" in the final fired multilayer ceramic structure as explained herein. Also as explained herein, such an amount of binder segregation can result in cracks in the device that result in device failure.

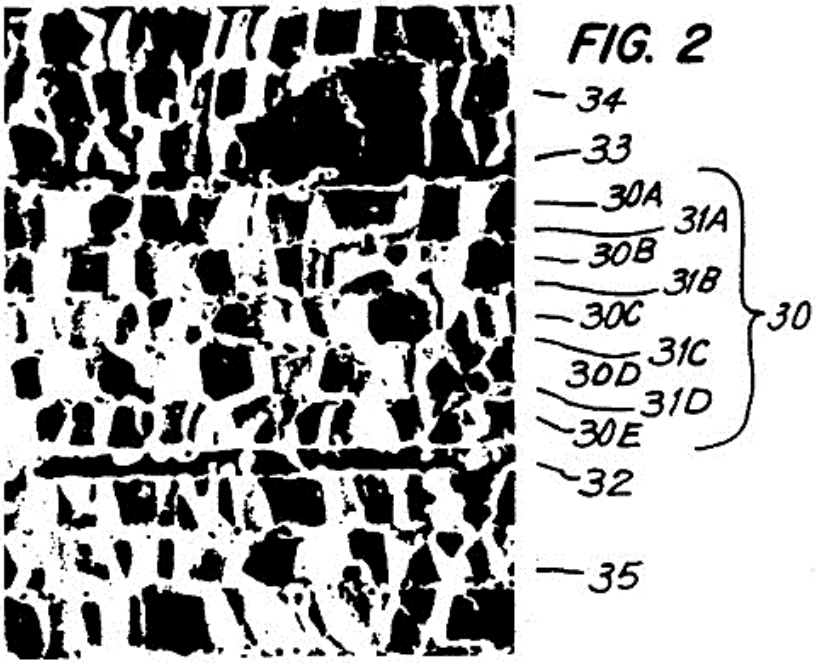
119. Additionally, the device fabrication process of Rutt, while similar, is much more complex than traditional MLCC fabrication processes. For example, Rutt requires as many as 5 or more strata per dielectric layer. In the case of 5 strata per dielectric layer or composite layer, this would increase green build up time by approximately 5 fold or more.

120. Further, Rutt requires the application of a barrier material between each stratum that is combined with at least one additional single dielectric layer or stratum to comprise each dielectric layer (i.e., composite of strata or single dielectric layers). Again, this would add greatly to the green build up time. Additionally, 5 times the amount of tape would need to be manufactured per layer in comparison to a

traditional MLCC fabrication process, thereby requiring five times the manufacturing equipment (e.g., tape casters). And in the case of thin dielectric layers (as in the '381 patent) that require supporting or carrier film during the green chip build up process as explained herein, the amount of expensive carrier film used and wasted (as it cannot be recycled) would be multiplied by a factor of 5 or more as well.

121. Combined, these factors would result in a process that is too slow and too expensive compared to traditional MLCC processes. Thus, a POSITA would be dissuaded from use of multiple strata and additional boundary layer material as taught by Rutt, as it would add extra cost and complexity to the process, and would lead to increased porosity at the interface between each stratum making up each dielectric layer, which would likely result in cracking and poor reliability.

122. Layer 30 disclosed in Rutt is a composite layer that is comprised of multiple strata or sublayers. In the case of Fig. 2 of Rutt, one can readily discern five individual strata or constituent layers (*i.e.*, "multiple sub-layers or strata,"). (*Id*. at 8:26). Thus, a POSITA would discern multiple constituent layers (strata) in Rutt's dielectric layer 30. For example, said constituent layers (strata) are depicted as Rutt's "five distinct strata 30A, 30B, 30C, 30D, and 30E" and are shown Fig. 2 of Rutt, reproduced below (See also *Id*. at 4:43-45).



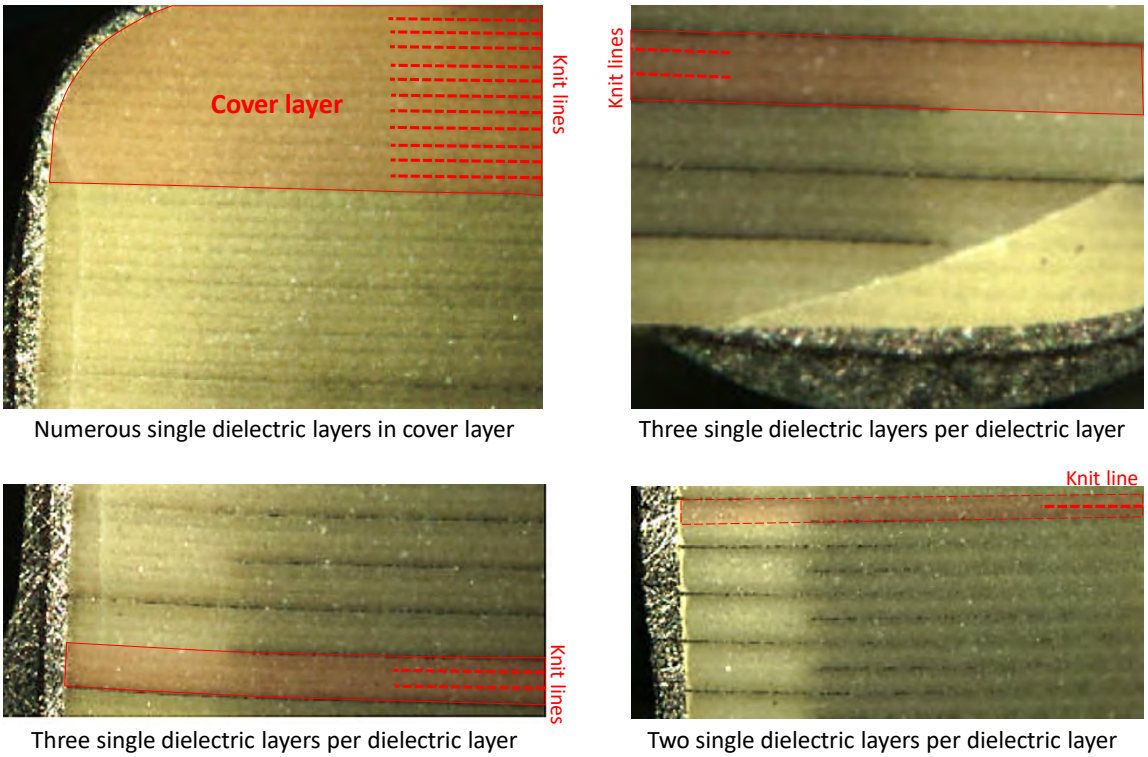
Rutt, Fig. 2

123. The stratified composite dielectric layer of Rutt is further disclosed in the description of how dielectric layer 30 is manufactured. Rutt describes "milling" zinc oxide (*i.e.*, turning it into a dispersion of powder particles) and then combining it with an acrylic latex binder and a dispersant (a mixture that includes water as a solvent) to create a "water slurry," which is then applied to a stainless steel surface or belt and is then "cut into rectangular pieces that are stacked in groups of five." (*Id*. at 5:35-49 and 5:56-57).

124. Although more complex, due to the multiple strata per dielectric layer as well as to the associated barrier layers, the process of Rutt mirrors the '381 patent's process for forming its green sheets by "mixing the ceramic powder, a

binder, and a solvent to prepare the slurry and then forming the prepared slurry as sheets having a thickness of several μm by a doctor blade method." (*Id*. at 8:15-18 and 8:25-27). The cut pieces of Rutt are called "strata" (*Id*. at 6:14-15), while the '381 patent refers to its corresponding pieces as "dielectric layers" (*Id*. at 8:13–14). Thus a POSITA would have understood that each single stratum of Rutt must be a single dielectric layer as used in the '381 patent. Because Rutt's "strata" are equivalent to dielectric layers in the '381 patent, Rutt's layer 30 cannot be "a single dielectric layer" because it is made up of the multiple single dielectric layers, each a stratum.

125. Examples of the use of multiple single dielectric layers (strata) in MLCCs are depicted below. Knit lines, due to the use of multiple single dielectric layers (strata) to make up each dielectric layer or cover layer are evident. These knit lines represent the boundary between each single dielectric layer in the fired cross section of the MLCC component, and are regions of relatively low density in the ceramic, due to one or more of binder segregation to the surface of the green tape during casting, or to the application of a boundary layer during green processing (as in Rutt) or to insufficient lamination in the green state, or the like. They are evident via optical microscopy and are typically termed "light dielectric," or "knit lines."



Examples of Multiple Single Dielectric Layers (Strata) Per Constituent Dielectric Layer[10]

As is evident from Fig. 2 and Fig. 3 of Rutt, these sublayers (each a stratum, or single dielectric layer) also are observable using scanning electron microscopy.

126. Although striations or knit lines by themselves may be deemed acceptable,[11] a POSITA would have understood that these relatively low density

[10] Adapted from, Ex. G: "Design and Process Guidelines for Use of Ceramic Chip Capacitors," CALCE Electronic Products and Systems Center, University of Maryland, 2001 (http://www.ieca-inc.com/images/Ceramic_capacitor_Failure_Mechanisms.pdf).
[11] See e.g., Ex. 1009: EIA Standard EIA-595-A, "Visual and Mechanical Inspection Multilayer Ceramic Chip Capacitors," ANSI/EIA, p. 7, Feb, 2009.

regions can lead to cracking, that result in device failure.[12,13,14,15,16,17,18] Further, as explained herein, the use of multiple sublayers per dielectric layer and the application of an additional barrier layer to constituent strata of each dielectric layer adds extra complication to the process and thus extra, unnecessary expense to each MLCC produced in this manner. Because of this, a POSITA would be dissuaded from the use of multiple single dielectric layers between opposing electrodes, unless there is a compelling reason to do so.

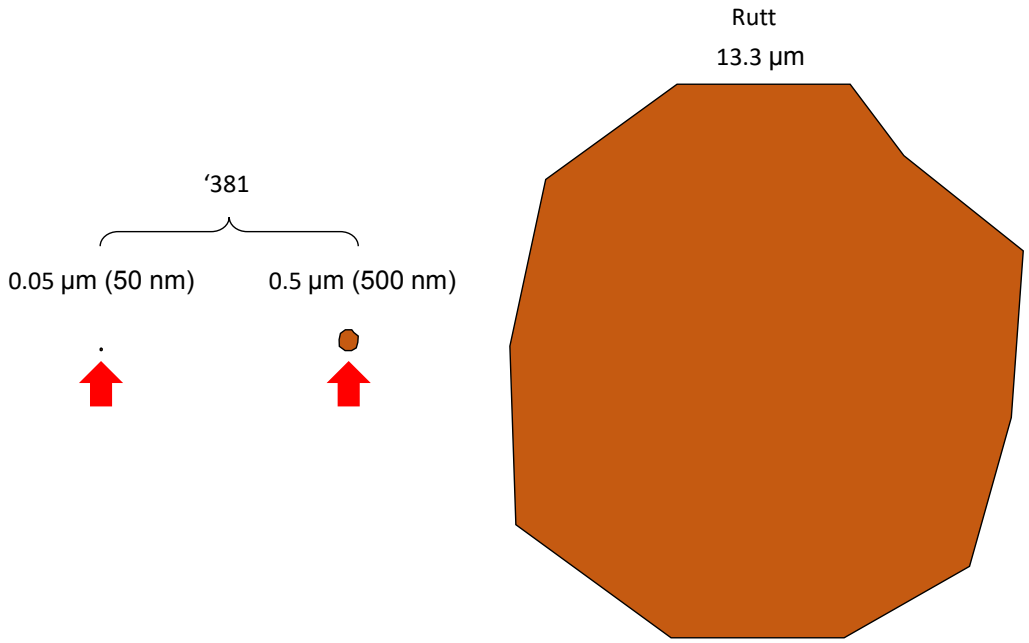
127. Rutt also equates each stratum or single ceramic layer with a green ceramic tape layer (*Id*. at 2:43-48) as does the '381 patent. However, in the case of Rutt, the stratum is configured such that a single grain results from each fired single dielectric layer or stratum when measured in a single stratum or single dielectric layer in the thickness direction. This is different from the '381 patent which discloses "an average number of dielectric grains in a ***single dielectric layer*** in a

[12] Ex. H: J. Maxwell, "Cracks: The Hidden Defect," AVX Technical Information, p. 9/10., 2000. http://www.avx.com/docs/techinfo/CeramicCapacitors/cracks.pdf.
[13] Ex. I: N. Blatau, et al., "Robustness of Surface Mount Multilayer Ceramic Capacitors Assembled with Pb-Free Solder," DfR Solutions, http://www.dfrsolutions.com/hubfs/DfR_Solutions_Website/Resources-Archived/Publications/2005-2007/2005_Cracking_Pb-free.pdf.
[14] Ex. J: NIC Components, Corp., "MLCC - Ceramic Chip Capacitors / Failure Mode Study, Potential Failure Causes, Accelerators, Behavior." http://www.niccomp.com/resource/files/ceramic/MLCC-FailureModeStudy-032012.pdf.
[15] Ex. G: "Design and Process Guidelines for Use of Ceramic Chip Capacitors," CALCE Electronic Products and Systems Center, University of Maryland, 2001 (http://www.ieca-inc.com/images/Ceramic_capacitor_Failure_Mechanisms.pdf).
[16] Ex. K: N. Blatau, C. Hillman, "Design Guidelines for Ceramic Capacitors Attached with SAC Solder," http://resources.dfrsolutions.com/Publications/2005-2007/2006_DesignCeramCapSAC.pdf.
[17] Ex. L: CALCE EPSC, University of Maryland, "Ceramic Capacitor Failures on the Rise," 2001. http://www.calce.umd.edu/whats_new/2001/Ceramic.pdf.
[18] Ex. M: A. Teverovsky, "Effect of Manual-Soldering-Induced Stresses on Ceramic Capacitors (Part I)," NEPP report, December, 2008. https://nepp.nasa.gov/files/16346/08_002_01%20GSFC%20Teverovsky.pdf.

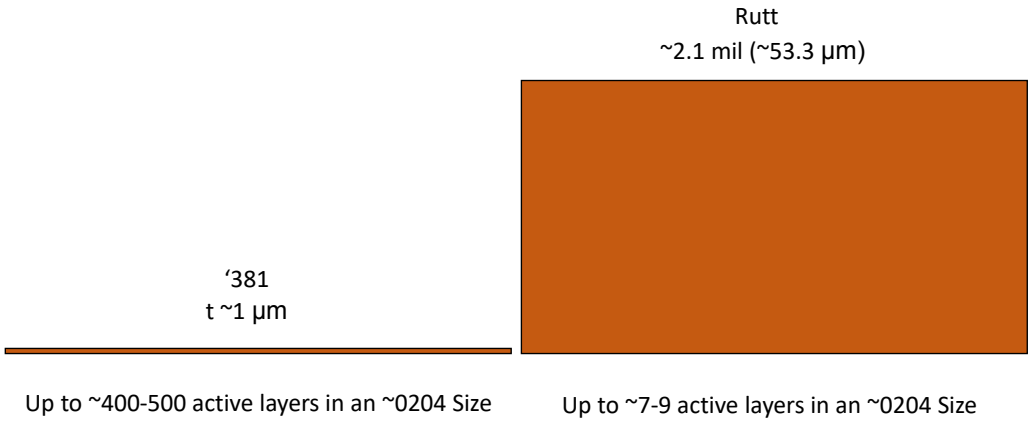
thickness direction thereof is 2 or greater." (see e.g., *Id*. at Abstract, 2:12-15, 4:39-41, 7:13-16, 7:16-19, 2:61-63, Claims 1-19).

128. Further, the dielectric thickness and grain sizes taught by Rutt are huge in comparison to those taught in the '381 patent. For example, Rutt teaches a fired varistor layer thickness of 2.1 mils (~53.3 μm) for layers containing 4 single dielectric layers, each a stratum (*Id*. at 6:64-68) or a grain thickness dimension of ~13.3 μm assuming 1 grain per stratum as shown in Fig. 2 of Rutt, while the '381 patent teaches dielectric layers of approximately 1 μm thickness (based upon a green tape thickness of 1.8 μm (*Id*. at 8:47) and taking into consideration reduction of the green tape thickness during lamination and firing shrinkage as described herein, as a POSITA would understand to be ca. 35 - 60% combined), with fired dielectric grains of between 0.05 μm to 0.5 μm (*Id*. at 7:28-29). Thus, the dielectric layers of Rutt are more than 50 times thicker than the dielectric layers of the '381 patent.

129. Additionally, the fired grain size disclosed in Rutt is more than 25X to 250X larger than the fired grains of the '381 patent. The significance of these two factors is illustrated in the sketch below. Dielectric layers and fired grains of this size could not enable a high *C/V* MLCC as taught in '381. Understanding this, a POSITA would thus be dissuaded from combining Rutt with any reference to attempt to achieve the thin layer (*t*), high active count (*n*), high *C/V* MLCC devices disclosed in the '381 patent.



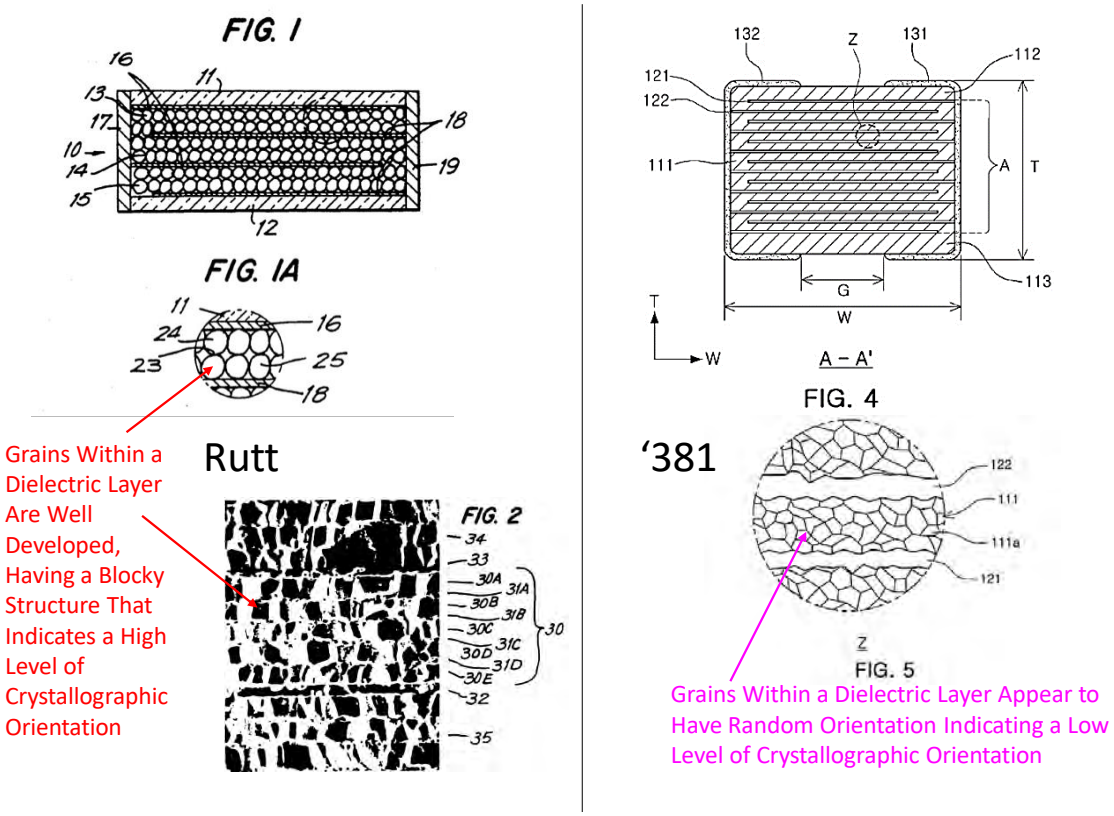
Relative dielectric grain size: ‘381 vs. Rutt



Relative Dielectric Thickness: ‘381 vs. Rutt

130. Further, the thermal process (firing) used by Rutt results in significant grain growth and grain development, such that the grains are “blocky,” having an appearance of grains that would have a relatively high level of crystallographic

orientation compared to dielectric grains resulting from the MLCC manufacturing method and microstructure disclosed in the '381 patent. This is because the firing schedule of Rutt is developed to achieve grain growth of a single grain across the depth of the entire stratum which would also result in a considerable increase in crystallographic orientation compared to the more random grain structure of the '381 devices as indicated in the illustration below.



Microstructures: Comparison of Rutt and '381

131. A POSITA would understand that this relatively high level of crystallographic orientation is counter to the firing profiles and resulting microstructures that are characteristic of the high *C/V* MLCCs of the '381 patent,

which aim for complete densification and not excessive grain growth or excessive crystallographic orientation as a POSITA would understand that would increase the piezoelectric effect and/or the electrostrictive effect exhibited by said ceramic dielectric materials.

132. As described above, a POSITA would have understood that use of the grain structure of Rutt would result in relatively high vibration amplitude exhibited by the resulting devices, which would result in a relatively high level of emission of acoustic noise when subjected to AC signals causing device vibrations in the audible frequency spectrum as described herein. A POSITA would have understood that this would be counter to the objective of the '381 patent (i.e., a low ESL, low acoustic noise emission, high *C/V* MLCC and associated configuration of said device mounted to a PCB), and thus would be dissuaded from using such a microstructure in the active dielectric layer of the '381 patent.

133. Further, the microstructures taught by Figs. 1 of Rutt are confusing as illustrated below. From Fig. 1 of Rutt, it appears that the cover layers and end margins are made from a different, dense material as compared to the active layer. The ceramic layers within the active layer also appear to be highly porous or to be infiltrated with another, unspecified material as indicated below. Because of this, a POSITA would be confused regarding the preferred fired microstructure of the device and thus would be dissuaded from trying to reproduce the results.

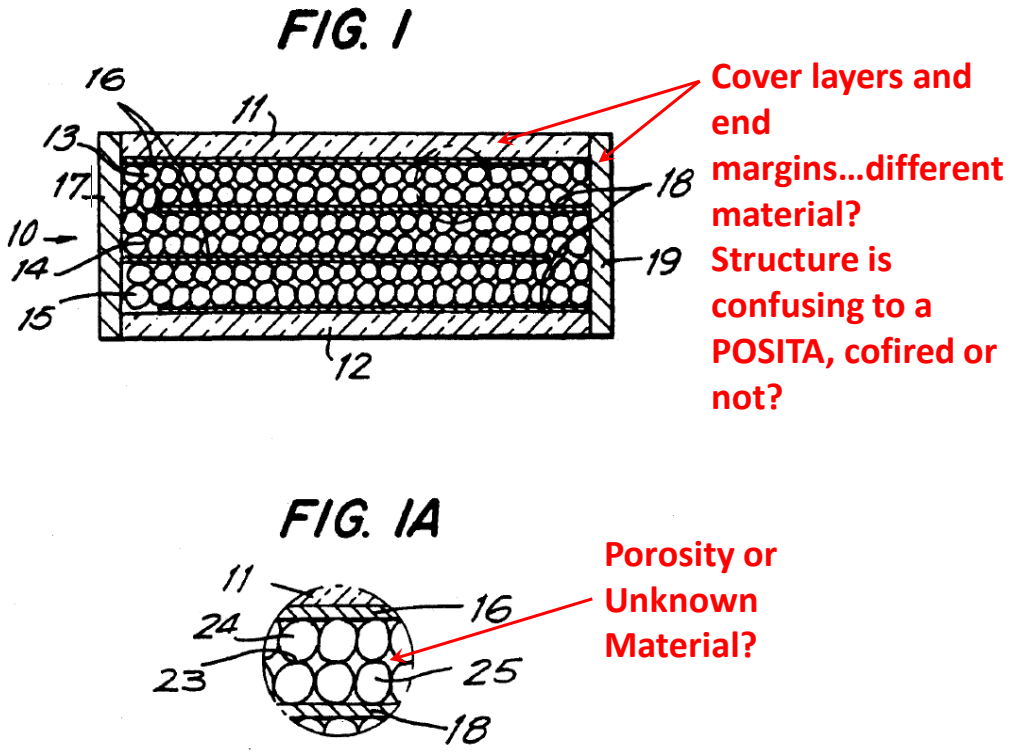


Fig. 1 of Rutt Would have been Confusing to a POSITA (annotated)

E. U.S. Published Patent Application US2012/0152604 (Ahn)

134. United States Published Patent Application US2012/0152604, having inventors Y. Ahn, et al., and assigned to Samsung Electromechanics, Co., Ltd., (Ahn) is directed toward a mounting structure of a circuit board having thereon a multi-layered ceramic capacitor, a method thereof, a land pattern of a circuit board for the same, a packing unit for a multi-layered ceramic capacitor taped horizontally, and an aligning method thereof. (*Id*. at par. 0004).

135. Ahn teaches that acoustic noise in mounted ferroelectric type MLCC capacitors can be reduced by implementation of two features:

1. Mounting the capacitor (MLCC) on the board so that its internal electrodes are horizontal
2. Reducing the height of the solder used to connect the capacitor to the electrode pads (e.g., to less than 1/3 the thickness of said MLCC)

136. Ahn teaches that acoustic noise is only an issue in high *C/V* ferroelectric or similar type MLCCs that exhibit significant piezeoelectric or electrostrictive effect or the like (and not other types of capacitors or electronic devices):

> "A ferroelectric material such as barium titanate having a relatively high dielectric constant is usually used as a dielectric material of the multi-layered ceramic capacitor. However, since such ferroelectric material has a piezoelectric property and an electrostrictive property, the mechanical stress and deformation occur when an electric field is applied to such ferroelectric material. In the case that a periodic electric field is applied to the multi-layered ceramic capacitor, the multi-layered ceramic capacitor vibrates by the mechanical deformation due to the piezoelectric property of its ferroelectric material. Such vibrations of the multi-layered ceramic capacitor are transferred to the circuit board having the multi-layered ceramic capacitor thereon." (*Id*. at par. 0009).

137. Ahn also discusses a separated electrode pad arrangement (see e.g., *Id*. at pars. 76-80, Fig. 5 and Fig. 6). However, this configuration is intended "to reduce the soldering amount" only, (see e.g., *Id*. at pars. 0059, 0066, 0078) and no additional

mechanism for emitted acoustic noise reduction is mentioned in Ahn. Therefore, the teachings of Ahn are limited to mounting the MLCC such that the internal electrodes are horizontal with respect to the plane of the circuit board (PCB), and to limiting the solder fillet height (15) to 1/3 or less of the thickness (T_{MLCC}) of said mounted MLCC or similar due to electrode pad land design parameters (e.g., $0<L_{LAND}/L_{MLCC}\leq 1.2$ and $0<W_{LAND}/W_{MLCC}\leq 1.2$).

V. PATENTABILITY OF THE CHALLENGED CLAIMS OF THE '381 PATENT

A. Applicable Legal Principles

138. I am informed by counsel and I understand that the first step in determining validity of a claim in a granted patent is to properly construe the claims. I understand that the Board has issued a Decision regarding the definition of the claim element "when a thickness of the ceramic body is defined as T and a width thereof is defined as W." It is my understanding that the Board agrees with the Petitioner that the meaning of "when a thickness of the ceramic body is defined as T and a width thereof is defined as W" is a reference "to the thickness and width of the ceramic body not including the external electrodes." I have applied the Boards' Decision in this report. It is also my understanding that, at this time in the proceeding, the Board has determined that it is not necessary to provide an express interpretation of any other term of the claims.

139. Further, I have been informed by counsel and it is my understanding that for a finding of invalidity of a patent under 35 U.S.C. § 102, i.e., anticipation, each and every element of a claim, as properly construed, must be found either explicitly or inherently in a single prior art reference. Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes the claimed limitations, it anticipates. However, if the prior art could function without the claimed limitations, then the claimed limitations are not inherent. It is my understanding that anticipation is not at issue with regard to any of the Petitioner's asserted grounds for invalidity of the '381 patent in this matter.

140. Further, I have been informed by counsel and I understand that a claimed invention is unpatentable under 35 U.S.C. § 103 if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Obviousness, as I understand it, is based upon the scope and content of the prior art, the differences between the prior art and the claim, the level of ordinary skill in the art, and any objective evidence of non-obviousness, which is also referred to as "secondary considerations of non-obviousness."

141. It is my understanding that secondary considerations of non-obviousness may include, for example:

1. Long felt but unmet need in the prior art that was satisfied by the invention;
2. Failure of others to achieve the results of the invention;
3. Commercial success of the invention;
4. Copying of the invention by others in the field;
5. Whether the invention was contrary to the accepted wisdom of the prior art;
6. Expression of disbelief or skepticism by those skilled in the art;
7. Unexpected results;
8. Praise of the invention by others skilled in the art; and
9. Taking of licenses under the patent by others.

142. I also understand that there must be a nexus between any such objective evidence of non-obviousness and the invention, and that mere conclusory statements cannot sustain an obviousness opinion; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. As I understand, it may be necessary to assess, among other things, the interrelated teachings of patents as well as the background knowledge of the ordinarily skilled person in order to determine an apparent reason to combine known elements as claimed. Further, I understand that it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does.

143. It is further my understanding that it is impermissible to simply engage in hindsight reconstruction of the claimed invention, using the applicant's invention

as a template and selecting elements from the references to fill the gaps. I am informed that a fact finder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon hindsight reasoning.

B. Claim Construction

144. I am informed by counsel that patent claims should be understood from the perspective of a person of ordinary skill in the relevant art to which the patents relate and based on the understanding of that skilled person at the time the application was filed. The ordinary artisan, in my opinion, would hold a Masters' Degree from an accredited university in Materials Science, or Materials Science and Engineering, or Chemical Engineering, or Chemistry or an analogous Engineering degree, and at least two years of industry experience in the design and manufacture of multilayer ceramic capacitors.[19] I also understand that advanced levels of experience can be considered as a substitute for formal education in certain cases.

145. With regard to the '381 patent, a POSITA would have understood the term "a single dielectric layer" to mean an integral layer of dielectric material having

[19] I have been informed by counsel of the legal standards used to determine the level of ordinary skill in the art. I understand that prior art references can provide evidence of the level of ordinary skill in the art and that factors that may be considered in determining this level of skill can include the educational level of the inventors and active workers in the field, the type of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, and the sophistication of the technology.

no discernable constituent layers. The '381 patent equates ceramic green sheets with dielectric layers (*Id*. at 8:9-15). Additionally, the '381 patent discloses numerous times that there may be more than one single dielectric layer or ceramic tape layer or stratum between each pair of first and second internal electrodes. (see e.g., *Id*. at 1:32-36, 1:66-2:1, 2:46-50, 4:23-27, 5:13-17, 6:14-18, claims 1-19). Finally, each and every time that the '381 patent discloses that the average number of dielectric grains in the thickness direction of the dielectric layer is 2 or greater, the word "single" is used to modify the words "dielectric layer." (see e.g., *Id*. at Abstract, 2:12-14, 2:61-64, 4:39-41, 7:13-16, 7:17-19, claims 1-19).

146. Further, a POSITA would have understood that the term "single layer" is synonymous with the term "stratum" in the context of both '381 and Rutt, as the definition of stratum is "A thin layer within any structure".[20] Thus a strata is a compilation of more than one single stratum. As discussed herein, a POSITA would have understood that the use of multiple single layers to form a dielectric layer is common in the industry for various reasons (e.g., to increase dielectric breakdown strength or dielectric withstanding voltage or to reduce shorts between electrodes due to "through porosity" or the like). However, a POSITA also would be dissuaded from the use of multiple single layers to form a dielectric layer unless there is a compelling reason to do so, as use of multiple single layers in a dielectric layer adds

[20] Ex. N: Oxford Dictionaries: Stratum. https://en.oxforddictionaries.com/definition/stratum

additional cost and complexity (especially in the case of the thin dielectric layers of the '381 patent) of the MLCC device. A POSITA is further dissuaded from the use of multiple single layers when knit lines or regions of low density are formed between each single dielectric layer, as these regions may result in cracking, delamination and the like that may result in failure of said MLCC devices as described herein.

147. Additionally, each single dielectric layer is discernable within a dielectric using means that would have been available to a POSITA as shown above in the case of knit lines, using for example, optical microscopy to examine multilayer ceramic capacitor cross sections. Further, the '381 patent discloses in its specification that:

> "the average number and the average grain size of the dielectric grains 111*a* may be measured from an image obtained by scanning a cross-section of the ceramic body 110 in the width direction." ('381 patent (Ex. 1001) at 7:45–48.).

The specification describes measuring at thirty equidistant points of a single dielectric layer captured by the image (*Id.* at 7:56–60), and sketches of images are shown in Figure 4 as well as an enlarged portion of Fig. 4 ("Z"), in Figure 5. (*Id.* at Figs. 4–5).

148. These images (either from optical microscopy or electron microscopy, such as scanning electron microscopy (SEM) or other suitable means) are commonly

obtained and used in the evaluation and inspection of the internal structure of MLCCs. Using said images, a POSITA could have visually distinguished or discerned a thickness of ceramic dielectric material in order to determine the thickness dimension of a "single dielectric layer" as described in the specification. Using said micrographs, a POSITA would visually identify a "single" dielectric layer in the image by locating an integral layer of dielectric material that cannot be discerned into constituent layers, then would measure the thickness of said dielectric layer using a method similar to that described in '381 for measuring dielectric grain size, or another suitable means. (see for example *Id*. at 7:42-63).

149. Further, the claims themselves support the above meaning of "single dielectric layer". For example, claim 1 uses the term "layer" without "single" when referencing a layer that has multiple constituent layers (e.g., "active layer" includes "a plurality of first and second internal electrodes disposed to face each other with at least one of the dielectric layers interposed therebetween and alternately exposed to the first or second side surface;" (see e.g., *Id.* at 1:65-2:2, 2:46-51, 4:23-27, 6:14-18, 8:23-32, Fig. 4, Claims 1-19).

150. Additionally, claim 1 uses the phrase "at least one of the dielectric layers interposed therebetween", which indicates that multiple dielectric layers may be interposed therebetween, and thus must be discernable as plural "layers," so that "at least one" such layer can be identified. (*Id.* at Claim 1). Claim 1 also uses the

designation "single" to reference one such discernable layer in the term "single dielectric layer." (*Id.* at Claim 1).

151. The above meaning of "single dielectric layer" is also supported numerous times in the specification of '381. For example, "The first and second internal electrodes **121** and **122** may be disposed to face each other, having at least one of the dielectric layers **111** interposed therebetween" (*Id*. at 5:13-16).

152. Additionally, the '381 patent discloses that "The active layer A may be formed by repeatedly stacking the plurality of first and second internal electrodes **121** and **122** having at least one of the dielectric layers **111** interposed there between." (*Id*. at 6:14-18).

153. Further, Itamura supports the proposed construction for single dielectric layer as it differentiates plating layers in a similar manner. For example, Itamura states:

> "The structure of the third layer 16 is not limited to the two-layer structure described above. The third layer 16 may include a ***single*** layer or three or more layers." (Id. at 7:27–29 (emphasis added)).

In the above excerpt from Itamura, "single" is used to differentiate layers that are each discernable into multiple constituent layers, as in Itamura's layer 16 being comprised of either two discernable layers or with three or more discernable layers. Because each single layer is discernable and makes up layer 16, Itamura also

supports the construction that a single layer, is a layer of material that that cannot be discerned into multiple constituent layers.

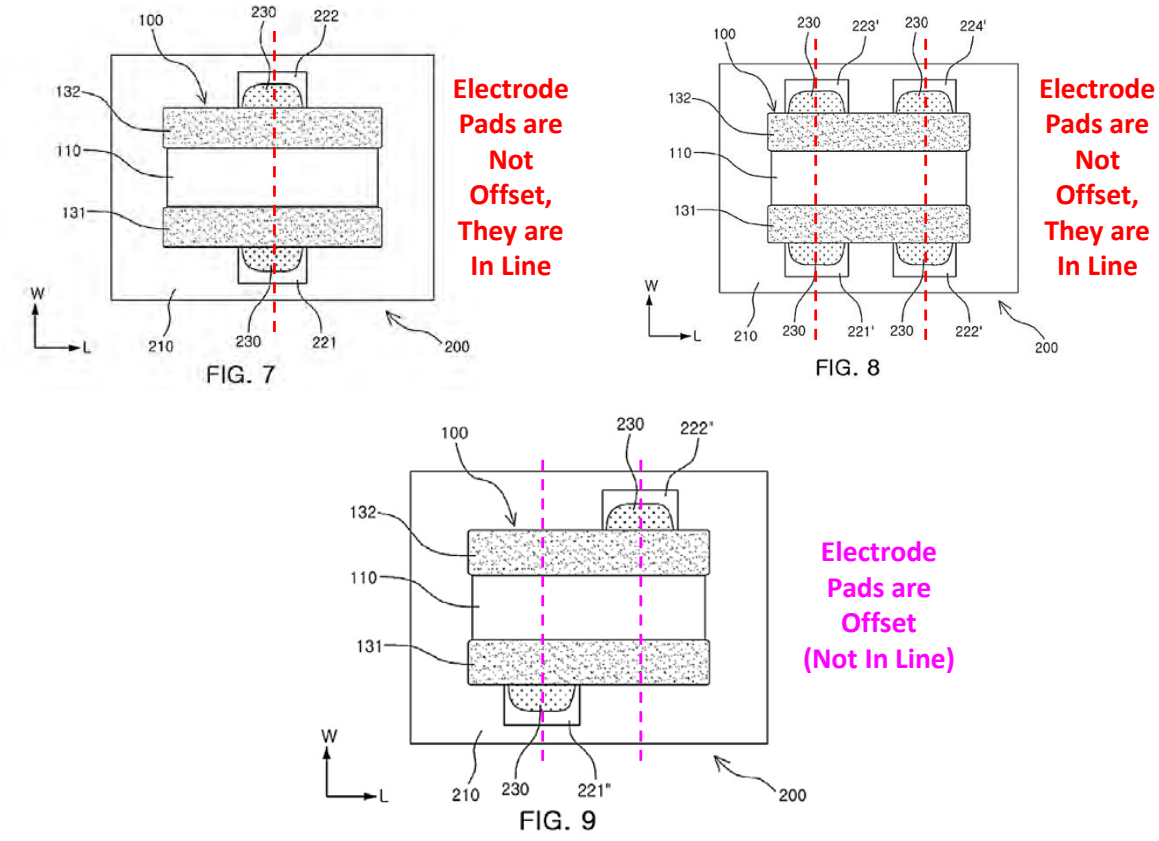
154. Further, as described herein, Rutt also differentiates a single layer or stratum from a dielectric layer. For example, Rutt discloses fabrication of a control device with "a thicker ***single film*** the total thickness of which approximately equaled the plurality of stacked films," which is compared to an embodiment where "layers of ceramic were fabricated by ***multiple sub-layers*** or strata." (*Id.* at 8:25-32 (emphasis added); see also *Id.* at 7:17-20.) As with Itamura and the '381 patent, Rutt uses the word "single" to distinguish from a layer that can be discerned into multiple constituent layers ("multiple sub-layers," each a stratum).

155. Further a POSITA would have understood the term "the first and second electrode pads are offset to each other in a width direction of the multilayer ceramic capacitor" to mean that each electrode pad of a first polarity connected to the multilayer ceramic capacitor is out of line, in the width direction, from all electrode pads of a second polarity connected to the capacitor.

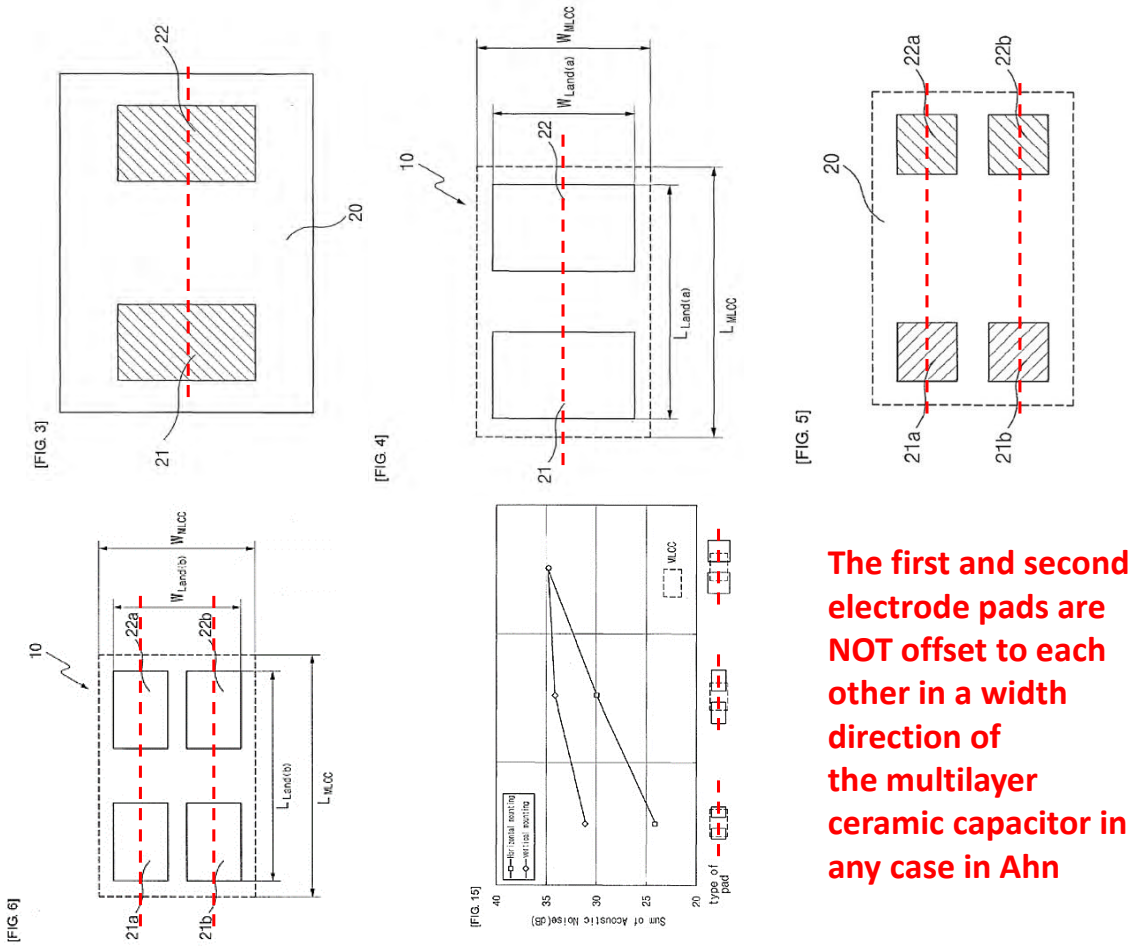
156. The definition of offset is to "place out of line" or "the amount or distance by which something is out of line."[21] An illustration of offset vs. in line with respect to electrode pads in the width direction of the mounted device as disclosed in '381 is shown below. None of the embodiments in the Ahn patent are

[21] Ex. O: Oxford Dictionary: Offset. https://en.oxforddictionaries.com/definition/offset

offset in this manner, but are all in line as illustrated below as well. Ahn does not mention offset. A POSITA would have understood that Ahn pertains only to circuit board structures wherein the electrode pads are in line with another electrode pad in the width direction of the mounted device in all cases. Ahn does not mention any design having offset electrode pads in the width direction, nor does Ahn mention or imply any benefit to such an offset configuration as is taught in the '381 patent.



Offset vs. In Line Electrode Pads



The first and second electrode pads are NOT offset to each other in a width direction of the multilayer ceramic capacitor in any case in Ahn

Ahn Does Not Teach First and Second Electrode Pads that are Offset to Each Other in a Width Direction of the MLCC

157. Further, a POSITA would have been dissuaded from using the electrode pad designs of the embodiments associated with Fig. 5 and Fig. 6 of Ahn (see e.g., *Id*. at pars. 0075-0080, Fig. 5, Fig. 6) as use of such a configuration would result in increased inductance as discussed herein. Since this practice would be contrary to the objective of the '381 patent (i.e., a low ESL (inductance), low acoustic noise

emission, high *C/V*, ferroelectric-type MLCC and associated configuration of said device mounted to a PCB), a POSITA would have been dissuaded from using Ahn in combination with Itamura and Rutt or other references, because the reduced amount of solder disclosed in Ahn, combined with the relatively small pads, each placed near the corners of the mounting perimeter of said MLCC, would increase inductance (ESL) of the mounted device, and thus would be contrary to the objectives of the '381 patent. This is because the inductance of the mounted device depends upon the inductance of the MLCC itself as well as upon the inductance of its mounting configuration as explained above).

158. Since the inductance of a conductor increases as the conductor is reduced in cross sectional area (i.e., less solder and lower solder fillet height, as well as less width dimension of two pads on a side with a gap in between, compared to one wide pad covering the entire width of the device as illustrated above), and since the inductance of a conductor increases as the length of the inductor increases (e.g., increased current path within the mounted MLCC, due to separated mounting pads), and since the inductance of a conductor increases due to mutual inductance effect of closely spaced conductors that flow current in the same direction, the inductance of the mounted device configuration would increase when using the mounting pad configuration associated with Fig. 5 and Fig. 6 of Ahn as discussed herein. Thus, a POSITA would understand that the increased inductance of Ahn would have worked

against the low inductance of Itamura, and would not have expected to achieve low ESL or to reduce ESL from an MLCC device mounted with this configuration (*Id*. at pars. 0075-0080), and thus would be dissuaded from using Ahn in combination with Itamura to achieve the objective of the '381 patent (i.e., a mounted, low ESL, high *C/V*, low acoustic emission device configuration).

159. Further, the '381 patent discloses an embodiment that is related to Fig. 7. For said embodiment, one electrode pad for connection to a first external electrode of an MLCC is in line, in the width direction, with one opposing electrode pad for connection to a second external electrode of said MLCC. (*Id*. at 12:5-67). Another embodiment disclosed in the '381 patent and related to Fig. 8 of '381, discloses two electrode pads for connection to the first polarity external electrode of an MLCC which are spaced apart from each other, but are both in line with two additional electrode pads for connection to the same second polarity external electrode of the same MLCC. (*Id*. at 13:1-12.). But, the '381 patent discloses "another exemplary embodiment", that is related to Fig. 9, wherein the electrode pads to be connected to the first external electrodes of an MLCC are designated as offset to the electrode pads to be connected to the second external electrode of said MLCC in the width direction as they are "offset to each other." (*Id*. at 13:13-22).

160. Thus, the '381 patent clearly and explicitly differentiates between inline and offset in the width direction. With regard to the '381 patent, a POSITA would

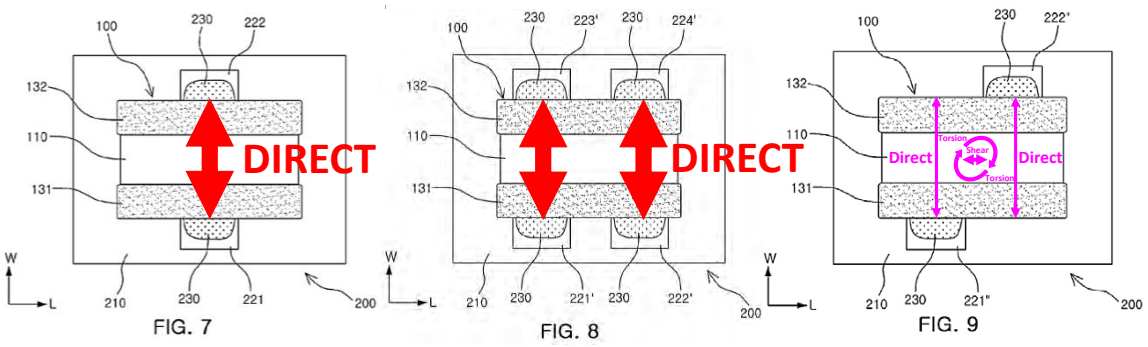
have understood that the term "offset" is used only with respect to the embodiment that is related to Fig. 9. A POSITA would have understood that the term "offset" electrodes is not used in the disclosed embodiments that related to either the Fig. 7 or Fig. 8 embodiments. (*See Id*. at 12:5-13:22.).

161. Further, the disclosed embodiments that are related to Fig. 7 and Fig. 8 each have their own corresponding claims (i.e., claim 17 and claim 19 respectively). (*Id*. at claims 17 and 19). Thus, a POSITA would have understood that the phrase "the first and second electrode pads are offset to each other in a width direction of the multilayer ceramic capacitor" to mean each electrode pad of a first polarity connected to the multilayer ceramic capacitor is out of line, or offset, in the width direction, from all electrode pads of a second polarity connected to the capacitor. This construction allows the disclosure of the "offset" embodiment that is related to Fig. 9, without erroneously or unduly restricting the embodiments related to Fig. 7 and Fig. 8 of the '381 patent.

162. A POSITA would have understood that, when the physical connections (i.e., solder connections in the case of the '381 patent) of the first and second external electrodes of an MLCC to a circuit board are not in line in the width direction, the vibrations emitted from the MLCC due to piezoelectric or electrostrictive effect, or the like, will not mechanically couple with the printed circuit board as well as if they are in line with each other in the width direction. This is because the expansions and

contractions of the MLCC that cause said vibrations, will be transformed from pure expansion/contraction to lesser expansion/contraction, combined with torsion and/or shear components, with respect to mechanical coupling with the printed circuit board (PCB). The lesser torsion and/or shear components will not mechanically transfer said vibrations to the circuit board as effectively as direct mechanical coupling of expansion/contraction of the MLCC does, thereby resulting in less acoustic noise emission from the mounted MLCC and board configuration.

163. Thus, reduced direct mechanical coupling of the MLCC to the printed circuit board (PCB), combined with relatively ineffective vibration transference to the circuit board from torsion and/or shear components, results in less overall transfer of vibrations from the MLCC to the printed circuit board (PCB). This results in less emitted noise from the PCB when the MLCC vibrates due to piezoelectric or electrostrictive effects or the like as illustrated below. A POSITA would have understood that this occurs when the MLCC is subjected to an AC signal or the like that causes said vibrations to occur in the audible frequency range.



In Line Electrode Pads Result in Direct Mechanical Coupling of the MLCC to the Circuit Board. Vibrations are Directly Transferred to PCB Due to Direct Mechanical Coupling and Emitted Noise is Maximized

Offset Pads Result in Reduced Mechanical Coupling to the PCB as There is no Physical Mount That is In Line with Another. Less Vibration is Transferred to the PCB as Torsion and/or Shear Forces Are Created That Do Not Mechanically Transfer the Vibrations as Well as Direct Mechanical Coupling. Less of Each Vibration is Transmitted and Less Noise is Emitted.

In Line (Direct) Mechanical Coupling Compared to Offset Mechanical Coupling

164. Thus, A POSITA would have understood that the offset disclosure of the '381 patent (*Id*. at 13:18–22):

> "since the first and second electrode pads 221" and 222" may be offset to each other in the width direction of the multilayer ceramic capacitor, contraction and expansion may be offset to each other, such that an effect of reducing acoustic noise may be further excellent."

explains that ***each*** electrode pad connecting to a first external electrode of an MLCC is out of line with (i.e., offset from) ***all*** electrode pads that connect to a second external electrode of the same MLCC. This is because an electrode pad that is connected to a first external electrode of an MLCC that is in line with an opposing electrode pad that is connected to a second external electrode of the same MLCC in

the width direction of said MLCC, even if offset to some other electrode pad (see for example Fig. 8 of '381), would not cause the less efficient transfer of vibrations emitted from the MLCC to the PCB as discussed above, and thus would not reduce acoustic noise emissions as effectively as the offset embodiment taught in the '381 patent, and thus is not the intended teaching of this embodiment of the '381 patent.

165. Thus, a POSITA would have understood that the term "the first and second electrode pads are offset to each other in a width direction of the multilayer ceramic capacitor" to mean that each electrode pad of a first polarity connected to the multilayer ceramic capacitor is out of line, in the width direction, from all electrode pads of a second polarity connected to the capacitor.

166. From the intrinsic evidence directly from the '381 patent, and the extrinsic evidence, a POSITA would have understood that there is no other reasonable way to construe "the first and second electrode pads are offset to each other in a width direction of the multilayer ceramic capacitor" at least because the related embodiment (i.e., Fig. 9) must be different from the embodiments related to Figs. 7 and 8 as they each relate to a separate and different claim (i.e., 17 and 19, vs. 18).

167. Further, Ahn teaches only that noise can be reduced by implementing its two inventive features: (1) mounting the capacitor on the board so that its internal electrodes are horizontal, and (2) reducing the height of the solder used to connect

the capacitor to the electrode pads. (see for example *Id*. at Abstract, pars. 0004, 0022, 0059). Ahn does not disclose reduced acoustic emission resulting from circuit board electrode pad configuration.

168. Further, a POSITA would have been dissuaded from using the electrode pad designs of the embodiments associated with Fig. 5 and Fig. 6 of Ahn (see e.g., *Id*. at pars. 0075-0080, Fig. 5, Fig. 6) as use of such a configuration would result in increased inductance, which is contrary to the objective of the '381 patent (i.e., a low ESL (inductance), low acoustic noise emission, ferroelectric-type MLCC and associated configuration of said device mounted to a PCB) as described herein.

169. A POSITA would have been dissuaded because the reduced amount of solder and the relatively small pads that are placed near the corners ends of the mounting perimeter of said MLCC would increase inductance (ESL) of the mounted device, and thus would be contrary to the objectives of the '381 patent as discussed herein.

170. This is because the inductance of the mounted device depends upon the inductance of the MLCC itself as well as upon its mounting configuration as explained above). Since the inductance of a conductor increases as the conductor is reduced in cross sectional area (i.e., less solder and lower solder fillet height, as well as less width dimension of two pads on a side with a gap in between, compared to one wide pad covering the entire width of the device), and since the inductance of a

conductor increases as the length of the inductor increases (e.g., increased current path within the mounted MLCC, due to separated mounting pads), and since the inductance of a conductor increases due to mutual inductance effect of closely spaced conductors that flow current in the same direction, the inductance of the mounted device configuration increases. Thus, a POSITA would not have expected to achieve low ESL or to reduce ESL from an MLCC device mounted as disclosed by the embodiments associated with Fig. 5 and Fig. 6 of Ahn (*Id*. at pars. 0075-0080), and thus would be dissuaded from using Ahn to achieve said objective of the '381 patent (i.e., a mounted, low ESL, high *C/V*, low noise emission device configuration).

C. Claim 1: Itamura and Rutt

171. The Board's institution decision as to claim 1 is based on the combination of Itamura and Rutt. As described below, it is my opinion that this combination does not render claim 1 obvious. Further, it is my opinion that those skilled in the art would have been dissuaded from combining Rutt with Itamura in order to practice the '381 patent as discussed below and herein.

172. Claim 1 recites, among other things, that "an average number of dielectric grains in a single dielectric layer in a thickness direction thereof is 2 or greater." As explained above, a POSITA would have understood "a single dielectric

layer" to mean "an integral layer of dielectric material having no discernable constituent layers." Petitioner AVX concedes that Itamura does not disclose or teach "an average number of dielectric grains in a single dielectric layer in a thickness direction thereof is 2 or greater." Petitioner instead points to the teachings of Rutt.

173. However, Rutt ***also*** does not teach an average number of dielectric grains in a single dielectric layer (stratum) in a thickness direction of 2 or greater. In contrast, Rutt teaches of a multilayer varistor or intergranular barrier layer capacitor (IBLC), having at least two individual ceramic layers, each a stratum, between each set of opposed electrodes (see for example, *Id*. at Abstract, 2:48-59, 3:8-15, 5:4-10, Examples I-VI, Claims 1-4).

174. Additionally, Rutt teaches that each of stratum must be separated by a boundary layer which resists grain growth there across. (see for example, *Id*. at Abstract, 2:38-60, 3:8-15, 5:4-10, Examples I-VI, Claims 1-4). The boundary layer of the embodiments of Rutt is high binder concentration (*Id*. at 2:43-48), or other means:

> "The invention is predicated in large measure on the discovery that ceramic grain growth is inhibited by the higher binder concentrations present at the upper surface of a green ceramic tape or stratum, such that when the tape or stratum is processed within controlled heating parameters, ceramic grains will not grow across the high-binder concentration boundary."

175. As discussed herein, a POSITA would have understood that this type

of boundary layer (resulting from an additional, separate application of binder or other material to each single layer (stratum) would result in knit lines or light dielectric in at each single layer (stratum) interface within the device. A POSITA would have understood that to be an undesirable feature which may result in cracking or similar intrinsic defect that would result in device failure as discussed herein.

176. A POSITA also would have understood that Rutt does not teach the claim limitations of claim 1 of the '381 patent, either alone or when combined with Itamura, because Rutt teaches the necessity of binder barrier layers or the like (as grain growth barrier layers) in between each stratum that together comprise each of the dielectric layers, which is not a feature anywhere in the '381 patent and which would have been dissuasive to a POSITA due at least to the numerous reasons discussed herein.

177. Further, Rutt does not teach a "single" layer dielectric layer. The intrinsic record of Rutt, including all of the claims, all of the embodiments and all of the descriptions, etc., teach of a multiple (i.e., more than one) stratum or single ceramic layer between opposing electrodes to comprise the dielectric layer or strata. Nowhere does Rutt disclose or imply an inventive device comprised of only one stratum per pair of opposing electrodes.

178. Further, a POSITA would have been dissuaded from using Rutt with Itamura to construct the devices of the '381 patent as they would understand that the

use of multiple single layers (strata) between opposing electrodes as the dielectric layer would require additional process complexity and cost as the method of using multiple strata and applied boundary layers per each dielectric layer would slow and complicate the manufacturing process considerably.

179. Further, for the thin dielectric layer devices of the '381 patent, use of multiple single dielectric layers (strata) per dielectric layer would result in increased waste of disposable material as the thin green tape used in the embodiments of the '381 patent must be supported by disposable carrier film that is expensive and is thrown away as part of the green chip manufacturing process.

180. Further, the technology (device type and material type) is prohibitively different from that of the devices of '381. A POSITA would have been dissuaded from combining Rutt with Itamura to achieve the devices of the '381 patent because Rutt pertains only to boundary layer devices such as varistors, intergranular boundary layer capacitors (IBLCs) or positive temperature coefficient of resistance (PTCR) thermistors, each of which are very different from the MLCCs of '381 due at least to the different chemistries and microstructures/microstructure sizes used, as well as to the different mechanisms of forming dielectric constant (ε') as well as to other reasons detailed herein.

181. As discussed above, there are many different types of capacitors that do not pertain to the '381 patent. The '381 patent does not pertain to electrolytic

capacitors, or to film capacitors, for example. Similarly, IBLC technology does not pertain to ferroelectric or similar MLCC technology, as IBLCs are made of a special type of ceramic that is doped with dopant chemistries in order to make it highly semiconducting. These semiconducting grains are combined with specialized insulating barrier layers around each semiconducting grain so as to provide capacitance via space charge polarization (*Id*. at 10:3-15):

> "For example, the number of grain boundaries between adjacent electrode layers is also of significance in capacitors such as intergranular barrier layer capacitors, such capacitors being fabricated of ceramic materials which have been doped to render the same semi-conductive and wherein the grain boundaries are relied upon to provide the insulative factor."

This is very different than the materials and mechanisms used to form capacitance in the MLCCs of the '381 patent as described herein.

182. Also as discussed above, IBLCs are large grained devices. Consequently, they must have very thick dielectric layers relative to the thickness of the dielectric layers of the '381 patent. As detailed above, the ceramic grains of Rutt are from 25X to 250X the size of the dielectric grains of the '381 patent. Also as detailed above, the dielectric layer thicknesses of Rutt are ~50X that disclosed in the '381 patent. Consequently, a POSITA would have been dissuaded from using Rutt to achieve the 200++ dielectric layer devices disclosed in the '381 patent.

183. Thus, a POSITA would have been dissuaded from combining Rutt with

Itamura (or any other prior art reference) to achieve the devices of '381 as the structure disclosed by Rutt simply does not and could not physically fit into the dimensions disclosed in the '381 patent. Additionally, the devices of Rutt do not exhibit appreciably either the piezoelectric or the electrostrictive effect, and thus acoustic noise emission is not an issue to be solved with these barrier layer devices.

184. Further, a POSITA would not have incorporated Rutt's teachings into Itamura because Itamura is not an IBLC. Rutt is primarily focused on varistors, but where its teachings are also applicable to capacitors, it is only in terms of IBLCs (See for example *Id*. at 2:35-41, 10:15-18).

185. Additionally, as described herein, a POSITA would have understood that the method and devices disclosed in Rutt are unnecessarily complicated, wasteful and expensive. A POSITA also would have understood that the devices of Rutt are inferior in internal structure, having internal knit lines and being susceptible to deleterious cracking, and or delamination, etc., as explained herein.

186. Further, the exaggerated growth of the ceramic grain structures disclosed in Rutt would increase piezoelectric and/or electrostrictive effects as it results in large, "blocky" grains, as illustrated in Fig. 2 and Fig. 3 of Rutt, which would exhibit enhanced piezoelectric or electrostrictive effect, which would further have dissuaded a POSITA from combining Itamura with Rutt as this would ***increase*** acoustic noise emission due to electrical signal related vibration in the MLCCs of

the ‘381 patent as explained above; contrary to the objective of the ‘381 patent.

D. Claims 3, 4, 6, and 7: Itamura and Rutt

187. Claims 3, 4, 6, and 7 depend from claim 1. As discussed above in section V.C, it is my opinion that the combination of Itamura and Rutt does not render claim 1 obvious. For those same reasons, it is my opinion that the combination does not render claims 3, 4, 6, and 7 obvious.

E. Claim 2: Itamura, Rutt, and Jeong

188. Claim 2 depends from claim 1. As discussed above in section V.C., it is my opinion that the combination of Itamura and Rutt does not render claim 1 obvious. For those same reasons, it is my opinion that the combination of Itamura, Rutt, and Jeong does not render claim 2 obvious.

F. Claims 8, 10, 11, 13-15, and 17-19: Itamura, Rutt, and Ahn

189. The Board’s institution decision as to claim 8 is based on the combination of Itamura, Rutt, and Ahn. As described below, it is my opinion that this combination does not render claim 8 obvious.

190. Claim 8 includes the same limitation of claim 1, that “an average number of dielectric grains in a single dielectric layer in a thickness direction thereof is 2 or greater.” Petitioner AVX concedes that neither Itamura nor Ahn disclose or teach “an average number of dielectric grains in a single dielectric layer in a

thickness direction thereof is 2 or greater." Petitioner instead points to the teachings of Rutt for claim 8, as it did for claim 1. For the same reasons discussed above in section V.C., it is my opinion that the combination does not render claim 8 obvious.

191. Further, it is my opinion that a POSITA would have been dissuaded from using the electrode pad designs of the embodiments associated with Fig. 5 and Fig. 6 of Ahn (see e.g., *Id*. at pars. 0075-0080, Fig. 5, Fig. 6) in combination with Itamura, as use of such a configuration would result in increased inductance as discussed herein.

192. For those same reasons, it is my opinion that the combination does not render claims 10, 11, 13-15, and 17-19 obvious.

193. For the reasons discussed above and below, it is my opinion that the combination of Itamura, Rutt, and Ahn does not render claim 18 unpatentable.

194. Claim 18 recites:

> "18. The board of claim 17, wherein the first and second electrode pads are offset to each other in a width direction of the multilayer ceramic capacitor."

195. As explained above, a POSITA would have understood that "the first and second electrode pads are offset to each other in a width direction of the multilayer ceramic capacitor" to mean that each electrode pad of a first polarity connected to the multilayer ceramic capacitor is out of line, in the width direction, from all electrode pads of a second polarity connected to the capacitor.

196. Petitioner AVX concedes that neither Itamura nor Rutt disclose or teach "the first and second electrode pads are offset to each other in a width direction of the multilayer ceramic capacitor." Petitioner instead points to the teachings of Ahn. However, as discussed above, Ahn does not teach offset electrodes.

197. As discussed above, the definition of offset is to "place out of line" or "the amount or distance by which something is out of line." None of the embodiments in the Ahn patent are offset in the width direction of the capacitor in this manner; each is in line with another opposite polarity electrode pad in the width direction of the mounted, or to be mounted, capacitor. Further, Ahn does not mention the word "offset." For at least these reasons, a POSITA would have understood that Ahn pertains, in all cases, only to circuit board structures wherein the electrode pads are in line with another electrode pad of opposite polarity in the width direction of the mounted device.

198. Further, Ahn teaches only that noise can be reduced by implementing its two inventive features: (1) mounting the capacitor on the board so that its internal electrodes are horizontal, and (2) reducing the height of the solder used to connect the capacitor to the electrode pads. (see for example *Id*. at Abstract, pars. 0004, 0022, 0059). Ahn does not disclose reduced acoustic emission resulting from circuit board electrode pad configuration as in the '381 patent.

199. Further, a POSITA would have been dissuaded from using the electrode

pad designs of the embodiments associated with Fig. 5 and Fig. 6 of Ahn (see e.g., *Id*. at pars. 0075-0080, Fig. 5, Fig. 6) in combination with Itamura, as use of such a configuration would result in increased inductance, which is contrary to the objective Itamura, as well as the objective of the '381 patent (i.e., a low ESL (inductance), low acoustic noise emission, ferroelectric-type, high *C/V* MLCC and associated configuration of said device mounted to a PCB). A POSITA would have been dissuaded because the reduced amount of solder and the relatively small pads that are placed near the corners of the mounting perimeter of said MLCC would result in increased inductance (ESL) of the mounted device, and thus would work against the low inductance objective of Itamura, and in combination with Itamura, would work contrarily to the low inductance objective of the '381 patent.

200. This is because the inductance of the mounted device depends upon the inductance of the MLCC itself as well as upon its mounting configuration as explained above). Since the inductance of a conductor increases as the conductor is reduced in cross sectional area (i.e., less solder and lower solder fillet height, as well as less width dimension of two pads on a side with a gap in between, compared to one wide pad covering the entire width of the device or more as illustrated below), and since the inductance of a conductor increases as the length of the inductor increases (e.g., increased current path within the mounted MLCC, due to separated mounting pads), and since the inductance of a conductor increases due to mutual

inductance effect of closely spaced conductors that flow current in the same direction, the inductance of the mounted device configuration would increase if configured as disclosed in Ahn.

201. Thus, a POSITA would not have expected to achieve low ESL or to reduce ESL from an MLCC device mounted as disclosed by the embodiments associated with Fig. 5 and Fig. 6 of Ahn (*Id*. at pars. 0075-0080). Thus a POSITA would be dissuaded from using Ahn to achieve said objective of the '381 patent (i.e., a mounted, low ESL device).

G. Claim 9: Itamura, Rutt, Ahn, and Jeong

202. Claim 9 depends from claim 8. As discussed above in section V.F., it is my opinion that the combination of Itamura, Rutt, and Ahn does not render claim 8 obvious. For those same reasons, it is my opinion that the combination of Itamura, Rutt, Ahn, and Jeong does not render claim 9 obvious.

H. Claim 16: Itamura, Jeong, Rutt, Ahn, and EIA Standard

203. Claim 16 depends from claim 8. As discussed above in section V.F., it is my opinion that the combination of Itamura, Rutt, and Ahn does not render claim 8 obvious. For those same reasons, it is my opinion that the combination of Itamura, Jeong, Rutt, Ahn, and EIA Standard does not render claim 16 obvious.

VI. CONCLUSION

204. For the reasons explained above, it is my opinion that challenged claims 1–4, 6–11, and 13–19 of the '381 patent are not rendered obvious based upon the instituted grounds.

205. I reserve the right to supplement or revise this declaration based on any additional information that may become available to me in this matter.

206. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information or belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: September 29, 2017

Michael Randall, Ph.D.

LIST OF DOCUMENTS REVIEWED

All Documents mentioned in my Expert Report
All Documents in the LIST OF EXHIBITS
Ex. 1001 U.S. Pat. No. 9,326,381
Ex. 1002 U.S. Pat. No. 9,326,381 File History
Ex. 1003 Declaration of John Galvagni, PGR2017-00010
Ex. 1004 U.S. Patent 7,808,770 (Itamura)
Ex. 1005 U.S. Patent Application Publication US 2011/0141655 (Jeong)
Ex. 1006 U.S. Patent 5,134,540 (Rutt)
Ex. 1007 United States Patent Application Publication US2012/0152604 (Ahn)
Ex. 1009 EIA Standard EIA-595-A
Ex. 1011 CV of John Galvagni

LIST OF EXHIBITS

Exhibit	Paragraph No.	Description
A	6	Curriculum Vitae of Michael Randall
B	21	J. Cain, "Parasitic Inductance of Multilayer Ceramic Capacitors," AVX Technical Information, p. 4/4, June 1997
C	45	TDK, "Frequently Asked Questions Regarding: Singing Capacitors (Piezoelectric Effect)," December, 2006.
D	45	NIC Components Corporation, Piezoelectric Noise: "MLCC Ringing – Singing," REV. May 2015.
E	45	KEMET Electronics Corporation, "Piezeoelectric Effects Ceramic Chip Capacitors (Singing Capacitors)," Arrow Asian Times, 2006-08, J. Prymak
F	50	J.C. Tucker, "Actuation for Mobile Micro-Robotics," North Carolina State University
G	125	Design and Process Guidelines for Use of Ceramic Chip Capacitors, CALCE Electronic Products and Systems Center, University of Maryland, 2001
H	126	J. Maxwell, "Cracks: The Hidden Defect," AVX Technical Information, p. 9/10., 2000.
I	126	N. Blatau, et al., "Robustness of Surface Mount Multilayer Ceramic Capacitors Assembled with Pb-Free Solder," DfR Solutions
J	126	NIC Components, Corp., "MLCC - Ceramic Chip Capacitors / Failure Mode Study, Potential Failure Causes, Accelerators, Behavior."
K	126	N. Blatau, C. Hillman, "Design Guidelines for Ceramic Capacitors Attached with SAC Solder," DfR Solutions
L	126	CALCE EPSC, University of Maryland, "Ceramic Capacitor Failures on the Rise," 2001
M	126	A. Teverovsky, "Effect of Manual-Soldering-Induced Stresses on Ceramic Capacitors (Part I)," NEPP report, December, 2008.
N	146	Oxford Dictionaries: Definition of Stratum
O	156	Oxford Dictionary: Definition of Offset

Exhibit A

Michael S. Randall

313 River Walk Drive
Simpsonville, SC 29681
Phone: 864-608-1047
Michael@Almegacy.com

SUMMARY: Seasoned technologist, inventor, entrepreneur and economic development specialist with over 25 years of experience in R&D, product development, intellectual property, and business identification including design, materials, processing, testing and business development, having a strong track record of taking ideas to profitable products. An experienced consultant having provided expert services in the areas of electronic materials, components and assemblies, intellectual property, product development, process optimization, market studies, and grants. Recognized technical expert in electronic components and certified Six Sigma Black Belt (DFSS). Award winning author, inventor on more than 20 patents, lecturer, adjunct professor, entrepreneur, investor and technical consultant.

WORK EXPERIENCE:

9/03 to present	Almegacy LLC, VP Consulting
10/08 to 1/17	Health Sciences South Carolina, Chief Economic Development Officer
11/99 to 8/08	KEMET Electronics, Director Advanced Technology
10/97 to 11/99	Ferro Corporation, Ferro Electronic Materials Division, Director of Research and Development
10/92 to 10/97	AVX Corporation, Advanced Products and Technology Center, Manager of Ceramic Capacitor Research and Development
3/97 to 10/97	Webster University, Myrtle Beach Metropolitan Campus, Adjunct Professor
12/91 to 10/92	Engineering Consulting Firm of Gould, Lewis, and Proctor, Engineering Consultant
5/85 to 12/91	University of Florida, Graduate Research Associate
7/83 to 1/84	National Bureau of Standards (NIST), Research Engineer (Cooperative Education Program with Alfred University)

EDUCATION:

Aug 1993	PhD Materials Science and Engineering, University of Florida (GPA: 3.96/4.00)
May 1985	MBA Business Management, Webster University (GPA: 4.00/4.00)
Aug 1987	MS Materials Science and Engineering, University of Florida (GPA: 3.95/4.00)
May 1985	BS Ceramic Engineering, NYSCC at Alfred University, Minors in Chemistry and Business Management (GPA: 3.85/4.00) magna cum laude

SPECIALIZED EXPERIENCE:	Electronic Materials and Processing, Ceramic Dielectric Materials and Processes, Passive and some Active Electronic Components, Surface Mount Technology, Invention and Ideation, Reliability Assessment, New Product Development, Business Development, Economic Development, Expert Witness and Support, Grants, Intellectual Property, Product Liability
PROFESSIONAL TRAINING:	Technology Leader's Forum, DFSS/6σ Black Belt, Leadership, TOPS, DOE, QOS, FMEA
AWARDS:	KEMET (Club of Excellence, ELT, Best & Brightest), InnoVision Winner and Runner Up, Best Paper, Distinguished Writer, Outstanding Student, Scholarship
SOCIETIES:	AcerS, SMTA, IMAPS, MRS, AESF, $A\Sigma M$, $T\Beta\Pi$, $\Phi K\Phi$, $A\Lambda\Delta$
PUBLICATIONS/PRESENTATIONS:	Approximately 100 Total, 18 Invited, 2 Best Paper awards
SUBJECT MATTER EXPERT:	Multiple cases involving patents and product liability (ITC, PTAB, District Courts)
PATENTS:	19 U.S. Patents Granted, 2 Chinese, Additional US/WIPO patents pending
GRANTS:	Managed DARPA grant, assisted NIH GO Grant, ARRA/ONC HITECH Grant, ARPA-eBEEST Program award, The Duke Endowment, SC-Israel Collaborative (>$25M in grants total)
SESSION CHAIR/PANEL LEADER:	5 Symposia
PERSONAL:	US Citizen with active passport, married, 2 children

WORK EXPERIENCE:

9/03 to Present **Almegacy LLC**, Simpsonville, SC
Vice President, Consulting

- Consultant for ideation, invention, selection, sourcing, design, materials, processing, technology, IP and expert services, as well as equipment selection for electronic components
    - Electronic device and materials consulting including formulation, processing and testing development
    - Electronic component selection and sourcing for projects (active and passive)
        - Capacitors (SLC, MLCC, GBLC, Film, Ta, AE, EDLC/Supercapacitors, Hybrid/Pseudocapacitors, others), resistors (thick and thin film), inductors and terminators, batteries, oscillators, LEDs, integrated Circuits, microprocessors, transducers, power harvesters and sensors (mechanical and gas including smart sensors), thermoelectric devices, and other passive electronic components
    - Component reliability assessment and modeling
    - Adhesive/coating/potting/encapsulation selection
    - Management of PCB fabrication and assembly processes
    - Advisement on product compliance per specification, including RoHS and REACH
    - Electronic materials selection and sourcing including ceramics, metals, and organics
    - Device, materials and process development for materials and related electronic components
    - High temperature materials selection, evaluation, design and processing
    - High energy density storage materials and devices design and development assistance
    - Product development assistance including design, materials selection and sourcing, processing and related process equipment, test and analysis, packaging, intellectual property protection and marketing
- Technical marketing studies for emerging proprietary technologies, including devices, materials, test and measurement, and associated equipment, intellectual property and technologies
- Consulted on ARPA-e grant team BEEST Program Award Recapping, Inc.: High Energy Density Capacitors, program in coordination with Recapping (Khosla Ventures funded) and Pennsylvania State University
- Subject matter expert: Ceramic capacitors, providing expert advisement on characteristics of single and multilayer ceramic capacitors, Class 1, Class 2, and Class 3 dielectrics, examples:
    - Expert support for ex partes re-examination and inter partes review petitions to USPTO: US6,014,309, US6,144,547, US6,243,254, US6,266,229, US6,337,791, US6,377,439, US6,992,879
    - Expert support for inter partes review responses to USPTO: US6,661,639
    - Expert support for U.S. District Court for the Central District of California, case number 8:09-cv-01124, Murata Manufacturing Co Ltd. v. Samsung Electro Mechanics Co. Ltd., et al., Assisted successful defense against infringement claims regarding US Patents 6,014,309 6,243,254 6,266,229 6,377,439
    - Expert for ITC trial Investigation Number 337-TA-692, “In the Matter of Certain Ceramic Capacitors and Products Containing Same”, Murata v SEMCO. Assisted successful defense against infringement claims regarding US Patents 6,014,309 6,243,254 6,266,229 6,377,439
    - Expert support for ITC trial Investigation Number 337-TA-813, “Certain Electronic Devices With Graphics Data Processing Systems, Components Thereof, and Associated Software”, S3 Graphics v Apple. Assisted successful defense settlement against infringement claims regarding US Patent 5,581,279
    - Expert support for U.S. District Court for the Eastern District of Texas, case number 2:11-cv-00052, MicroUnity Systems Engineering, Inc. v. Apple, Inc., et al. Assisted successful defense settlement against infringement claims regarding US Patent 6,643,765
    - Expert support for U.S. District Court for the Southern District of California, case number 3:14-cv-02061, Presidio Components, Inc. v. American Technical Ceramics Corp., Assisted successful prosecution of infringement on claims regarding US Patent 6,816,356

- Expert for U.S. District Court for the Eastern District of New York, case number 2:14-cv-06544, American Technical Ceramics Corp., and AVX Corporation vs. Presidio Components, Inc. regarding US Patents 6,144,547, 6,337,791, and 6,992,879
- Expert for Fourth Circuit Court, Duval County Florida, product liability case number 16-2010-CA-001815, Gentleman v Medtronic. Assisted successful settlement for client
- Additional expert support

- Technical and market development advisor to several startup businesses in the field of passive electronic components (high temperature, high energy density storage devices and materials, high temperature gas sensing systems)
- Instructor, seminar on patent portfolios and intellectual property at CARTS USA 2011
- Invited instructor, seminar on intellectual property at SmartState™ Council of Endowed Chairs, May 2013
- Invited speaker for ASM seminar, October 2014
- Invited lecturer for BioE 8600, Introduction to Common Machining/Manufacturing Techniques for Medical Devices, Good Manufacturing Practices, October 2015
- Invited lecturer for BioE 8600, "Manufacturing Technology for Implantable Electronic Medical Devices:
- Processes, Verification, Validation and Scale-up," November 2016
- Adjunct professor in Bioengineering, Clemson University
- Technical blogger for "The Circuit: A Blog for Engineers," http://www.venkel.com/blog
- Marketed IP rights to patent portfolio for emerging technology company
- Client base includes more than 40 clients, from "start up" to "Fortune 100"

10/08 to 1/17 Health Sciences South Carolina, Columbia SC

Chief Economic Development Officer

- Assisted economic and business development at HSSC and 12 sponsored Centers of Economic Excellence
- Intellectual property development, 7 Idea disclosures/applications, 2 US Patents granted, 1 technology license
- New Product Design, Development and New Business Development
- Strategic planning
- Selection and implementation of advanced, HSSC-wide, clinical analytics system
- Promoted networking between member organizations and external organizations to provide business, legal, information and government services needed by member organizations
- Assisted organizations in finding and developing relationships with allied organizations
- Assisted establishment of businesses in South Carolina, promoting quality job creation in South Carolina
- Team member of an ARRA Grand Opportunities ("GO") Grant (RFA OD 09-004. CFDA 93.701) to establish unique Research Permissions Management System, $4.3M award
- Team member of an ARRA/ONC RC HITECH RC Grant (EP-HIT-09-003) to establish CITIA-SC, $6.4M award
- Team member for The Duke Endowment Grant II to HSSC, $11.25M award
- Team member for SC-Israel Collaborative Industry R&D Program Grant, $1M Total budget
- Member of the Board of Directors, NXT Health
- Member of the Economic Advisory Board and the Board of Directors of Clemson University Department of Bioengineering
- Established EDAC (Economic Development Advisory Committee) for HSSC membership
- Established Vendor Selection Committee for CITIA-SC (South Carolina's REC) and managed and performed contract review and negotiations for EHR vendor and Analytics Software vendor selection activities
- Assisted development of statewide clinical trials and research system plan
- Established HEAL SC (Health Economy Advancement Legacy for South Carolina) symposium, South Carolina's first statewide health sciences related economic development summit
- Organized SC Collaborative at BIO International
- Represented HSSC at numerous meetings as a Panelist, Panel Leader or Information Conveyor

1/05 to 8/08 **KEMET Electronics**, Advanced Technology Group, Simpsonville, SC
Director, Advanced Technology

- Business identification, demand creation, invention and NPD for 7 new advanced products from ideation to pilot scale addressing more than $450M in potential markets
    - D-Stick (low inductance feed through decoupling capacitor)
    - Controlled ESR D-Stick
    - D-Pack (ultra-low inductance feed through capacitor array)
    - L-CAP (low cost, two terminal low inductance capacitor)
    - Controlled ESR L–CAP
    - K-SIP (decoupling capacitor array interposer for SIP packaging)
    - V-Max (very high capacitance density hybrid dielectric capacitor system)
- Development of non-destructive screening method for enhancement of device reliability
- Intellectual property generation and searches for patentability and product clearance Internal expert for Ceramic Business Group NPD activities
- Technology assessment for due diligence for M&A efforts resulting in successful acquisition of Evox Rifa Oy
- Enhancement of customer relations through specialized designs and prototype evaluations
- Partnering and open innovation activities with customers, suppliers, universities, and government agencies
- Member of Extended Leadership Team (ELT)
- Member of the Club of Excellence (2007 and 2008)
- KEMET Special Recognition Award
- KEMET patent awards: More than 10 U.S. Patents granted U.S.
- Honorable mention in 10 press releases

4/03 to 1/05 **KEMET Electronics**, Technical Marketing and New Business Dev., Simpsonville, SC
Director of Ceramic Technical Marketing and New Business Development

- Quantification of $17B Capacitor Market Landscape
- Identification of $400M+ potential KEMET markets
- Produced and managed Advanced Products Portfolio
- Member of due diligence teams for 9 separate, investment/M and A opportunities
- Established business case and business risk assessment system
- Assisted Development of 4 new product lines
    - HV Commercial SMD MLCC
    - HV Leaded MLCC
    - Flex Robust MLCC
        - Open Mode, Soft Termination, Clip On Leadframe
    - Environmentally friendly, high CV COG MLCC
- Directed and managed technical support for all ceramic products
- Established highly effective system for competitor analyses/competitive intelligence

11/99 to 4/03 **KEMET Electronics**, Ceramic Technology, Ft Inn, SC
Director of Ceramic Technology

- Responsible for the direction of seven, process specific, functional teams, providing technology solutions for Multilayer Ceramic Capacitor (MLCC) development needs, including:
    - Mixing, Milling and Coating of Dielectric Tapes
    - Electrode Materials
    - Green Chip Processing
    - Thermal Processing and Corner Rounding
    - Termination Materials and Processing

    - Plating
    - Test and Failure Analysis
- Directed/Assisted Platform product development teams
    - COG, X5R and Y5V (PME and BME)
- Directed/Assisted non-platform development teams
    - Product performance improvement
    - Quality improvement
    - Cost and yield improvement
    - Employee and laboratory performance improvement
- KEMET university liaison for Ceramic Technology Department
- Directed or assisted/facilitated projects responsible for ≈70% of ceramic capacitor new product sales

9/98 to 11/99 **Ferro Corporation, Ferro Electronic Materials, CA (Formerly The Electronic Materials Division)**, San Marcos and Santa Barbara, CA
Director of Research and Development

- Responsible for planning, direction and oversight of all division level research and development and new product development, including the following product lines:
    - LTCC (Low Temperature Cofired Ceramic systems)
    - MMS (Multilayer Materials Systems)
    - OEM (Organic Electronic Materials systems)
    - PVS (Photovoltaic materials Systems)
    - RMS (Resistor Materials Systems)
    - TFS (Thick Film materials Systems)
- Directed new product development of more than 225 new line item products accounting for ~25% of FEM, CA FY99 total sales
- Established and managed an R&D/NPD group
- Established a comprehensive R&D information system
- Established and managed a process engineering group
- Established and managed a QA group
- Corporate level R&D interaction for division
- Division level interaction with external product development sources
- Managed divisional intellectual property
- Managed DARPA grant for high aspect ratio electrode printing on low loss dielectric packaging
- Member of Senior Management Committee

10/97 to 9/98 **Ferro Corporation, Electronic Materials Division**, San Marcos/Santa Barbara, CA
Manager of Research and Development

- Responsible for planning, management and oversight of all division level research and development and new product development including the product lines outlined above
- Managed new product development of more than 125 new line item products
- Responsible for all corporate level R&D interaction with division
- Established R&D new product development system
- Established R&D long term project portfolio

4/94 to 10/97 **AVX Corporation, Advanced Products and Technology Center**, Myrtle Beach, SC
Manager of Ceramic Capacitor Research and Development

- Responsible for planning and oversight of all multi-layered ceramic capacitor development
- Oversight of development of base metal, relaxor and conventional MLCC systems, high CV, low cost (Ni-metallurgy X7R and Y5V, Relaxor-based Y5V/Y5U)

- For high frequency applications (Cu-metallurgy COG)
- For harsh environments (X8R/other under-the-hood applications)
- Assisted Integrated Passive Component development

- Member of AVX Development Council
- Member of AVX Dielectric Strategy Committee
- Oversight Committee for competitor benchmarking
- Interface and assist corporate MLCC development at satellite plants (Myrtle Beach, SC, Conway, SC, Raleigh, NC, Olean, NY, Vancouver, WA, Coleraine, Ireland, Kyocera (Japan and USA))
- Member of Environmental, Health and Safety Council
- AVX Representative to the American Ceramic Industries Association

10/92 to 4/94 **AVX Corporation, Corporate Research Laboratory**, Conway, SC
Principal Engineer

- Responsible for pilot scale actuator green fabrication and thermal processing
- Project leader for piezoelectric voltage generator development
- Project leader for voided piezoelectric sensor project
- Developed various piezoelectric and electrostrictive devices

3/97 to 10/97 **Webster University, Myrtle Beach Metropolitan Campus,** Myrtle Beach, SC
Adjunct Professor (part time (weekends) while working at AVX)

- Instructor for BUSN 6080: Management Information Systems
- Instructor for BUSN 6150: Business Communications and Technology
- Assisted establishment of computer/communications lab for new, state-of-the-art campus (LAN, ISP, presentation system, etc.)

12/91 to 10/92 **The Engineering Consulting Firm of Gould, Lewis and Proctor**, Gainesville, FL
Engineering Consultant

- Designed, built and maintained a direct tension, multi-station, hydraulic apparatus for investigation of and characterization of accelerated stress corrosion cracking and hydrogen embrittlement of high strength steel reinforcement wire used in pre-stressed concrete pipe.
    - Equipment payback achieved within 2 months of implementation. System proved highly reliable and highly profitable.
    - Received a bonus and a raise as reward for the uniqueness, functionality and profitability of the direct tension mechanical test system

5/85 to 12/91 **University of Florida**, Gainesville, FL
Graduate Research Assistant

- Performed graduate level research in the areas of phase separation and crystallization in heavy metal fluoride glasses (Master's research) and in the area of low dielectric loss electronic packaging materials (Doctoral research)
- Designed and outfitted a general purpose research laboratory

7/83 to 1/84 **National Bureau of Standards** (now NIST), Gaithersburg, MD
Research Engineer (Cooperative Education Program with Alfred University)

- Characterized the high TiO_2 end of the BaO/TiO_2 binary phase diagram via XRD on samples prepared via a drop-tube quench furnace
- Characterized the high Li_2O end of the Li_2O/Al_2O_3 binary phase diagram via XRD on samples heat treated in controlled atmosphere or microtorr furnaces
- Rebuilt/redesigned intermediate temperature, microtorr vacuum furnace

- Investigated PSZ/SiC(w) composite precursor powder-whiskers, produced via spray drying, using optical microscopy, SEM, ASEM, and LS particle size analysis
- Assisted set up of a powder processing/characterization laboratory

EDUCATION:

University of Florida, Gainesville, FL
Degree: Ph.D. Materials Science and Engineering, August 1993
GPA: 3.96/4.00
Dissertation: Processing, Characterization and Modeling of Low Dielectric Constant, Low Dielectric Loss, Porous Composites for Use in High Frequency Applications
Candidacy Defense: "SSACTECD: Smart-Switched, Actively Controlled Transmissive, Electrochromic Device"
Advisors: Prof. J. H. Simmons, Prof. M. D. Sacks

Webster University, St. Louis, MO (Myrtle Beach, SC Campus)
Degree: M.B.A. Business Management, May, 1995
GPA: 4.00/4.00
Thesis: Case Study: Kyocera Corporation

University of Florida, Gainesville, FL
Degree: M.S. Materials Science and Engineering, August, 1987
GPA: 3.95/4.00

Thesis: Immiscibility and Crystallization in the Cadmium-Lithium-Aluminum-Lead Fluoride Glass System
Advisor: Prof. J. H. Simmons

N.Y.S. College of Ceramics at Alfred University, Alfred, NY
Degree: B.S. Ceramic Engineering, May, 1985
Minors: Chemistry, Business Management
GPA: 3.85/4.00, Magna Cum Laude
Thesis: Characterization of PTCR Behavior in $BaTiO_3$-Based Thermistors
Advisor: Prof. V. R. W. Amarakoon

SPECIALIZED EXPERIENCE:

- Ideation and Invention: Inventor on more than 20 patents. Brainstorming Sessions, Options Selection and Projects Portfolio Establishment and Management
- Basic Design and Performance Modeling: Passive Electronic Components: Multilayer Devices (MLCC, Multilayer Arrays, Low ESL MLCC, Controlled ESR MLCC, Multilayer Piezo Devices, Film Capacitors, Electrolytic Capacitors, EDLC/Supercapacitors, Hybrid/Pseudocapacitors), Thick Film Devices, EMI Filters, LTCC
- Formulation: Dielectrics, Glasses, Thick Film Pastes, Organic Vehicles, Additives and Modifiers
- Synthesis: Ceramic (Barium Titanate, BCT, BCTZ, Calcium Titanate, Calcium Zirconate, PMN/PT, PZT, Glass), Organic (Uniform Polystyrene Latex Particles, Polymethylmethacrylate)
- Powder Processing and Characterization: Batching, Milling, Mixing, Dispersing, Classifying, Coating/Pressing, Surface Area, Particle Size Analyses, Microscopy, Bulk Chemistry, Surface Chemistry, Density (Tap, Pycnometer, Bulk), Porosity (Archimedes, Hg Porosimetry), X-Ray Diffraction, FTIR, ICP, Rheometry (Liquid Viscometry), Fraction Solids (Organic and Ceramic), Other
- Microscopy and Associated Analytical Techniques: Optical, ASEM, ATEM, sample preparation techniques and data interpretation
- Analytical Testing Techniques: ICP, LAMS, XRF, XRD, TGA/DTA, DSC, TMA
- Thermal Processing: Low and High Temperature, Controlled Atmospheres (Vacuum, Inert and Reactive Atmospheres), Microwave Sintering

- Finishing: Corner Rounding, Thick Film Conductors, Plating (Electroless and Electrolytic)
- Device Sorting, Testing and Packaging: Capacitance, Dissipation Factor, Dielectric Constant, Dielectric Withstanding Voltage, Dielectric Breakdown Strength, Insulation Resistance, Temperature Coefficient of Capacitance, Field Effect, Dielectric Aging, Tape and Reel, Other
- Reliability Testing: Thermal Shock, Thermal Cycling, Highly Accelerated Life Test, Life Test, Temperature Humidity Bias Test, Non Destructive Test (CSAM and SLAM), Other
- Analysis and Failure Analysis
- Guidance of product performance vs. specification (Military, Aerospace, Automotive, other)
- Management of board builds including working with PWB fabricators and assemblers, conformal coating selection and RoHS advisement
- Mechanical Characterization: Tension, Torsion, Flexural, Wrap, Pull, and Microhardness Indentation, Fatigue Acceleration, Lamination/Bond Strength
- Technology Management/Direction: Personnel/Group Management, Project Management, Technology Management, Strategic Analysis, Portfolio Management, Acquisition Analysis and Due Diligence, IP and IP Portfolio Management, Quality Management
- Market Analysis and Business Identification: Electronic Market Segments Analysis, Competitive Intelligence/Analysis, Product Portfolio Management, Roadmap Establishment and Management, Economic Analysis
- Ideation, Technical Author, Statistical Analysis, Lean Design, Design for Manufacturability, Process Design, Grant Writing, Grant Budgeting and Management, Expert witness, Expertise in Multilayer Passive Electronic Components and Related Design, Materials, Processing, Testing and Markets

PROFESSIONAL TRAINING AND CERTIFICATIONS:

- Team Oriented Problem Solving (TOPS II/TOPS III, Global 8D, Ford Sanctioned)
- Design of Experiments (DoE, StorageTek, KEMET, Minitab Sanctioned)
- Failure Modes and Effects Analysis (FMEA, Ford Sanctioned)
- QV2000/Quality Operating System (QOS, AVX Sanctioned)
- A Leadership Course In: Effective Employee Motivation (Dun and Bradstreet)
- A Leadership Course in: Effective Time Management (Dun and Bradstreet)
- Making Managers Into Leaders (Enlightened Leadership International)
- Project Management Training (CareerTrack)
- Managing Multiple Projects and Priorities (Fred Pryor)
- The Seven Habits of Highly Successful People (Stephen Covey, Fred Prior Sanctioned)
- Personal Productivity (The Leadership Group Sanctioned)
- Effective Leadership Skills (The Leadership Group Sanctioned)
- Project Planning with Microsoft Project (Sam Brooks Associates, Microsoft sanctioned)
- Benchmarking: An Introduction (AVX sanctioned)
- Technology Forum (KEMET Sanctioned)
- Lean Six Sigma, Design for Six Sigma (Green Belt and Black Belt Trained and Certified)
- Licensed Real Estate Salesperson, State of South Carolina, Lic #46203
- KEMET Technology Leadership Forums 1 and 2

AWARDS:

- Member, KEMET ELT (Extended Leadership Team, 2005-2008)
- Member, KEMET Club of Excellence 2007, 2008
- Noted as one of KEMET's Best and Brightest (KEM press release, December 19, 2006)
- Innovision Awards Finalist (D-Pack), 2006
- Innovision Awards Winner (Green BME COG), 2007
- KEMET Special Recognition Award, 2008

- KEMET Patent Awards, 2006, 2007, 2008
- John D. Moynihan Best Paper Award, CARTS USA 2003
- Distinguished Writer Award, AVX Corporation, Recipient (1995, 1996, 1997)
- University of Florida President's Recognition for Outstanding Students (1992)
- University of Florida Graduate Council Fellowship, Recipient (1985-1986)
- Alfred University Southern Tier Scholarship, Recipient (1981-1985)
- New York State Regents Scholarship, Recipient (1981-1985)

SOCIETIES:

ACerS Reviewer for Journal of the American Ceramic Society, 2011-Present, Director of History and Personnel, Electronics Division 2005, ACerS Director of Corporate Membership, Electronics Division 2006, ACIA Board Member, Session Chair, Committee Chair for Electronic Division History and Personnel Committee, ACerS (technical reader for Ceramic Transactions 19: Advanced Composite Materials 1988), Keramos (University of Florida Secondary Founder, Secretary, Treasurer 1986), MRS, ISHM/IMAPS (founded the University of Florida Chapter 1986, Board Member of So Cal IMAPS, Editor of So Cal IMAPS Newsletter 1997), SMTA, AESF, IEEE, Alpha Sigma Mu, Tau Beta Pi, Phi Kappa Phi, Alpha Lambda Delta

SELECT PUBLICATIONS, POSTERS AND PRESENTATIONS:

- M. Randall, "Manufacturing Technology for Implantable Electronic Medical Devices: Processes, Verification, Validation and Scale-up," invited lecture, Clemson University Department of Bioengineering, BioE 8600: Biomedical Engineering Device Design Innovation, November 18, 2016.
- M. Randall, "Part I: Introduction to Common Machining/Manufacturing Techniques for Medical Devices and Good Manufacturing Practices," invited lecture, Clemson University Department of Bioengineering, BioE 8600: Biomedical Engineering Device Design Innovation, October 23, 2015.
- M. Randall, "Business Plans," invited lecture, University of South Carolina Arnold School of Public Health, HSPM 791: Healthcare Innovations, June 22, 2015.
- M. Randall, "A Farad on the Head of a Pin for Free," invited talk ASM Greenville SC, October 23, 2014.
- Invited panelist, Healthcare: IT-Ology Summit on Information Technology, Columbia SC April 23, 2014.
- Invited panelist (Moderator), Health IT: SCBIO Face to Face, Charleston, SC November 14, 2013.
- M. Randall, "Optimize and Protect Your Patent Portfolio," invited talk, South Carolina SmartState™ Council of Chairs Meeting, Columbia SC, May 15, 2013.
- J. Gasque, M. Randall, W. Harrell, G. Alapatt, "Better Impedance Measurement Using Kelvin-Type Test Fixturing," CARTS International 2012 Proceedings, Las Vegas, NV, pp. 157-185, March, 26-29, 2012.
- M. Randall, "Optimize and Protect Your Patent Portfolio," invited instructor, for-fee seminar," CARTS USA 2011, Jacksonville, FL, 9:00am to Noon, March 28–30, 2011.
- M. Randall, "Electronic Health Records: Vendor Selection Process and Next Steps," South Carolina Primary Health Care Association Annual Conference, Invited Talk, Myrtle Beach, SC, October 15-17, 2010.
- M. Randall, "SEMCO MLCC Tutorial Presentation," Trial Investigation Number 337-TA-692, "In the Matter of Certain Ceramic Capacitors and Products Containing Same," Presentation to the Court of the International Trade Commission, Washington D.C., July 21, 2010.
- M. Randall, "CITIA-SC Vendor Selection and Group Purchasing Committee Update," SCORH Rural Health Clinic Meeting, Invited talk, Columbia, SC, June 9, 2010.
- M. Randall, "Vendor Selection and Group Purchasing Committee Update," HIT SC Summit #8, Invited talk, April 22, 2010.
- M. Randall, "A Statewide Clinical Trials System," Invited talk, 2nd Annual South Carolina Human Research Conference, Greenville, SC, November 13, 2009.

- J. Prymak, M. Randall, P. Blais, B. Long, P. Staubli, E. Chen, “Why 47 uF Capacitor Drops to 37 uF, 30 uF, and Lower,” CARTS Europe 2008 Proceedings, Helsinki, Finland, October 20-23, 2008.
- J. Prymak, E. Reed, R. Hahn, M. Randall, P. Blais, B. Long, “Decoupling Solutions,” CARTS USA 2008 Proceedings, Newport Beach, CA, March 18–20, 2008.
- J. Prymak, M. Randall, P. Blais, B. Long, “Why That 47 uF Capacitor Drops to 37 uF, 30 uF, or Lower,” CARTS USA 2008 Proceedings, Newport Beach, CA, March 18–20, 2008.
- J. Prymak, E. Reed, M. Randall, P. Blais, B. Long, “Decoupling Solutions,” PCI (Passive Components Industry) Magazine, pp. 8-13, January-February, 2008.
- M. Randall, T. Kinard, J. Qazi, R. Hahn, P. Lessner, A. Tajuddin, S. Trolier-McKinstry, S. Ko, T. Dechakupt, C. Randall, E. Dickey, “Hybrid Dielectric,” 13th US-Japan Seminar on Dielectric and Piezoelectric Ceramics, pp. 315-18, Hyogo, Japan, November 4-7, 2007.
- M. Randall, J. Prymak, M. Laps, G. Renner, E. Chen, K. Lai, “D-Pack 3D Interposer Decoupling System”, CARTS Asia 2007 Proceedings, Taipei, Taiwan, October 9 – 13, 2007.
- R. Hahn, M. Randall, J. Paulsen, “The Battle for Maximum Volumetric Efficiency – Part 1: When Technologies Compete, Customers Win,” CARTS Europe 2007 Proceedings, pp. 63-73, Barcelona, Spain, October 29 – November 1, 2007.
- M. Randall, T. Kinard, J. Qazi, R. Hahn, P. Lessner, S. Trolier – McKinstry, S. Ko, S. Lu, T. Dechakupt, C. Randall, E. Dickey, “The Battle for Maximum Volumetric Efficiency – Part 2: Advancements in Solid Electrolyte Capacitors,” CARTS Europe 2007 Proceedings, pp. 25-36, Barcelona, Spain, October 29 – November 1, 2007.
- M. Randall, J. Prymak, M. Laps, G. Renner, P. Blais, P. Staubli, A. Tajuddin, “D-Pack 3D Interposer Decoupling System,” CARTS Europe 2007 Proceedings, pp. 147-161, Barcelona, Spain, October 29 – November 1, 2007.
- X. Xu, A. Gurav, M. Randall, J. Magee, M. Laps, A. Tajuddin, “BME C0G MLCC: The High Capacitance Class - I Solution,” CARTS Europe 2007 Proceedings, pp. 277-284, Barcelona, Spain, October 29 – November 1, 2007.
- P. Blais, M. Carter-Berrios, M. Randall, B. Sloka, M. Laps, G. Renner, J. Prymak, A. Tajuddin, “Decoupling Solutions,” Automotive Electronics Council, Component Technical Committee Proceedings, May 22-24, 2007.
- X. Xu, P. Pinceloup, A. Gurav, M. Randall, A. Tajuddin, “High Reliability, Thin Layer BME X7R Dielectric with only a Few Core-Shell Grains,” Proceedings of the 15th IEEE International Symposium on the Applications of Ferroelectrics, ISAF 2006, pp. 17-20, 2007.
- S. Ko, H. Nagata, E. Hong, S. Trolier-McKinstry, C.A. Randall, P. Pinceloup, M. Randall, A. Tajuddin, “Micro-Contact Printed Thin Film Capacitors,” IEEE International Symposium on the Applications of Ferroelectrics, Poster, ISAF 006.
- B. Sloka, D. Skamser, R. Philips, A. Hill, M. Laps, R. Grace., J. Prymak, M. Randall, A.Tajuddin, “Flexure Robust Capacitors,” CARTS USA 2007, The 27th Symposium for Passive Electronic Components, pp. 125-40, Albuquerque, NM, March, 2007.
- X. Xu, P. Pinceloup, A. Gurav, M. Randall, A. Tajuddin,” High VC BME COG MLCC, CARTS USA 2007, The 27th Symposium for Passive Electronic Components, pp. 179-88, Albuquerque, NM, March 26-29, 2007.
- M. Laps, R. Grace, J. Prymak, X. Xu, P. Pinceloup, A. Gurav, M. Randall, P. Lessner, A. Tajuddin, “Capacitors for Reduced Microphonics and Sound Emission,” CARTS USA 2007, The 27th Symposium for Passive Electronic Components, pp. 207-15, Albuquerque, NM, March 26-29, 2007.
- M. Randall, B. Sloka, M. Laps, G. Renner, J. Prymak, P. Blais, A. Tajuddin, “Decoupling Solutions,” CARTS USA 2007, The 27th Symposium for Passive Electronic Components, pp. 217-32, Albuquerque, NM, March 26-29, 2007.
- M. Randall, D. Skamser, T. Kinard, J. Qazi, A. Tajuddin, “Thin Film MLCC,” CARTS USA 2007, The 27th Symposium for Passive Electronic Components, pp. 403-15, Albuquerque, NM, March 26-29, 2007. This paper won the CARTS USA 2008 John D. Moynihan Award for Best Paper at the 2007 CARTS USA symposium.
- H. Nagata, S. Ko, E. Hong, C. Randall, S. Trolier-McKinstry, P. Pinceloup, D. Skamser, M. Randall, A. Tajuddin, “Micro-Contact Printed BaTiO3 and LaNiO3 Thin Films for Capacitors,” J. Am. Ceram. Soc., 89, [9], pp. 2816-2821, 2006.
- M. Randall, “Piezoelectric Materials,” Invited talk, Michelin Americas Research Center (MARC), May 22, 2006.

- P. Pinceloup, M. Randall, A Gurav, “BME-C0G MLCC with Ni Electrodes and the Role of Mn in CaZrO3-Based Dielectric,” CARTS US 26th Symposium for Passive Electronic Components, Orlando Fl, pp. 459-66, 2006.
- M. Randall, P. Blais, J. Prymak, M. Prevallet, D. Skamser, A. Gurav, P. Pinceloup, X. Xu, A. Tajuddin, P. Lessner, T. Ashburn, “Capacitor Considerations for Power Management,” CARTS US 26th Symposium for Passive Electronic Components, Orlando Fl, pp. 97-111, 2006.
- Y. Fang, M. Lanagan, D. Agrawal, G. Yang, C. Randall, T. Shrout, A. Henderson, M. Randall, A. Tajuddin, “An Investigation Demonstrating the Feasibility of Microwave Sintering of Base-Metal-Electrode Multilayer Capacitors,” Journal of Electroceramics, 15, pp. 13-19, 2005.
- H. Nagata, S. Ko, S. Trolier-McKinstry, C. Randall, P. Pinceloup, J. Beeson, D. Skamser, M. Randall, A. Tajuddin, “Microcontact Printed Thin Film Capacitors,” 12th US Japan Seminar on Dielectric and Piezoeletric Ceramics Nov. 6-9, Annapolis, MD, pp. 297-300, 2005.
- P. Pinceloup, A. Gurav, M. Randall, “Effect of Manganese Distribution on Properties of CaZrO3 - Based Ceramics,” 12th US Japan Seminar on Dielectric and Piezoelectric Ceramics Nov. 6-9, Annapolis, MD, pp. 293-296, 2005.
- M. Prevallet, S. Bagdy, J. Prymak, M. Randall, “High Voltage Considerations with MLCCs,” IEEE International Power Modulator Symposium and High Voltage Workshop, San Francisco, (2004).
- L. Mann, M. Randall, D. Barber, P. Pinceloupe, J. Beeson, G. Yang, C. Randall, “Is Core-Shell Grain Structure Required for Reliable, High VE, B-Type, BME MLCC?” 11th US-Japan Seminar on Dielectric and Piezoelectric Ceramics, Sapporo, Japan, (9-12, 2003).
- M. Randall, “High Volumetric Efficiency MLCC,” Plenary Lecture, 11th US-Japan Seminar on Dielectric and Piezoelectric Ceramics,” Sapporo, Japan, (September 9-12, 2003).
- G. Yang, E. Dickey, C. Randall, M. Randall, “Modulated and Ordered Defect Structures in Electrically Degraded Ni-BaTiO3 Mulitlayer Ceramic Capacitors,” J. App. Physics, 94 (9) 5990-5996.
- Y. Fang, H. Peng, D. Agrawal, M. Lanagan, M. Randall, “Rapid Sintering of Base-Metal-Electrode Mutlilayer Capacitors Using Microwave Technology,” Sintering 2003: An International Conference on the Science, Technology and Applications of Sintering, Session 9, Electronics and Technical Ceramics, Session Chair T. Kimura, Penn State University, (September15-17, 2003).
- Y. Fang, D. Agrawal, M. Lanagan, T. Shrout, C. Randall, M. Randall, A. Henderson, “Microwave Cofiring of Base Metal Electrode Capacitors.” Ceramic Transactions, Vol. 150, Ceramic Materials and Multilayer Electronic Devices, pp. 359-366, Editors: K.M. Nair, A.S.Bhalla, S.-I. Hirano, D. Suvorov, W. Zhu, R. Schwartz, pp. 359-366 (2004), The American Ceramic Society, 2003.
- Y. Fang, H. Peng, D. Agrawal, M. Lanagan, M. Randall, “Microwave Cofiring of Base-Metal-Electroded Ceramic Capacitors,” ACerS 105th Annual Meeting and Exposition, Nashville, TN, AM-S19-49-2003, (April 27-30, 2003).
- M. Randall, A. Gurav, L. Mann, J. Beeson, “Thin Layer BME MLCC Technology,” Invited talk, ACerS (The American Ceramic Society) 105th Annual Meeting and Exposition, Nashville, TN, AM-S19-96-2003, (April 27-30, 2003).
- M. Randall, A. Gurav, D. Skamser, J. Beeson, “Lifetime Modeling of Sub 2 Micron Dielectric Thickness BME MLCC, CARTS 2003,” pp. 134-140, (March 31-April 3, 2003).
- M. Randall, “Multilayer Capacitor Materials and Devices,” Invited talk, the 27th Annual Cocoa Beach Conference and Exposition on Advanced Ceramics and Composites (Held in conjunction with the Electronics Division of the American Ceramic Society), ECD-S3-39-2003, (January 26-31, 2003).
- M. Randall, “Precious and Base Metal Powders: Application in the Manufacture of Multilayer Ceramic Capacitors,” Invited talk, Clarkson Center for Advanced Materials Processing (CAMP) Meeting, Saratoga Springs, NY, (May 13-15, 2002).
- M. Randall, “High Volumetric Efficiency MLCC Components,” Invited talk, Penn State University Center for Dielectric Studies (CDS), State College, PA, (April 22-23, 2002).
- Gurav, M. Randall, L. Mann, “Selection of Nickel Powders for Base Metal Electrodes in MLCC,” CARTS 2002, St. Petersburg, FL, pp. 81-88, (March 25-29, 2002).

- L. Mann, J. Beeson, M. Randall, J. Paulsen, E. Reed, “Reliability of Base Metal Electrode Multilayer Ceramic Capacitors,” The tenth US-Japan Seminar on Dielectric and Piezeoelectric Ceramics, Providence, RI, pp. 39-42, (September 26-29, 2001).
- M. Randall, “A Case for Integrated MLCCs: The Effect of Design Factors on Maximum Capacitance and Volumetric Efficiency,” CARTS 2000, Huntington Beach, CA, pp. 195-203, (March 6-10, 2000).
- K. McVicker, G. Gunter, B. Fu, G., Sabo, M. Randall, “Organic Systems for Base Metal Multilayer Ceramic Capacitors,” CARTS 2000, Huntington Beach, CA, pp. 116-119, (March 6-10, 2000).
- U. Kumar, G. Gunter, M. Randall, “Low Temperature Firing Platable Silver Termination for Capacitors,” CARTS 2000, Huntington Beach, CA, pp. 234-239, (March 6-10, 2000).
- L. Chai, M. Randall, S. Turvey, “Ferro LTCC Systems for Wireless Packaging Applications,” IWPC Wireless Symposium/Portable by Design Conference & Exhibition at PCS’99, New Orleans, LA, (Sept. 21-24, 1999).
- L. Chai, M. Randall, “Novel Manufacturing Techniques in LTCC Technology,” IMAPS, Chicago-Milwaukee Meeting, (April 28, 1999).
- S. Turvey, M. Randall, “Ferro LTCC Systems—An Update,” IWPC Joint International Conference, Vancouver, Canada, (Feb. 21-23, 1999).
- M. Randall, S. Turvey, “Low Temperature Cofired Ceramic Tape Systems in Sensor Applications,” IMAPS Advanced Technology Workshop on Sensor Packaging, Ojai, CA, (Jan. 26-28, 1998).
- U. Kumar, J. Hock, B. Rawal, M. Randall, “Dielectric Properties of PMN Based Ceramic Under D.C. and A.C. Fields,” The Eighth US-Japan Seminar on Dielectric and Piezeoelectric Ceramics, Plymouth, MA, pp. 193-196, (October 15-18, 1997).
- U. Kumar, H. Pak, B. Rawal, M. Randall, “High Capacitance Value Multilayer Ceramic Capacitors from PMN Based Dielectrics,” CARTS 97: 17th Capacitor and Resistor Technology Symposium, pp. 286-291, (March 24-27, 1997).
- U. Kumar, M. Randall, A. Ritter, "Actuator Miniaturization," Invited Paper, Symposium on Micro-Integrated Smart Materials and Structures, Society for Experimental Mechanics, Williamsburg, VA, (Oct. 11-12, 1995).
- U. Kumar, M. Randall, J. Hock, A. Ritter, "Reliability Studies on Electrostrictive Actuators," Journal of Intelligent Material Systems and Structures, Vol. 5, No. 6, pp. 802-809, (1994).
- M. S. Randall, "Low-Loss Cofirable Ceramic Materials for High Frequency Applications," presented at KII 5 (Kyocera International Incorporated Annual Technical Conference), Vancouver, WA, (May 13-14, 1994).
- M. S. Randall, “Optimization of Actuator Burnout: Application of Controlled Rate of Weight Loss Thermal Treatment Schedules,” KII 4 (Kyocera International Incorporated Technical Conference), Myrtle Beach, SC, (April 16-17, 1993).
- M. D. Sacks, M. S. Randall, G. W. Scheiffele, R. Raghunathan, J. H. Simmons, "Processing of Silicate Glass/Silicon Nitride Composites with Controlled Microporosity," Ceramic Transactions, 19, The American Ceramic Society, Inc., Westerville, OH, pp. 407-420, (1991).
- M. S. Randall, M. D. Sacks, J. H. Simmons, "Processing of Borosilicate Glass/Silicon Nitride Composites Containing Controlled Porosity," presented at the Second International Ceramic Science and Technology Congress and Electronics Division Meeting, American Ceramic Society, Orlando, FL, (Nov. 12-15, 1990).
- M. S. Randall, J. H. Simmons, O. H. El-Bayoumi, "Primary and Secondary Phase Separation in CdF2-LiF-AlF3-PbF2 Glasses," J. Am. Cer. Soc., 71, [12], pp. 1134-41, (1988).
- M. S. Randall, C. J. Simmons, "Crystallization from Liquid-Liquid Immiscibility in Mixed Cadmium-Lead Fluoride Glasses," presented at the ACerS Annual Glass Division Meeting, Bedford, PA, (Sept. 30-Oct. 2, 1987).
- M. S. Randall, J. H. Simmons, "Primary and Secondary Phase Separation in Mixed Cadmium Lead Fluoride Glasses," presented at the ACerS Annual Glass Division Meeting, Bedford, PA, (Sept. 30-Oct. 2, 1987).

PATENTS:

- 6,162,849, “Thermally Conductive Thermoplastic,” Q. Zhuo, R.M.Harris, D.C. Skovran, L.F. Lightner, M.S. Randall, V. E. Stygar.
- 6,906,907, “Monolithic Multi-Layer Capacitor with Improved Lead-Out Structure,” J. D. Prymak, M.S. Randall., “Refractory Metal Nickel Electrodes for Capacitors,” D.E. Barber, A. Wang, M.S. Randall, A. Tajuddin.

- 7,211,740, “Valve Metal Electromagnetic Interference Filter,” M.S. Randall.
- 7,277,269, “Refractory Metal Nickel Electrodes for Capacitors,” D.E. Barber, A. Wang, M.S. Randall, A. Tajuddin.
- 7,280,342, “Low Inductance, High ESR Capacitor,” M.S. Randall, A. Hill, P. Blais, G. Renner, R. Vaughan, A. Tajuddin.
- 7,292,429, “Low Inductance Capacitor,” M.S. Randall, J. Prymak, A. Tajuddin.
- 7,545,623 and WO2008067300, “Interposer Decoupling Array Having Reduced Electrical Shorts,” M. Randall, G. Renner.
- 7,670,981 and CN101456731, “C0G multi-layered ceramic capacitor,” M.S. Randall, C. Antoniades, D.E. Barber, X. Xu, J. Beeson, P. Pinceloup, A. Gurav, T. Poole, A. Tajuddin, I. Burn.
- 7,916,451 and CN101456731, “C0G multi-layered ceramic capacitor,” M.S. Randall, C. Antoniades, D.E. Barber, X. Xu, J. Beeson, P. Pinceloup, A. Gurav, T. Poole, A. Tajuddin, I. Burn.
- 7,923,395 and CN101456731, “C0G multi-layered ceramic capacitor,” M.S. Randall, C. Antoniades, D.E. Barber, X. Xu, J. Beeson, P. Pinceloup, A. Gurav, T. Poole, A. Tajuddin, I. Burn.
- 7,958,627, “Method of attaching an electronic device to an MLCC having a curved surface,” M.S. Randall, C. Wayne, J. McConnell.
- 8,111,524 and CN101632173, “Electronic Passive Device,” M. Randall, G. Renner, J. Prymak, A. Tajuddin.
- 8,293,323 “Thin Metal Film Conductors and Their Manufacture,” S. Trolier-McKinstry, C.A. Randall, S.W. Ho, M.S. Randall.
- 8,414,962, “Microcontact Printed Thin Film Capacitors,” S. Trolier-McKinstry, C.A. Randall, H. Nagata, P. I. Pinceloupe, J.J. Beeson, D.J. Skamser, M.S. Randall, A. Tajuddin.
- 8,717,774, “Electronic Passive Device,” M.S. Randall, G. Renner, J.D. Prymak, A. Tajuddin.
- 8,828,480, “Microcontact Printed Thin Film Capacitors,” S. Trolier-McKinstry, C.A. Randall, H. Nagata, P. I. Pinceloupe, J.J. Beeson, D.J. Skamser, M.S. Randall, A. Tajuddin.
- 8,895,940, “Switch Sanitizing Device,” J. Moskowitz, M. Randall
- 8,910,356, “Method of attaching an electronic device to an MLCC having a curved surface,” M.S. Randall, C. Wayne, J. McConnell.
- Additional applications in process

SESSION CHAIR:

- Workshop Facilitator for the High Volume MLCC Components Session of the Spring 2002 Meeting of the Center for Dielectric Studies, State College, PA, April 23-24, 2002.
- Session Chair for the Microwave and LTCC Materials Session of the 27th Annual Cocoa Beach Conference and Exposition on Advanced Ceramics and Composites, Cocoa Beach, FL, January 26-31, 2003.
- Session Chair for the BME Session of the Spring, 2003 Meeting of the Center for Dielectric Studies, State College, PA, April 24-25, 2003.
- Panel Leader for Face to Face Health Information Technology Breakout Panel, November, 2013.

COMMUNITY SERVICE:

- United Way
    - Executive Director, KEMET Corporate Campaign: Team raised over $250,000, a new record for KEMET
    - Assistant Director, KEMET Corporate Campaign
    - Member Palmetto Society
- CROP WALK
    - Manager for Eastminster Presbyterian Church
    - Board Member, CROP Walk Greenville, SC
    - CROPWALK Participant
- Golden Strip YMCA, Board of Directors 2004-2006, Property Team Director, 2006

    - Hollingsworth property development plan and approval
    - Golden Strip YMCA Improvement Plan, author and champion
    - Golden Strip YMCA, Board of Directors, 2005-2008
- Habitat for Humanity, Habitat Partner's Council
- Trees for the Future donor (enabling the planting of >110,000 trees)
- FLL: First Lego League team captain for Sterling School (Charles Townes Center)
- Junior Achievement Instructor (JA Economics, JA Interpersonal Skills, JA Our World Economics, JA Business Structure, JA Our Cities)
- Blood Donor, 3 Galloneer

PERSONAL:

- Married (Dr. Sara Pittman Elder Randall, Ph.D. Metallurgy, University of Florida, 1990)
- Children: Clarice (22) USC Honors College Dual Major Alumni, Henry (20) Clemson University Honors College Dual Degree Candidate (Junior)
- U.S. Citizen with active passport

REFERENCES: Available upon request

Exhibit B

TECHNICAL INFORMATION

PARASITIC INDUCTANCE OF MULTILAYER CERAMIC CAPACITORS

by Jeffrey Cain, Ph.D.
AVX Corporation

Abstract:

The parasitic inductance of multilayer ceramic capacitors (MLCCs) is becoming more important in the decoupling of high speed digital systems. There exists conflicting data and statements on the parasitic inductance of the MLCC. This work shows the measurement techniques of the inductance parameters, focusing mainly on the fixturing needed to accurately measure the chips. The effects of various compensation and calibration methods will also be demonstrated. A comprehensive table will be shown that includes the parasitic inductance for a range of MLCCs from 0402 through 1210.

PARASITIC INDUCTANCE OF MULTILAYER CERAMIC CAPACITORS

by Jeffrey Cain, Ph.D.
AVX Corporation

I. Introduction

The simplest equivalent circuit model of MLCCs, described in [1] is the series model. The circuit is shown in Figure 1.

Figure 1. Equivalent circuit model of MLCC.

The three elements being the capacitor, the parasitic inductance and series resistance. This paper will focus on the inductance and the methodology used to calculate it.

The parasitic inductance of MLCCs is becoming more and more important in the decoupling of today's high speed digital systems. The relationship between the inductance and the ripple voltage induced on the DC voltage line can be seen from the simple inductance equation:

$$V = L\frac{di}{dt} \qquad [1]$$

The $\frac{di}{dt}$ seen in current microprocessors can be as high as 0.3A/ns [2], with future generations looking at 10A/ns. At 0.3A/ns, 100pH of parasitic inductance can cause a voltage spike of 30mV. While this does not sound very drastic, with the Vcc for microprocessors decreasing at the current rate, this can be a fairly large percentage.

Another important, often overlooked, reason for knowing the parasitic inductance is the calculation of the resonant frequency. This can be important for high frequency, by-pass capacitors, as the resonant point will give the most signal attenuation. The resonant frequency is calculated from the simple equation

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \qquad [2]$$

This paper will discuss the measurement technique used to calculate the inductance, as well as different available methods. A comprehensive table will be given showing the various capacitor case sizes and a curve fit based on the lengths and widths will be derived.

II. Measurement

For this paper, the Hewlett-Packard impedance analyzer, HP4291A, was used exclusively. This analyzer has a frequency range from 1 MHz to 1.8 GHz. Perhaps even more important is the fixture, which was a HP16192A, SMD fixture. This fixture is rated for the entire frequency range of the HP4291A.

Calibration and fixture compensation are the most important procedures for generating relevant data. Open, short and load calibration must be done for the cables and test head, using the devices supplied by HP. Then the fixture compensation must be done, again using open, short and load. Using the pre-programmed compensations is not recommended, as environmental conditions can change day to day.

This compensation and calibration sequence is straight forward, until it comes to the shorting of the fixture. There are two techniques that can be used on the HP16192A. One is to use shorting blocks and the other is to slide the pins together and short them, both shown in Figure 2.

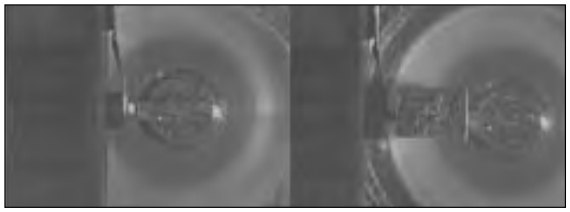


Figure 2. Photograph demonstrating the two shorting techniques for the 16192A fixture.

For an inductance measurement, the shorting blocks should not be used. The inherent inductance of the path length, of say and 0805 chip, is compensated out of the system. This is demonstrated in Figure 3 for an 0805, 0.1µF capacitor. Notice that the resonant frequency is shifted by 4.63 MHz, or 23%. Since the capacitance is identical, using equation [2]

$$\omega_1 = \frac{1}{\sqrt{L_1 C}},\ \omega_2 = \frac{1}{\sqrt{L_2 C}} \qquad [3a]$$

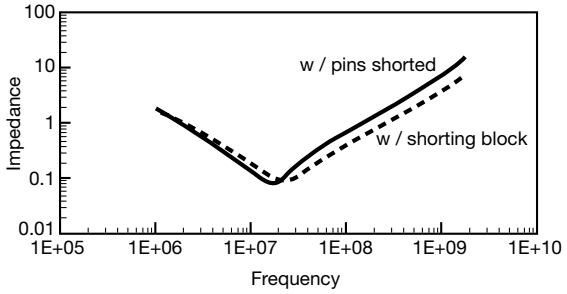


Figure 3. Shift in resonant frequency caused by using a shorting block in fixture compensation of HP16192A.

$$\frac{L_1}{L_2} = \frac{\omega_2^2}{\omega_1^2} \qquad [3b]$$

This implies that the ratio of L_1:L_2 is 0.59. That is to say, if the inductance measured by shorting the pins of the HP16192A is 1nH, using the shorting block for compensation will give an inductance value of 600pH! This is quite significant and cannot be ignored. For this paper, all data is generated by shorting the pins of the HP16192A together.

One more thing to consider, the HP4291 is an impedance analyzer which measures phase and magnitude. Only the real and imaginary part of the impedance can be calculated exactly. Referring to Figure 1, the impedance of a MLCC is

$$Z = R + j\left(\omega L - \frac{1}{\omega C}\right) \qquad [4]$$

The real part being R and the imaginary part $\omega L - \frac{1}{\omega C}$. One cannot possibly separate the inductance and capacitance from the reactance, one equation, two unknowns. Fortunately, one of the terms, inductive or capacitive, becomes much smaller than the other as the frequency moves away from resonance. That is to say as

$$\omega > \omega_{res},\ \omega L >> \frac{1}{\omega C} \qquad [5]$$

For this paper, all inductance numbers cited are taken from the 1 GHz measurement point. This frequency is far enough from resonance that the capacitive term is much smaller than the inductive term.

III. Results

All data was taken in one sitting, with the same calibration. This was done to ensure that even if the calibration was off, the relative change in inductance from case size to case size would remain intact. Figure 4 shows the impedance curves of four different case sizes with the same capacitance values of 0.1µF.

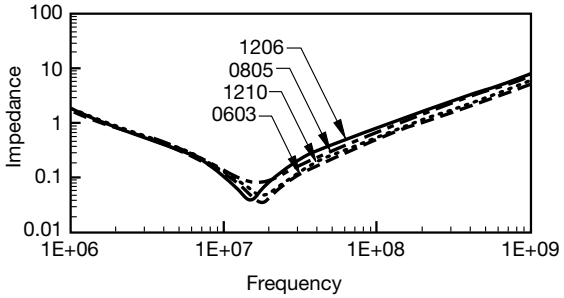


Figure 4. Impedance curves for 0.1µF capacitors.

Using the data from Figure 4, the typical inductance values are calculated to be:

MLCC Chip Size	Inductance (pH)
0603	870
0805	1050
1206	1200
1210	980

Table 1. Inductance values for 0.1µF MLCC.

It should be noted that error on a 10 piece sample run was ±7.4% across the entire range of chip sizes.

The next measurement set was to determine if the inductance value changed when more electrodes were used in a given package. In other words, is the inductance constant for different values of capacitance. Figure 5 shows the results for a 1206 package. All one needs to do is examine the impedance lines at the upper frequency limit to notice that the inductance does not vary by package type. After running 10 pieces of each value, the inductance number never differentiated by more than ±10%.

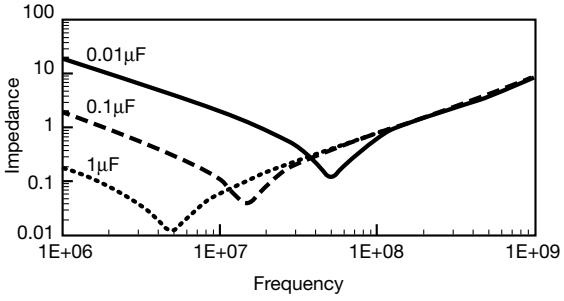


Figure 5. 1206, X7R impedance curves for a variety of capacitance values.

A variety of techniques have been employed to lower the parasitic inductance of MLCCs. The first method used was to terminate the MLCC along the long edges, thus turning a 1206 into an 0612. Figure 6 shows the comparison of a 0.1µF capacitors in both the 1206 and 0612 forms. Table 2 list the measured inductance values for both the 0612 and 0508.

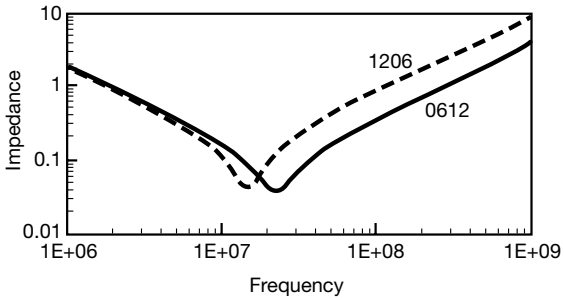


Figure 6. Impedance comparison of 1206 and 0612 form factors.

Chip Style	Inductance (pH)
0612	610
0508	600

Table 2. Inductance values of low inductance chips.

Once all of this information was compiled, an exponential curve fit was performed. The fit was centered around two x variables, namely the length to width ratio (L/W) and the length from one termination to the next. The following equation was derived:

$$L = 394.727 \times 1.052\text{^}L \times 1.317\text{^}(L/W) \quad [6]$$

Table 3 shows the difference between the curve fit and the measured data. The error is never greater than 12.4%, with the worst case being the 0805.

Chip Style	L/W	L	Fit	Measured
1210	1.2	12	1010	980
1206	2	12	1255	1250
0805	1.6	8	920	1050
0603	2	6	925	870
0612	0.5	6	615	610
0508	0.625	5	605	600

Table 3. Comparison of measured and fitted inductance values.

The model allows us to consider the inductance of future devices, such as an 0306, which yields an inductance value of 527 pH.

IV. Conclusions

This paper emphasizes the importance of a proper calibration method when attempting to calculate the parasitic inductance of surface mount capacitors. A curve fitting scheme is also highlighted as an aide to predetermine inductance values for various dimensions of MLCCs.

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AVX Southwest, AZ
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Exhibit C

Frequently asked questions regarding:

Singing Capacitors (Piezoelectric Effect)

Abstract

In some applications, design engineers are finding a vibration or low audible hum coming from certain ceramic capacitors. This is sometimes described as a singing capacitor and is actually a piezoelectric effect. This FAQ will discuss some aspects of this "singing capacitor" phenomena.

December, 2006

Singing Capacitors (Piezoelectric Effect)

Q1. ***What is a Singing Capacitor?***
A1. Singing is one of many ways to describe the piezoelectric effect on the capacitor. This "singing" is actually a vibration of the capacitor on the PCB that many occur under specific conditions.

Q2. Do all MLCCs exhibit a piezoelectric effect?
A2. The piezoelectric effect occurs in ferroelectric capacitors (i.e. class II & III). Class I capacitors are not ferroelectric and therefore do not exhibit a piezoelectric effect. It is also important to understand that not all ferroelectric capacitors will experience a piezoelectric effect. A specific combination of component construction and circuit usage conditions must exist in order to cause the capacitor to vibrate or ring.

Q3. What are some of the factors that can cause a MLCC to "sing"?
A3. There are several factors that contribute to the piezoelectric effect. There are contributing factors based on the design/construction of the MLCC, the electrical parameters of the MLCC, and the outside factors of the MLCC in circuit.

Design/construction contributors include the material dielectric constant, the number of active layers, the layer thickness, and the package size. Electrical contributors include DC bias.

Externally one of the most significant contributors is the application voltage and ripple current of the input signal. The threshold ripple is dependent on other external stresses applied to the MLCC. High temperature, for example, limits the ripple current capability of the MLCC and therefore can play a part in causing the capacitor to sing.

Q4. What generalizations can be made regarding the piezoelectric contributing factors?
A4. Each of the factors discussed here play a role in contributing to the piezoelectric effect. All of these contributing factors affect the piezoelectricity differently. These factors can work together to increase or decrease the piezoelectric effect. Due to this complexity, there is no easy way to offer any design guide rules of thumb.

As an example, we can look at layer count. With all design factors being the same, a capacitor with higher layer count (layer # ratio) would result in greater piezoelectric amplitude. This is simply because the total amplitude is the combined effect of the amplitude of each layer.

Contributing factors can also offset or decrease the piezoelectric effect. For example, a higher dielectric constant can offset the effects of DC bias. This would result in lower piezoelectric amplitude.

The details and physics behind each combination of contributing factors are beyond the scope of this paper. It is important to remember that the piezoelectric effect will not manifest without the correct combination of external factors.

Most problems can be avoided if the Design Engineer can optimize the quality of the incoming signal as well as the environment surrounding the circuit. If a piezoelectric problem still exists, the Design Engineer then needs to look at component selection and design.

December, 2006

Q5. Can this piezoelectric effect be measured?
A5. When evaluating component selection and design, it can be helpful to compare some form of piezoelectric intensity between different components. Therefore, a measurement method is needed any relative comparison can be made.

The piezoelectric effect is actually a vibration of the capacitor. This vibration causes capacitor displacement as shown in figure 1. This displacement can be measured as amplitude.

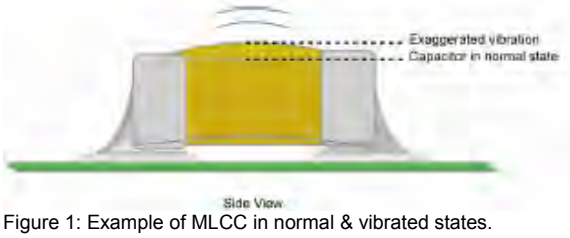


Figure 1: Example of MLCC in normal & vibrated states.

Since the vibration and displacement occurs on such a relatively small scale, a non-contact method should be used to actually measure the displacement. A device such as a laser vibrometer (figure 2) allows for accurate non-contact displacement measurements to be made.

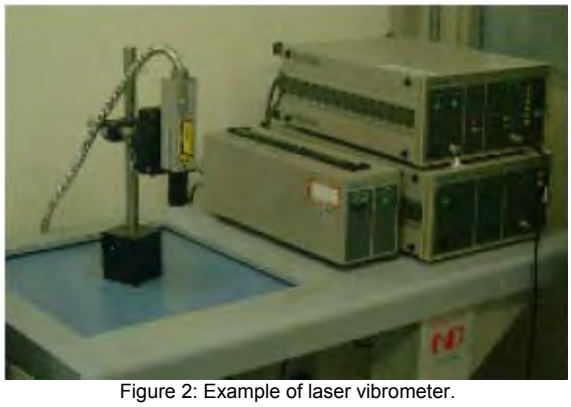


Figure 2: Example of laser vibrometer.

Q6. Is there a standard or specification for piezoelectric level?
A6. Currently is no industry standardized method for reporting piezoelectric level. The piezoelectric effect occurs as the result of a combination of many variables. The correlation on the degree of one variable against others also adds a layer of complexity. The piezoelectricity can be measured but is only useful as a relative comparison between different measurements.

Q7. If piezoelectric amplitude can be measured, can this be used to generalize MLCC performance?
A7. Table 1 shows an example of non-contact measurements several MLCCs. These amplitudes are based on specific input test signals. The Engineer cannot make general assumptions based on these measurements alone.

As discussed earlier (in question #4) the higher the layer # ratio, the greater the piezoelectric amplitude. This is because the total amplitude is the combined amplitude of each layer. This does not always mean that different designs with the same layer # ration will necessarily perform the same.

Looking at a simple example in table 1 you find two MLCCs (#4 & #5) with the same layer # ratio. Although MLCC #4 has the same layer # ration as MLCC #5, the amplitude in MLCC # 5 is higher. In this example, this is because MLCC #5 has a lower layer thickness ratio.

#	Item	Dielectric Constant	Layer # Ratio	Layer Thickness Ratio	DC Bias Factor	Amplitude @ $1V_{rms}$
1	C3225Y5V1E106Z	100	100	100	-90	15nm
2	C3225X7R1E475K	20	165	90	-30	25nm
3	C3225X7R1H155K	20	105	160	-13	11nm
4	C4532X7R1E475K	20	125	100	-25	12nm
5	C5750X7R1E106K	20	125	90	-30	14nm

Table 1: Example measurements.

Looking at another example, the first three MLCCs in table 1 shows that MLCC #2 measures the greatest piezoelectric amplitude. If the design engineer used multiple capacitors, the ripple current would be distributed between the capacitors. To keep the math simple, assume 10 capacitors are used in parallel.

Using MLCC #1, ten 10µF MLCCs in parallel gives a nominal effective capacitance of 100µF. A DC bias factor of -90 means that 10% of the capacitance is available after DC voltage is applied. 10% of 100µF is 10µF. Distributing the impedance between the ten MLCCs (10 caps / effective capacitance) gives an amplitude scale factor of 1 and therefore the resultant amplitude would be 15nm.

It follows that MLCC #2 would yield an effective capacitance of 33µF. The amplitude scale factor is 10/33. By multiplying this scale factor with the measured amplitude in table 1 results in the resultant amplitude of 8nm.

MLCC #3 would yield an effective capacitance of 13μF. The amplitude scale factor is approximately 10/13 and therefore the amplitude would be (25/3) approximately 8.5nm.

Based on these calculations, MLCC #2 measured the highest in Table 1 but is our best choice in the design.

This example shows that although the piezoelectric amplitude can be measured, the value alone can not determine the effect on a circuit. Clearly, the circuit design also plays an important factor.

Q8. If the piezoelectric effect is a vibration, what causes the "singing"?
A8. The piezoelectric effect is the vibration. The singing effect occurs under certain conditions of vibration. If the vibration frequency occurs within the audible range (approximately 20Hz – 20kHz) then you may also hear an audible hum. When the MLCC is soldered to a circuit board or substrate, the intensity of the audible noise may also intensify. What you could basically end up with is a crude speaker or even a microphone in your circuit board.

Q9. What can the Design Engineer do to reduce the "singing"?
A9. The engineer should determine if the vibration or humming is causing other problems in the overall system. For example, if the circuit is exhibiting a low frequency audible hum but will later be drowned out by the sound of a motor, the Engineer must decide if an improvement is necessary or not.

If the Engineer decides to improve the circuit, the first step is to look at reducing the ripple coming into the circuit. This will not only benefit the MLCC, but the entire circuit.

If ripple cannot be reduced, the Engineer can consider adding capacitors in parallel to distribute the ripple current or other stresses. It should be noted that this is not necessarily to increase bulk capacitance so the goal is not to simply provide the maximum capacitance value.

If the circuit does not require high capacitance then Class I (C0G) MLCC should be considered. Since Class I dielectrics are not ferroelectric, they will not exhibit the piezoelectric effect.

Q10. Is there long time reliability affects due to the capacitor singing?
A10. There is currently no conclusive test data that would suggest any reliability risk. A MLCC that does not exhibit any piezo vibration will result in equal or better reliability compared to a MLCC that does exhibit piezo vibration.

MLCCs already possess superior reliability as compared to competing technology. MLCC qualification tests such as those suggested in the Automotive "AEC-Q200" specification includes tests based on the Military standard Mil-Std-202. These tests contain a variety of environmental, mechanical, and electrical stress tests. Among them are two tests in particular that test for mechanical shock (Mil-Std-202 method 213) and vibration (Mil-Std-202 method 204). These tests apply an external stress to ensure the MLCC will withstand external shock and vibration stresses.

Additional resources:
For additional information that was referenced in this FAQ please see the following.

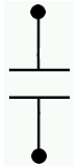
Mil-Std-202
CDF-AEC-Q200
Ripple Current for MLCCs, TDK FAQ

December, 2006

Exhibit D

NIC Components Corp.

Piezoelectric Noise: MLCC Ringing - Singing



Possible solutions for reducing or eliminating MLCC ringing – singing issues

- *Modified PCB materials or layout (page 3)*
- *Lower K Dielectric MLCCs (page 4)*
- *SMT Film Capacitors (pages 5 ~ 16)*

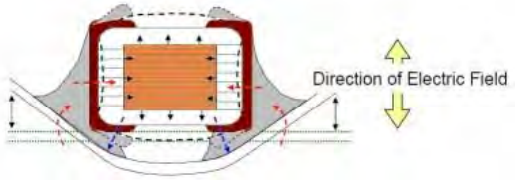
REV: May 2015

Piezoelectric effect in MLCCs (Multilayer Ceramic Chip Capacitors)

MLCCs (Multi Layer Ceramic Capacitor) have **several advantages**

- low Equivalent Series Resistance (ESR)
- low Equivalent Series Inductance (ESL)
- small size
- non-polarized

Oscillation Effect

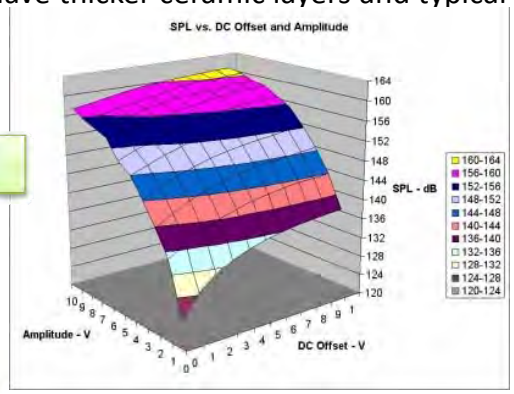


A **disadvantage** of the MLCC can be the **piezoelectric nature** of the ceramic material. MLCCs are made from ceramic dielectrics (*which have ferroelectric properties*), which can exhibit problematic or disruptive noise (*ringing or singing*) due to oscillations with PCB.

Contributors to Ringing – Singing Noise in circuits using MLCCs:

- Operating frequency of signal *(or harmonics)* within the audible range *(20Hz ~ 20KHz)*
- Operating voltage … higher signal voltage produces higher SPL (sound pressure level)
- Ceramic dielectric constant (K) … Higher K ceramics exhibit higher ferroelectric properties
- Ceramic layer thickness ... Higher voltage rated MLCVC have thicker ceramic layers and typical exhibit lower SPL

Voltage vs. SPL

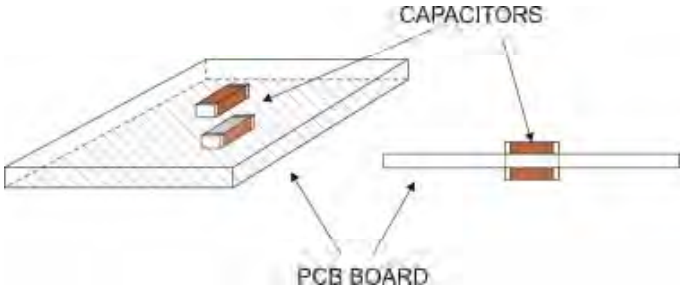


Images from EE Times - April 2012
"*Reducing MLCCs' piezoelectric effects and audible noise*"
by Nicolas Guibourg ,Texas Instruments Germany

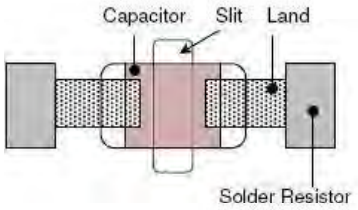
Contributors to Ringing – Singing Noise in circuits using MLCCs:

PCB = Printed Circuit Board

- PCB material and thickness … The thicker the PCB, more resistant it is to deformation and the lower SPL it produces
- PCB layout
  - MLCC capacitor placed at the edge of the PCB will be preferred (lower SPL) to placement away from edge of PCB.
  - Placed next to each other, MLCC capacitors generate higher overall SPL (+14 dB between a single capacitor and three placed in parallel).
  - On the contrary, when placed symmetrically on each side (opposite sides) of the PCB board *as shown in below figure*, MLCC capacitors tend to cancel out each other's vibrations.



Oscillation effects reduced when mounting MLCCs symmetrically opposite one another



Slit in PCB added under MLCC can help to reduce coupling to PCB and reduce SPL

Image from EE Times - April 2012
"*Reducing MLCCs' piezoelectric effects and audible noise*"
by Nicolas Guibourg ,Texas Instruments Germany

Potential Remedies

Goal: Reduce SPL to acceptable levels

X7R
X5R
Y5V → **NPO**

- Use **MLCC with lower dielectric constant** (K)
- Replace high K dielectrics Y5V / X5R / X7R **with NPO dielectric** (low K)
- Below table shows maximum capacitance values for 50V, 100V and 250V rating in **NPO dielectric** MLCCs

(*3-digit capacitance code & corresponding capacitance value*) for 0402 case size to 2225 case size

	0402	0603	0805	1206	1210	1808	1812	2220	2225
50V	471 (470pF)	332 (3300pF)	153 (0.015uF)	223 (0.022uF)	223 (0.022uF)	473 (0.047uF)	104 (0.10uF)	224 (0.22uF)	224 (0.22uF)
100V		102 (1000pF)	103 (0.01uF)	223 (0.022uF)	223 (0.022uF)	333 (0.033uF)	823 (0.082uF)	104 (0.10uF)	104 (0.10uF)
250V		471 (470pF)	392 (3900pF)	103 (0.01uF)	103 (0.01uF)	223 (0.022uF)	473 (0.047uF)	823 (0.082uF)	823 (0.082uF)

PART NUMBER SYSTEM

NMC 0805 NPO 101 J 50 TRP or TRPLP 3K F

- F — RoHS Compliant
- 3K — Optional Reel Qty (3K=3,000pcs)
- TRPLP — Tape & Reel (Embossed Plastic Carrier)
- TRP — Tape & Reel (Punched carrier)
- 50 — Voltage (Vdc)
- J — Capacitance Tolerance Code (see chart)
- 101 — Capacitance Code, expressed in pF, first 2 digits are significant, 3rd digit is no. of zeros, "R" indicates decimal for under 10pF
- NPO — Temperature Characteristic
- 0805 — Size Code (see chart)
- NMC — Series

*Added benefit of using **NPO** is far greater **stability over voltage, temperature and time** as compared to X7R / X5R / Y5V dielectric*

NSPH Series - SMT Film Chip Capacitors

NSPH - High Capacitance SMT Film Chip Capacitors

NSPH series, High Capacitance SMT Film Chip Capacitors

NIC Components is pleased to announce the addition of NSPH series of High Capacitance Multilayer Polymer Film SMT Chip Capacitors. Supplied in four EIA surface mount cases sizes; 1206, 1210, 1812 & 2220 in capacitance values from 0.1uF to 22uF with voltage ratings from 16V ~ 63VDC (11V ~ 45Vrms). NSPH series is rated for operating temperatures of -55°C to +125°C with typical capacitance change within ±5% of 25°C capacitance value.

NSPH series is RoHS compliant and is halogen free. Supplied tape and reel packaged, for high speed automated placement and compatible with high temperature Pb-Free alloy soldering (+260degC soldering heat rated). NSPH unit pricing range from $0.39 ~ $1.09 with production lead times of 8 to 10 weeks. Please contact NIC today for Free component samples and to review your requirements.

Features:

- High Capacitance in Small Case Sizes
- Stable Cap Value over Voltage, Temperature & Time
- Low Noise for Digital Audio Streamer applications
- **Reduce or eliminate MLCC Piezoelectric Effects**
  - ***Capacitor singing or ringing effects***
- Low Dielectric Absorption for use in A to D applications (*10X ~ 20X improvement over X7R MLCCs*)
- Self healing construction (open mode failure)
  - *Free of component cracking failures (MLCC weakness)*
- High IR; low leakage current performance (compared to high cap X5R MLCCs)
- Replace large leaded film capacitors with small low profile (low ESL) SMT chip
- RoHS compliant and Halogen Free

SMT Film Capacitors; **Series** & Case Sizes

NSPH series
High Capacitance SMT Film Chip Capacitors

- **High Capacitance**
- **Reduced Case Sizes**
- **High Voltage @ >1uF**

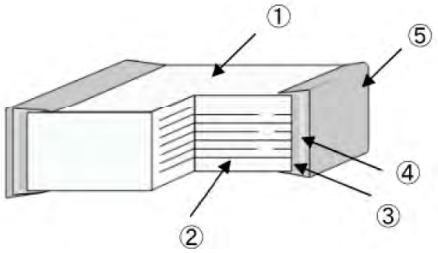
Voltage Rating (VDC)	< 0.01uF	0.01uF	0.022uF	0.047uF	0.1uF	0.15uF	0.22uF	0.33uF	0.47uF	0.68uF	1.0uF	1.5uF	2.2uF	3.3uF	4.7uF	6.8uF	10uF	15uF	22uF
250V	NSWC 1913~2420	NSWC 2420																	
100V	NSWC 1206~1210	NSWC 1210	NSWC 1913	NSWC 1913	NSWC 2416	NSWC 2416	NSWC 2820												
	NSHC 1913~2820	NSHC 2820	NSHC 2825																
		NSMX 2218	NSMX 3021	NSMX 3022	NSMX 3024	NSMX 3026	NSMX 4028	NSWC 2820	NSWC 3022	NSWC 3925	NSWC 3925								
63V							NSPH 1206	NSPH 1210	NSPH 1210	NSPH 1812	NSPH 1812	NSPH 1812	NSPH 2220	NSPH 2220					
50V	NSHC 0805~1913	NSHC 1913	NSHC 2416		NSPH 1206		NSPH 1206	NSPH 1206	NSPH 1210	NSPH 1210	NSPH 1812	NSPH 1812	NSPH 1812	NSPH 2220	NSPH 2220				
35V									NSPH 1206	NSPH 1206	NSPH 1210	NSPH 1210	NSPH 1812	NSPH 1812	NSPH 1812	NSPH 2220	NSPH 2220		
25V										NSPH 1206	NSPH 1206	NSPH 1210	NSPH 1210	NSPH 1812	NSPH 1812	NSPH 1812	NSPH 2220	NSPH 2220	
16V					NSPU 0805	NSPU 1206	NSPU 1206	NSPU 1206	NSPU 1206	NSPU 1206	NSPH 1206	NSPH 1206	NSPH 1210	NSPH 1210	NSPH 1812	NSPH 1812	NSPH 1812	NSPH 2220	NSPH 2220
	NSHC 0603~1210	NSHC 1210									NSPU 1210								
6.3V																			

Capacitance Value

NSPH - High Capacitance SMT Film Chip Capacitors

CONSTRUCTION

	Part	Materials
1	Capacitor Element	Acrylic base polymer film
2	Internal Electrode	Vapor deposited aluminum
3	First Termination Layer	Copper alloy
4	Second Termination Layer	Conductive paste
5	Third Termination Layer	100% Sn (tin) plating



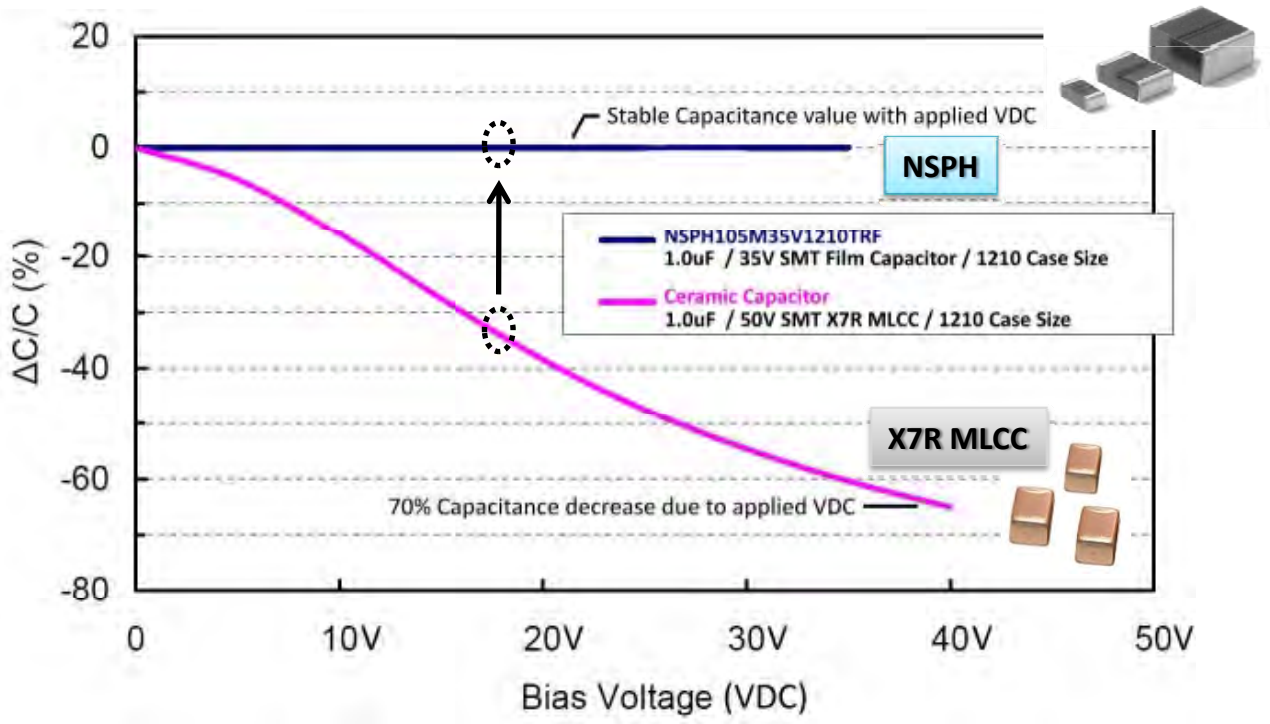
NSPH is ideal for use in green power, network infrastructure, instrumentation, high-end audio, digital audio streaming equipment and audio DAC applications.

NSPH series **have many advantages over high capacitance MLCCs (X5R& X7R) capacitors**:

- ✓ Higher voltage ratings (15uF & 22uF)
- ✓ **Stability over voltage, temperature** and **time**
- ✓ The low loss film construction is **free from piezoelectric noise** (MLCC distortion)
- ✓ Free from MLCC cracking failures
- ✓ Superior **low leakage current characteristics** for green power applications (high efficiency)
- ✓ **Low dielectric absorption** characteristics, *10X ~ 20X improvement over X7R MLCCs*
- ✓ **Open-mode failure** advantage of NSPH series, compared to short-circuit failure mode of MLCC capacitors.

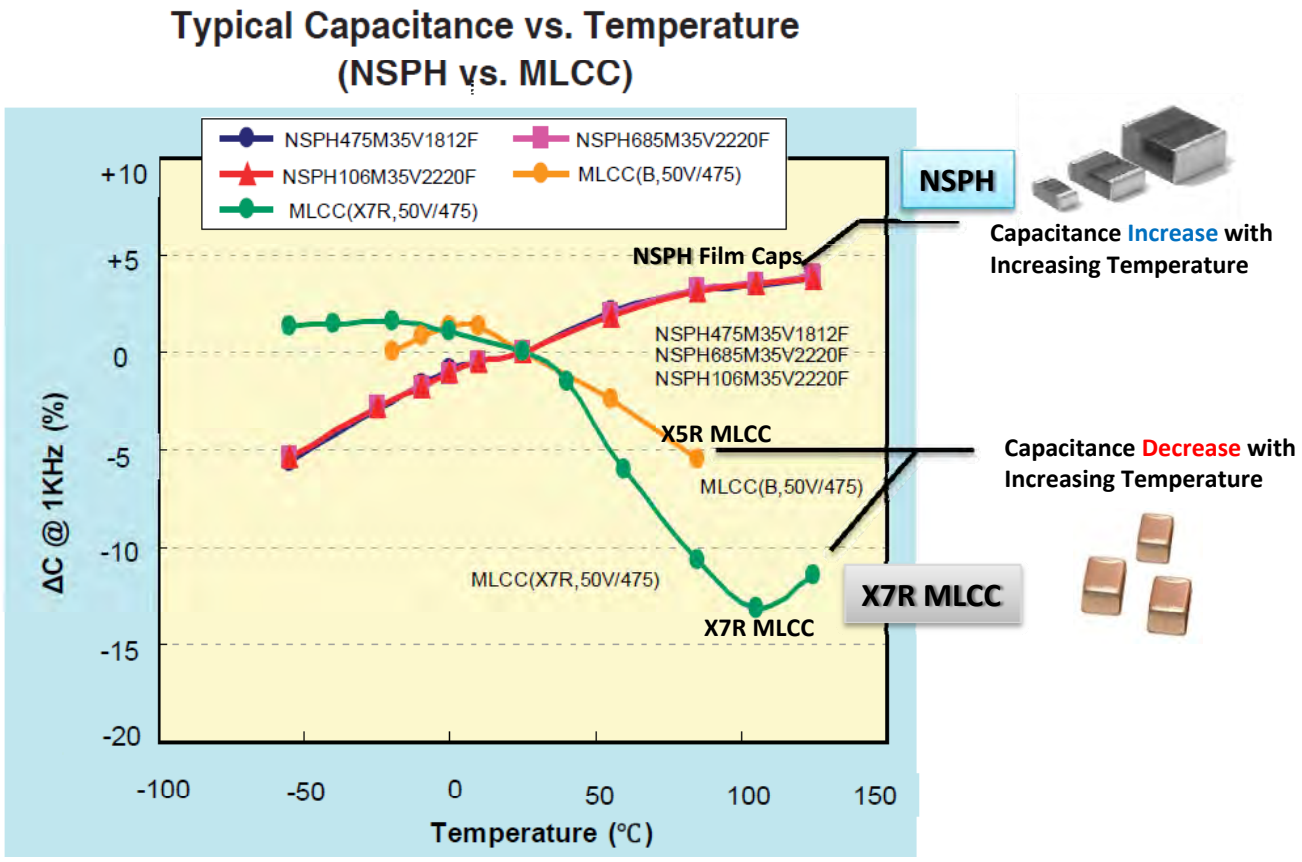
NSPH - High Capacitance SMT Film Chip Capacitors

NSPH stability advantage over high capacitance MLCCs capacitors



NSPH - High Capacitance SMT Film Chip Capacitors

NSPH advantage over high capacitance MLCCs capacitors



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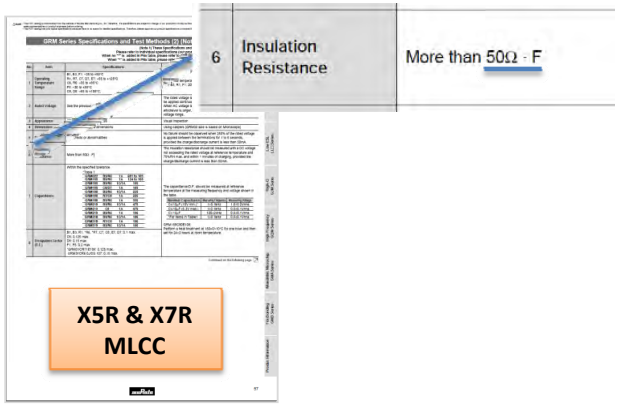
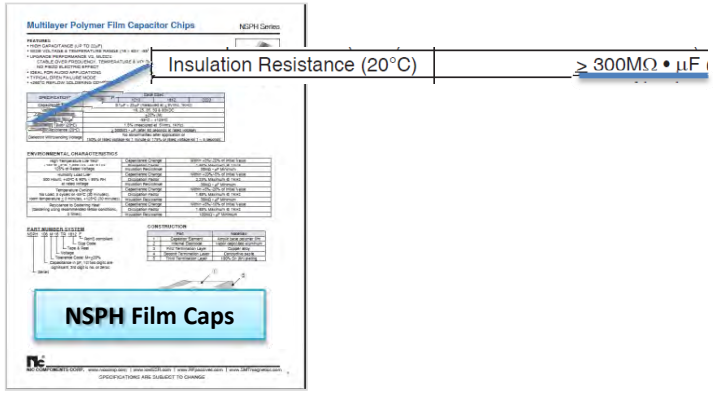
NSPH - High Capacitance SMT Film Chip Capacitors

NSPH lower leakage current advantage compared to high capacitance MLCCs capacitors

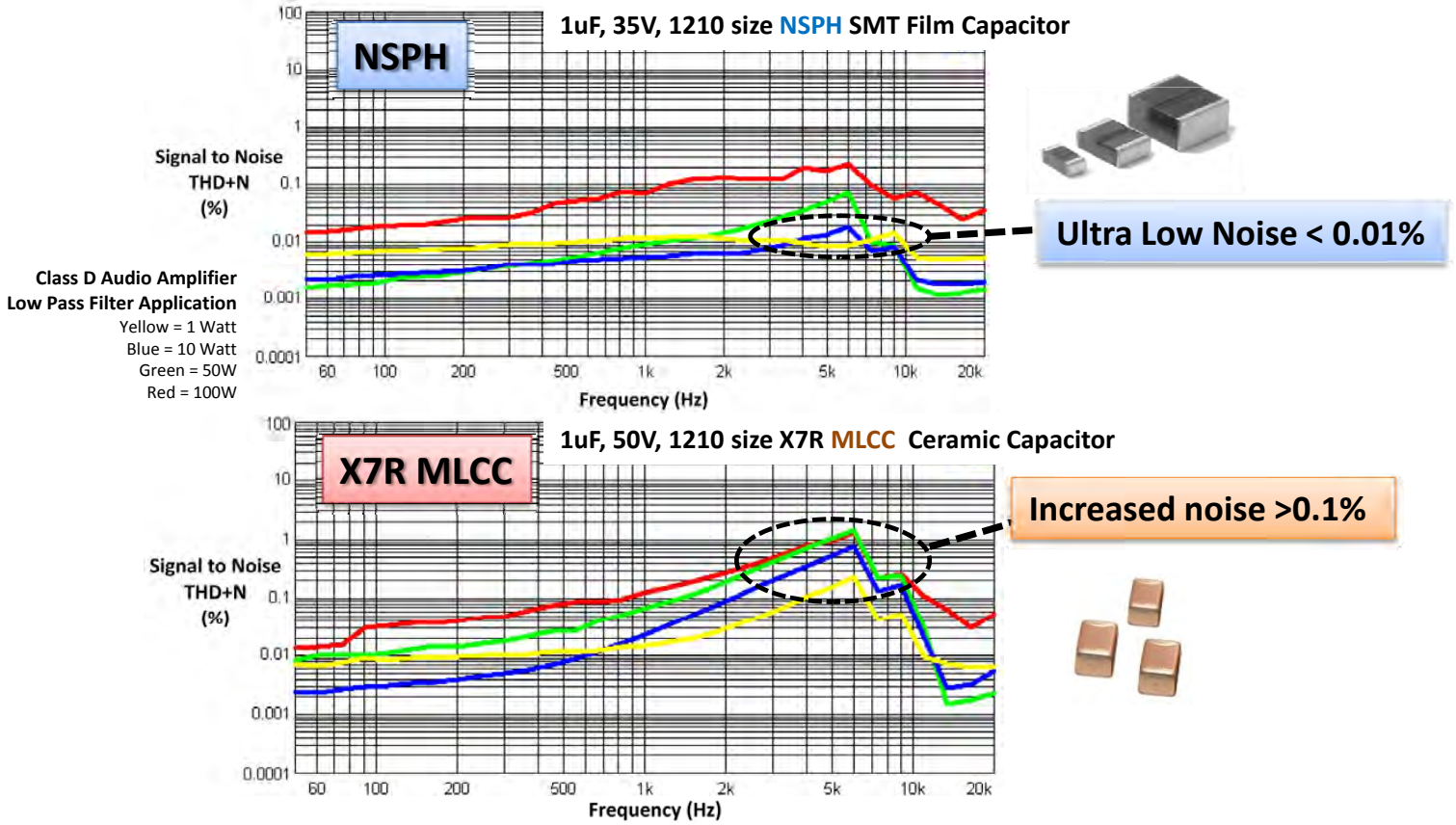
	Type	IR Insulation Resistance	22uF Capacitor Leakage Current @ 5VDC Operation	*Using 4 Capacitors* Energy Loss due to Capacitor LC
NSPH	NSPH Film Cap	> 300MΩ • µF	0.37 uA	up to **1.5 uA** ← **6 X Improvement**
X7R MLCC	MLCC X5R & X7R	" > 50Ω • F " > 50MΩ • µF	2.2uA	up to **8.8uA**





NSPH - High Capacitance SMT Film Chip Capacitors

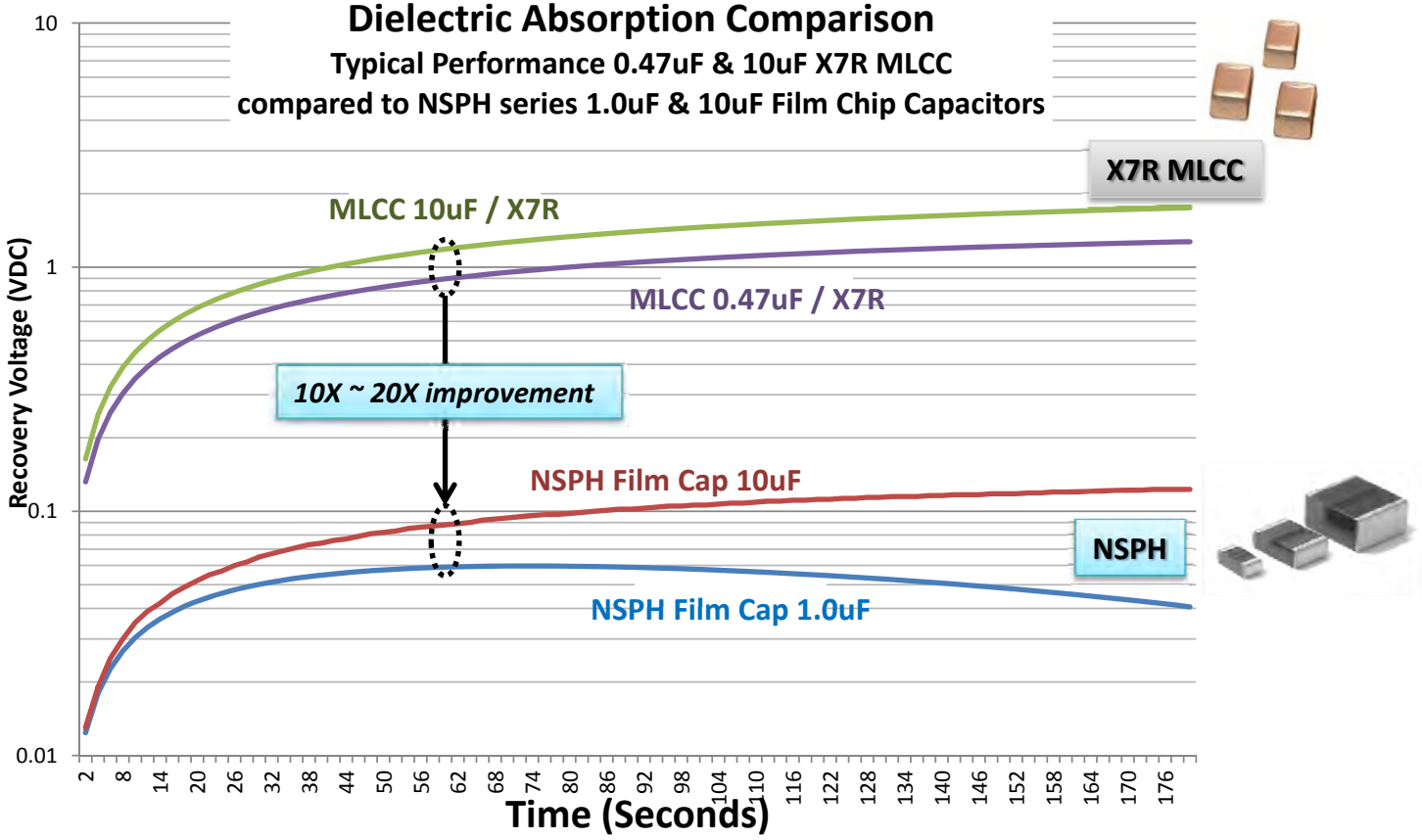
NSPH lower distortion advantages over high capacitance MLCCs capacitors



THD+N is a sum of harmonic distortion components and noise

NSPH - High Capacitance SMT Film Chip Capacitors

NSPH lower dielectric absorption advantages over high capacitance MLCCs capacitors



SMT Ceramic MLCC Capacitors; **TCs** & Case Sizes

NSPH series
High Capacitance SMT Film Chip Capacitors

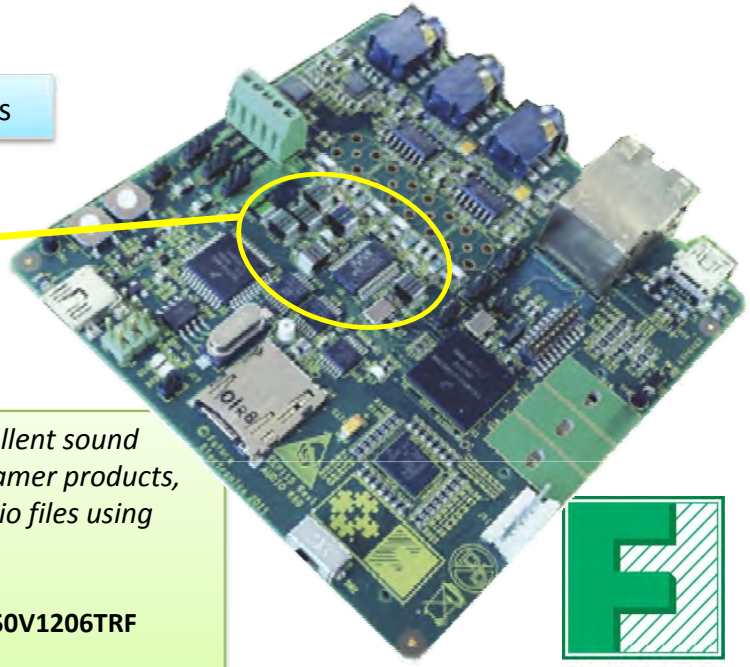
Please review to assure NSPH meets **circuit voltage** and **current requirements** of circuit

Voltage Rating (VDC)											
100V	X7R 1210, 1812, 1825, 2220, 2225	X7R 1210, 1812, 1825, 2220, 2225	X7R 1210, 1812, 2220, 2225	X7R 2220 & 2225	X7R 2220 & 2225						
50V	X7R 0805, 1206, 1210 1812, 1825, 2220	X7R 1210, 1812, 1825, 2220	X7R 1210, 1812, 1825, 2220	X7R 1812, 1825, 2220	X7R 1812, 1825, 2220	X7R 2220	X7R 2220				
35V				NSPH 1812	X7R 1210		NSPH 2220	← Advantage NSPH			
			X5R 1210	↑ Advantage NSPH		↓ Advantage NSPH	X5R 1210				
25V	X7R 0805, 1206, 1210 1812, 2225	X7R 2225	X7R 1206, 1210, 2225	X7R 1206 & 1210	X7R 1206	NSPH 2220	X7R 1210 & 1812	↓ Advantage NSPH			
	X5R 0603 & 0805		X5R 0805 & 1206	X5R 1206	X5R 1206 & 1210	NSPH 1812	X5R 1206 & 1210	NSPH 2220	↓ Advantage NSPH		
16V	X7R 0603, 0805, 1206 1210, 1812			X7R 1206	X7R 0805, 1206, 1210	↓ Advantage NSPH	X7R 1206 & 1210	NSPH 2220	NSPH 2220		
	X5R 0402, 0603, 0805	X5R 1206	X5R 0603, 0805, 1206	X5R 1206	X5R 0805, 1206, 1210	NSPH 1812	X5R 0805, 1206, 1210		X5R 1206 & 1210		
10V	X7R 0603, 0805, 1206 1210, 1812			X7R 1206	X7R 0805, 1206, 1210		X7R 1206 & 1210				
	X5R 0402, 0603, 0805		X5R 0402, 0603, 0805, 1206	X5R 0805 & 1206	X5R 0603,0805 , 1206, 1210		X5R 0805, 1206, 1210		X5R 1206 & 1210		
6.3V				X7R 0805	X7R 0805		X7R 1206				
	X5R 0402, 0603, 0805		X5R 0402	X5R 0603, 0805, 1206	X5R 0402, 0603,0805 , 1206, 1210	X5R 1206	X5R 0805, 1206, 1210		X5R 0603, 0805, 1206	X5R 1206 & 1210	X5R 1210
4V							X5R 0603			X5R 1206	
	1.0uF	1.5uF	2.2uF	3.3uF	4.7uF	6.8uF	10uF	15uF	22uF	47uF	100uF
	Capacitance Value										

➔ Specification Sheet: www.niccomp.com/catalog/nsph.pdf

NSPH - High Capacitance SMT Film Chip Capacitors

Small SMT Film Capacitors
NSPH series



NSPH series, SMT Film capacitors contribute to *"excellent sound reproduction and very low distortion" … in Audio Streamer products, decoding FLAC, WAV, MP3 and Ogg Vorbis digital audio files using ARM Cortex-M4 embedded processor*

100nF (0.1uF) /1206 / NSPH/20% /50V = PN: **NSPH104M50V1206TRF**

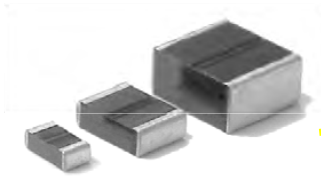
10uF/1812/NSPH/20%/16V = PN: **NSPH106M16V1812TRF**

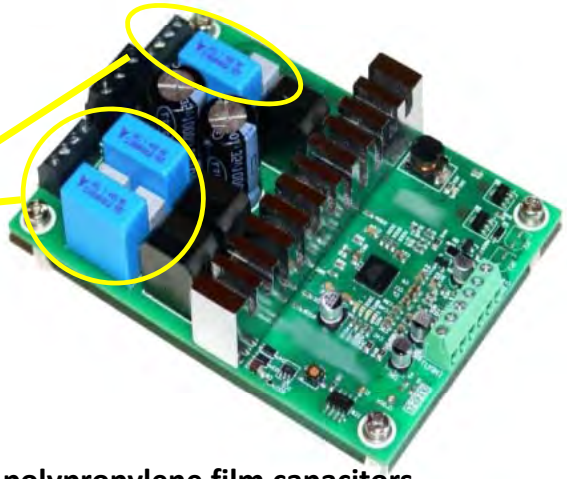
FUTURE ELECTRONICS

Applications:

- *High-End Audio*
- *Digital audio streaming and audio DAC applications*
- *Battery Powered: Handheld & Portable Devices*
- *Green Power*
- *Test & Instrumentation*
- *Network Infrastructure*

NSPH - High Capacitance SMT Film Chip Capacitors





Circuit Redesign & Downsize

Small SMT type **NSPH** series can replace **large leaded polypropylene film capacitors**

* Please review to assure NSPH meets circuit voltage and current requirements of circuit

EIA surface mount cases sizes

- 1206 (3.2mm x 1.6mm x 1.6mm)
- 1210 (3.2mm x 2.5mm x 2.2mm)
- 1812 (4.5mm x 3.2mm x 2.8mm)
- 2220 (5.7mm x 5.0mm x 2.8mm)

Downsize from large radial leaded film capacitor in **18mmx 18mm x 9mm size** to small SMT film capacitor in **5.7mm x 5.0mm x 2.8mm size**

Capacitance = 10µF
Voltage Rating AC = 40V (63VDC)
Dielectric Material = Polyester
Package / Case = Radial Box Type
Size / Dimension L x W **= 18.0mm x 9.0mm**
Height (Max) H = **17.5mm**
Lead Spacing LS = **15.00mm**

Additional Information Needed?

Need Samples?

Technical Support: tpmg@niccompcom

Sales Support: sales@niccomp.com

- European Engineering Support
- North America Engineering Support
- SE Asia Engineering Support

NIC Components offers **unique performance passive components** that provide advantages to design engineers to create high performance end products in smaller and lower total cost formats

- Surface Mount SMT formats (*high speed auto placement*)
- Pb-Free Reflow Compatible (*high temperature reflow*)
- Performance advantages over competing technologies

NIC Components Corp.

Exhibit E

KEMET Electronics Corp

PIEZOELECTRIC EFFECTS CERAMIC CHIP CAPACITORS (Singing Capacitors)

Most dielectrics of ceramic capacitors exhibit a characteristic identified as piezoelectric effects than can cause unexpected signals in certain circuits. In some cases, the piezoelectric effect may result in the appearance of electrical noise, while in other cases; an acoustic sound may be heard, emanating from the capacitor itself.

The basic element in most MLCCs is barium-titanate, or some close derivative of this. Piezoelectric properties are common to the barium-titanate structure. If you are old enough to recall before CDs, acoustic recordings were mostly sold on vinyl records and the signals were picked up using a needle that was contained in a spiraling groove cut in the record's surface. Within these grooves, the needle would ride on roughened surfaces that created mechanical vibrations of the needle. The needle was connected to a crystal structure (in less expensive turntables), and this crystal would generate an electrical signal that correlated with the vibration's frequency and magnitude, which was then amplified to generate the speaker signals. What was the crystal structure of these ceramic cartridges? They were based on barium-titanate!

Piezoelectric effects can result in noise for ferroelectric ceramic chips, such as those of the middle to high dielectric constants like X5R, X7R, X8R, Y5V, Y5U, Z5U, etc. Piezoelectricity occurs in all ferroelectric dielectrics, regardless of manufacturer, and the means to reduce these effects usually requires the dielectric constant be lowered (the capacitance capability is also lowered with the lower dielectric constant) while moving to higher dielectrics (Y5V, Z5V are usually cheaper) creates a higher susceptibility to this effect. Note that there are no measurable piezoelectric effects in Class 1 capacitors, such as C0G or NP0 - neither of which is considered ferroelectric.

Historically, the piezoelectric noise has been only an occasional issue, since it was at such a low level. It can occur as a mechanically induced electrical noise or it can occur as an electrically induced mechanical noise (this is what a speaker or buzzer does). If a capacitor is surface-mounted on a PCB, there is a direct mechanical connection between the board and the capacitor. Vibrations created on the board can create electrical signals within the capacitor. Electrical signals in the capacitor can create mechanical vibrations of the board. Multiple chips located in a specific area can flex the board, creating a larger speaker area.

These created signals can be problematic enough, but the translation from electrical to mechanical, then mechanical back to electrical both involve delays and can create a slight echo or distortion effect in the circuit. The peak response of these capacitors is within and slightly above the audio frequency range. Many attempts to use these SMT devices in final stages of audio amplifiers have left many designers scrambling for alternatives, yet they can be used in the front-end stages because the signal levels are lower.

More recently, power integrity circuits involved with microprocessor decoupling have been experiencing this effect in ceramic capacitors. The microprocessor 'sleep' mode involves removing the voltage from the power rails on an intermittent basis, and periodically checking for any request for activity. The typical frequency for this sleep mode is at 1 kHz, and designers are experiencing a 1 kHz tone emanating from the processor region of the computer when the processor goes into its sleep mode.

This problem is becoming more noticeable because the MLC capacitors are evolving and their applications are expanding. This effect is related to the signal strength, which is related to the electrical stress within the capacitor. As the dielectrics are shrinking to enable higher capacitance with these packages, the critical stress levels are being reached at lower voltage levels.

Solutions to these noise problems may involve alternative types of capacitors (e.g., tantalum, aluminum, ta-polymer, al-polymer, film, as this effect is unique to ceramic), leaded or standoff capacitors (using leadframes to eliminate the mechanical tie to the PCB eliminates a unified or cumulative response of multiple ceramic capacitors), using higher voltage ratings (lowers the stress), and others. It should be pointed out that this effect is lost at frequencies well above 30 kHz because the body cannot respond fast enough to the changing stress levels. The peak response region and the noise attributes dictates that these capacitors should be used very carefully in audio circuits, as well as high-gain circuits; and, be careful that an audio application may not easily appear to be an audio circuit (sleep mode conditions of microprocessors).

John D. Prymak – KEMET Applications Manager

2006-08 Arrow Asian Times Article

Exhibit F

Actuation for Mobile Micro-Robotics

John C. Tucker
North Carolina State University

Introduction

Advances in precision micro-machining has led to an interest in micro-robotics. Applications of micro-robotics range from micro-assembly, to biomedics (inner space), to land mine sweeping, to city water system analysis. As with conventional robotics one of the biggest challenges is making robots that are mobile and can traverse a wide variety of terrain. Furthermore, in micro-robotics there is the problem that as the robot gets smaller the terrain obstacles seem bigger. A pebble is no problem for a six meter long HMV, but it is real challenge for a ten millimeter surveillance robot.

Actuation systems for mobile micro-robotics must meet the following challenges:

- Traverse terrain with obstacles bigger than robot
- Low power/ high efficiency
- Simple control
- Withstand harsh environments
- Simple mechanics for both scalability and ease of manufacturing

Obviously the actuation method must be designed to meet the needs of the robot. A robot in a desert (scorpion design) will have a different design than one in a water pipe (fish design). This paper reviews the current technologies for actuation systems and then discusses some designs for a micro-robot.

Conventional Electromagnetic Motors and Solenoids

In the past robotics has mainly used motors and solenoids to make robots mobile. This can be done simply by using motors with wheels or tracks, or by using arms and legs powered by motors and solenoids. Designs of this type benefit from the large amounts of physical motion that can be produced. Furthermore, rolling motion like a car is very efficient and traverses simple terrain very well. The use of arms and legs adds the ability to traverse steps and other obstacles. However, electromagnetic motors are mechanically complex and do not scale down very well. Manufacturing electric motors less than a millimeter in size is very challenging. Other problems are power efficient (30-40% max.) and fragility.

Piezoelectric Linear Actuators

Piezoelectric materials are materials that expand/contract when an electric field is applied to them. They also will produce an electric field across themselves if a mechanical force is applied to them. Common places for piezoelectrics are in gas lighters, high frequency speakers, and micro-positioners.

These devices rely on the piezoelectric effect. The piezoelectric effect happens in materials with an asymmetric crystal structure. When an external force is applied, the charge centers of the crystal structure separate creating electric charges on the surface of the crystal. This process is also reversible. Electric charges on the crystal will cause a mechanical deformation. Quartz, turmalin, and seignette are common natural piezoelectrics. Much work has gone into making polycrystalline ceramic piezoelectrics because physical properties can be tailored to the application. Furthermore, these materials can be bulk produced or deposited onto surfaces. Common ceramic piezoelectrics are lead-zirconate-titanate (PZT) and lead-magnesium-niobate (PMN). Piezoelectrics have also been made in polymer form, such as poly-vinylidene fluoride (PVDF).

Piezoelectrics deform linearly with applied electric field. Unfortunately, conventional materials only deform up to 0.1%. Thus, for a 5 cm leg on a micro-robot, the motion will be only 50 um. Furthermore, this happens at an electric field around 2 kV/mm. Thus, the applied voltage would have to be 100 kV. Piezoelectrics follow the equation

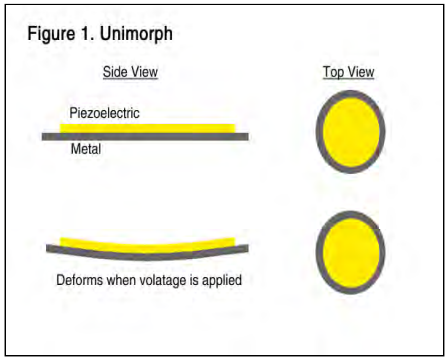
$$\Delta L = EdL_o + \frac{F}{C_T}$$

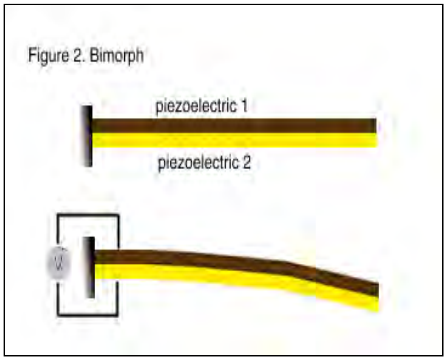
where E is the electric field, d is the piezoelectric tensor of the material, F is an externally applied force, and C_T is the stiffness of the material. Because strains are so small, piezoelectric actuators are mainly used in speakers or precision micro-positioning applications where small, precise motion is needed. However, deflection amplification methods make piezoelectrics possible actuators in micro-robotics.

Bending Mode Mechanical Amplifiers

Unimorph

One amplification method is the unimorph design shown in figure 1. When a voltage is applied across the ceramic and metal plate the unimorph bends. Reversing the voltage bends it in the other direction. This device relies on the d_{31} piezoelectric factor. This is the change in strain induced perpendicular to the electric field. The factor d_{31} is typically half of d_{33}, the induced normal to the electric field. However, a motion of 0.875 inches can be produced by a unimorph approximately one inch in diameter and 0.02 inch thick. This design is typically found in loud speakers.





Bimorph

Like the unimorph, the bimorph uses d31 piezoelectric actuation. The bimorph uses two piezoelectric plates that amplify the deflection as shown in figure 2. The two plates can be electrically connected in parallel or in series. A parallel connection produces twice the displacement as a series connection. In either case the strain is proportional to the square of the applied voltage.

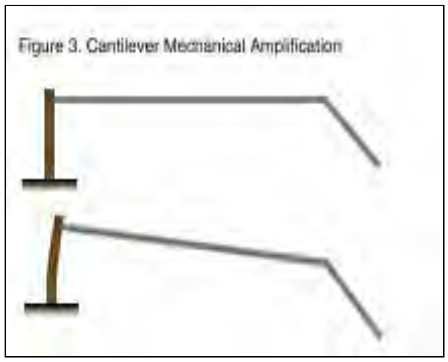
RAINBOW

RAINBOWs or **R**educed **A**nd **I**nternally **B**iased **Ox**ide **W**afers are piezoelectric wafers with an additional heat treatment step to increase their mechanical displacements. In the RAINBOW process, developed by Gene Heartling at Clemson University, typical PZT wafers are lapped, placed a on graphite block, and heated in a furnace at 975 C for 1 hour.[8] The heating process causes one side of the wafer to become chemically reduced. This reduced layer, approximately 1/3 of the wafer thickness, causes the wafer to have internal strains that shape the once flat wafer into a dome. The internal strains cause the material to have higher displacements and higher mechanical strength than a typical PZT wafer. RAINBOWs with 3 mm of displacements and 10 kg point loads have been reported.[9]

Flextensional Amplifiers

Stacks

Similar to the bimorph is the piezoelectric stack where several elements are placed on top of each other and electrically connected in parallel. The advantage of this design is that a stack uses the d33 which is larger than the d31 effect. Furthermore, displacements are N (number of elements in stack) greater for the same applied voltage.

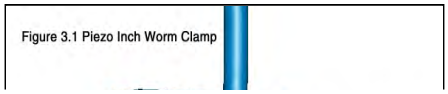


Cantilevers

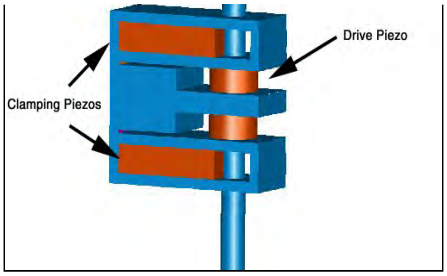
Other ways of producing mechanical amplification are through the use of cantilevers in figure 3. This is just a simple mechanical amplifier that increases displacement but reduces force.

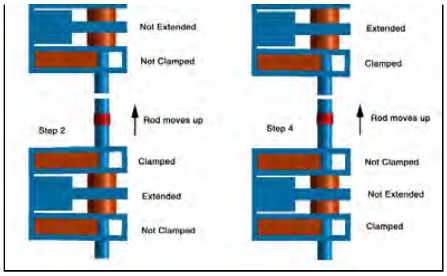
Inch Worm Motors

Piezoceramic inch worm motors are



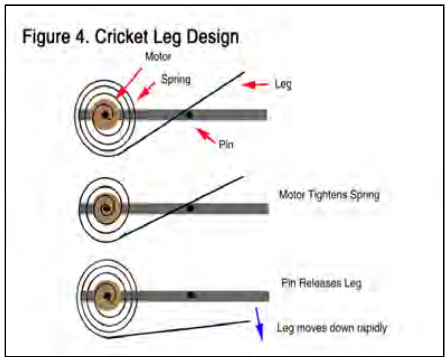
linear motors generally used in micro-positioning applications due to the ability to make very small accurate motions. The concept is shown in figures 3.1 and 3.2. There are two clamps and one extentional element. While clamp A is on and clamp B is off the drive piezo is extended. Then, clamp A is off and B is on returning clamp B to its original position by relaxing the drive piezo. Again, clamp A is on and clamp B is off the drive piezo is extended and so on. This is done many times and the rod moves up. Reversing the clamping sequence can make the rod move down. These devices can be operated at high frequencies to achieve millimeter per second motions. Some challenges of inch worm devices are achieving high precision in manufacturing so that the clamps work properly.





Piezoelectric Rotary Motors

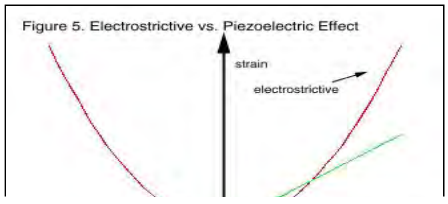
Piezoelectric rotary motors have been developed that not only weigh much less than conventional electromagnetic motors but also supply much higher stall torque. Timothy S. Glenn and Nesbit W. Hagood at MIT have developed an 330 gram ultrasonic piezoelectric motor that can supply 170 N-cm. of torque[1]. A 8 mm, 0.26 gram motor has also been developed that can provide 0.054 N-cm of torque[2]. Piezoelectric rotary motors are also available commercially from Shinsei and Canon. Like other piezoelectric devices, these motors require a high voltage supply (~150 V).



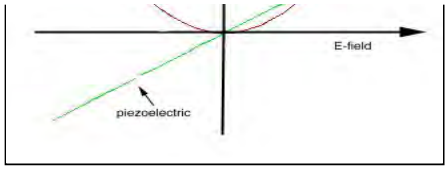
One possible actuator design with a piezoelectric rotary motor is shown in figure 4. The motor winds a spring up. The other end of the spring is held by a pin. When the pin is pulled back the leg moves down quickly and produces a "cricket" jumping motion.

Relaxor-ferroelectrics

Relaxor-ferroelectrics are similar to piezoelectrics except the strain is produced by the second order electrostrictive effect as opposed to the first order effect. The advantages of these actuators over conventional piezoelectrics include improved stroke (quadratic relationship to applied electric field shown in figure 5), low hysterisis, return to zero



displacement when voltage is suddenly removed, and insusceptibility to stress depoling[3]. However, they have a higher temperature dependence of 65% change in expansion 0-50 C (only 5% for piezos)[4].



All insulators are electrostrictive and produce a strain under an applied electric field. While this effect is negligible in most materials, the PMN-PT-BT relaxor-ferroelectric manufactured by Lockheed Missiles and Space Company had a 0.1% strain at 1 kV/mm.

Magnetostrictive Actuators

Like the Piezoelectric effect where the material deforms under an applied electric filed, a magnetostrictive material deforms in a magnetic field. Induced strains and maximum stresses are on the same order of magnitude as piezoelectrics. One common magnetostrictive material TERFENOL (TER (Terbium) FE (Iron) NOL Naval Ordinance Laboratory)) produces a 0.2% strain in a 100 kA/m field[5]. One major disadvantage of magnetostrictive actuators is the need for a device to produce the magnetic fields. This device is typically a coil wrapped around the material. This makes the device bulky and losses in the coils can be high.

Hybrid Actuators

Because piezoelectrics are capacitive and magnetstricters are inductive, delivering high electrical power to them individually can be inefficient and/or require matching networks. Even with with matching networks, high efficiency over a wide frequency range is difficult. However, recent work has been done using the two devices together in order to increase frequency operation[6].

Enhanced Electrostrictive Actuators

CRESCENT (CERAMBOW)
THUNDER
Caterpillar d33 unimorph

Ion Exchange Actuators

The theory behind ion-exchange-membrane-metal composites is fairly complex. Essentially the materials are made of ionizable molecules that can dissociate and attain a net charge when a electric field is applied. These actuators have a large deformation in the presence of low applied voltage.

Actuators made from these materials can deform as much as 2.5 cm under a 7 V applied voltage[7] . These actuators best work in a humid environment, but may be encapsulated.

Shape Memory Alloys

Shape memory alloys are metals that deform when electric current is passed through them. The deformation is due to thermal expansion.

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3. Craing L. Horn and Natarajan Shankar, "Modeling the Dynamic Behavior of Electrostrictive Actuators", *SPIE Conference Procedings* Vol. 3041, pp.268-280, 1997.

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8. E. Furman, G. Li, and G.H. Heartling, "Electromechanical Properties of Rainbow Devices", *Proceedings of the 9th International Meeting on Applications of Ferroelectrics*, pp.313-318, University Park, PA, 1994.

9. G. H. Haertling, "Chemically Reduced PLZT Ceramics for Ultra-High Displacement Actuators", *Ferroelectrics*, vol. 154, pp.233-247, 1990.

For more information on MEMS research at North Carolina State University visit the Electronics Research Laboratory.

Actuation for Mobile Micro-Robotics / John C. Tucker / jctucker@eos.ncsu.edu

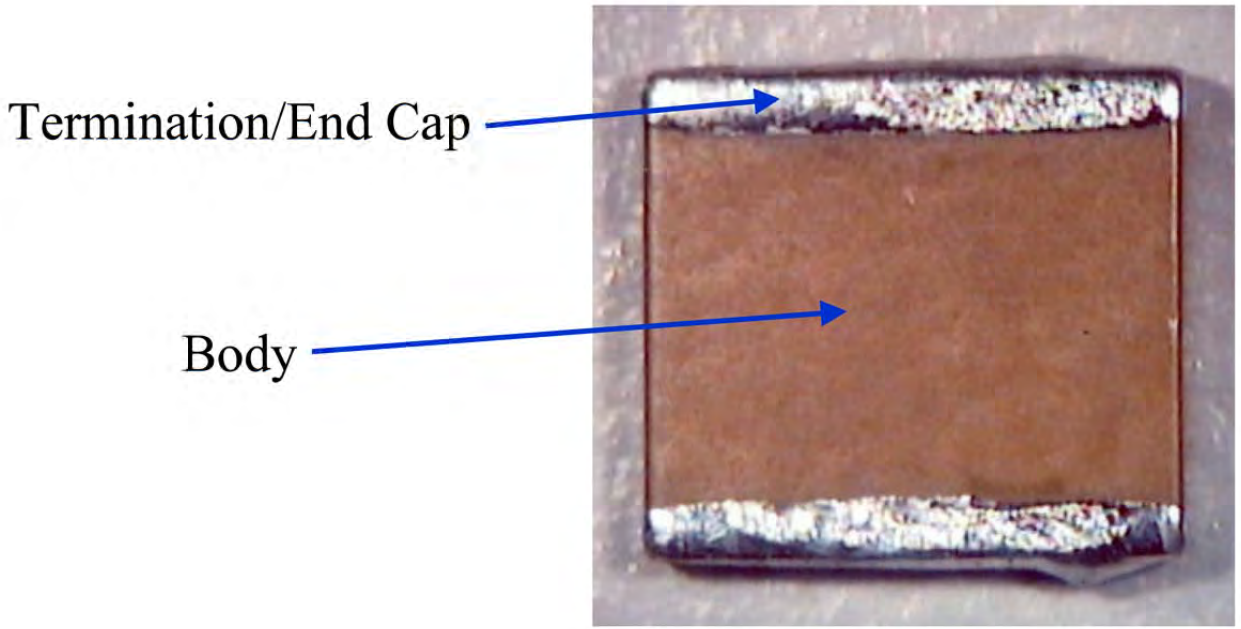
Exhibit G

Design and Process Guidelines for Use of Ceramic Chip Capacitors

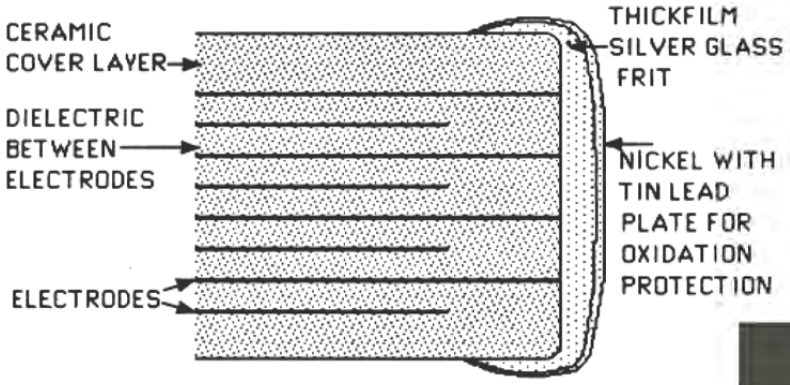
What are ceramic chip capacitors?

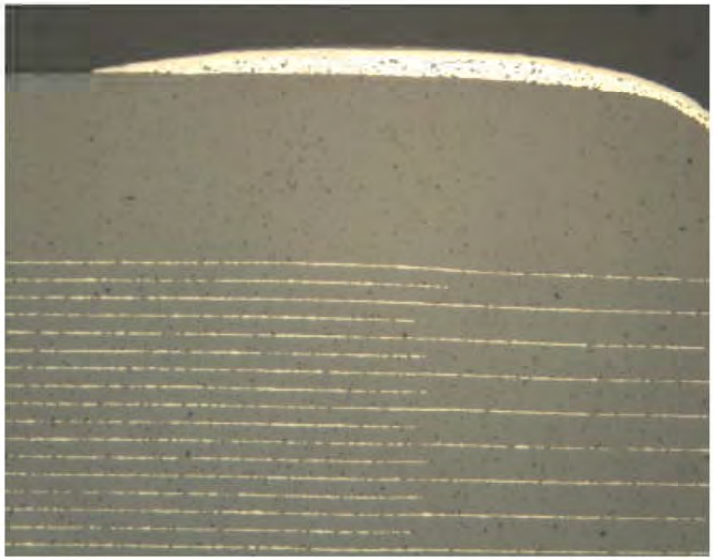
- Introduced in 1977
- Also known as multilayer ceramic capacitors (MLCC's)
- One of the most common components in the electronics industry
  - The largest manufacturers produce approximately 2 billion MLCC's per year
  - 98% yield would result in 40 million defective components
- Operating Specifications
  - 1 pF to 30 μF; 10 to 3000 volts

MLCC's



Architecture of MLCC's





- Dielectric is a proprietary alloy of barium titanate
- Electrode is often an alloy of silver or silver palladium (rarer due to cost)
- Electrode spacing can be as small as 25 μm

Manufacture of MLCC's

- Two processes
  - Dry Sheet
  - Wet Build Up
- Final steps are similar
  - Termination:
    - Silver or silver palladium alloy frit
    - Nickel barrier layer
    - Tin overplate
  - 100% Final Testing
    - Insulation Resistance, Overvoltage (2x rated voltage), Capacitance and Dissipation Factor

Dry Sheet Fabrication

- Dry Build is most common
- Green tape process
  - Mixture of dielectric powder and organic binder
- Green tape is coated with a film of silver or silver palladium alloy
- The coated tapes are then stacked, pressed and the entire structure is sintered at 1000 to 1400°C.
- The dense blocks are then cut to final dimensions and tumbled to round corners
- Primary advantage: Tight control of electrode spacing

Wet Build Up Fabrication

- Uses screen printing to lay down successive layers of dielectric (ceramic) and electrodes
- Preform is cut and then baked to provide some degree of strength
- Rounding is followed by sintering to full density
- Process is closed-loop, fully-automated
  - Allows greater control with minimal handling
- Primary advantages:
  - High density of the wet layers reduces shrinkage
  - Wet process tends to induce better interlayer bonding

Manufacture of MLCC's (cont.)

- Standard sizes
  - 0805: 0.08 in x 0.05 in x 0.05 in (varies w/capacitance)
    2.0 mm x 1.3 mm x 1.3 mm
  - 0402, 0603, 1206, 1210, 1812, 1825, and 2225 (precludes high voltage)
  - 0201 starting to be introduced
- High volume manufacturers of MLCC's
  - Kemet ($1.4 billion in annual revenue)
  - AVX ($2.6 billion)(division of Kyocera)
  - Vishay ($2.4 billion)
  - Others: Murata ($3.1 billion, Japan), KOA-Speer, Sierra-KD, Rohm ($2.7 billion, Japan), TDK ($4.2 billion, Japan), Panasonic, and Phycomp (formerly Philips)

Failure of MLCC's

- Definitions
  - Failure Mode: The effect by which the failure is observed (i.e., capacitor burns)
  - Failure Mechanism: The process(es) by which the failure mode is induced (i.e., migration of silver between adjacent electrodes)
  - Failure Site: The physical location of the failure mechanism (i.e., board side of the termination of the end cap)
  - Root Cause: The process, design and/or environmental stress that initiated the failure mechanism (i.e., excessive flexure of the board)

Definitions (cont.)

- Definitions (cont):
  - Wearout Failures: Failures due to the accumulation of damage exceeding the endurance limit of the material
  - Overstress Failures: Catastrophic failures due to a single occurrence of a stress event
  - Intrinsic Defects: Defects introduced as a result of the raw materials or the manufacturing process
  - Extrinsic Defects: Defects introduced after the manufacture of the product

Do MLCC's Wearout?

- The primary type of mechanisms that induces wearout failures in MLCC's is punch-through, which is an iterative process:
  - Areas of current leakage experience self-heating.
  - Causes deterioration of the insulation resistance
  - Leads to increase the current leakage
  - Eventually, a conductive path is formed between adjacent electrodes.
- Does not include failure of the solder interconnect, a common failure mode in large MLCC's in severe environments.
  - Large, leadless, ceramic (small CTE)

MLCC Wearout (cont.)

- Due to the widespread practice of derating (operating the capacitor at 50% rated voltage) MLCC's are not expected to experience wearout during operation.
- According to Mogilevsky and Shin (1988):

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^3 \exp\frac{E_a}{K_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)$$

where t is time, V is voltage, T is temperature (K), E_a is an activation energy (~1.3) and K_B is Boltzman's constant (8.62 x 10^{-5} eV/K)

Operating Life

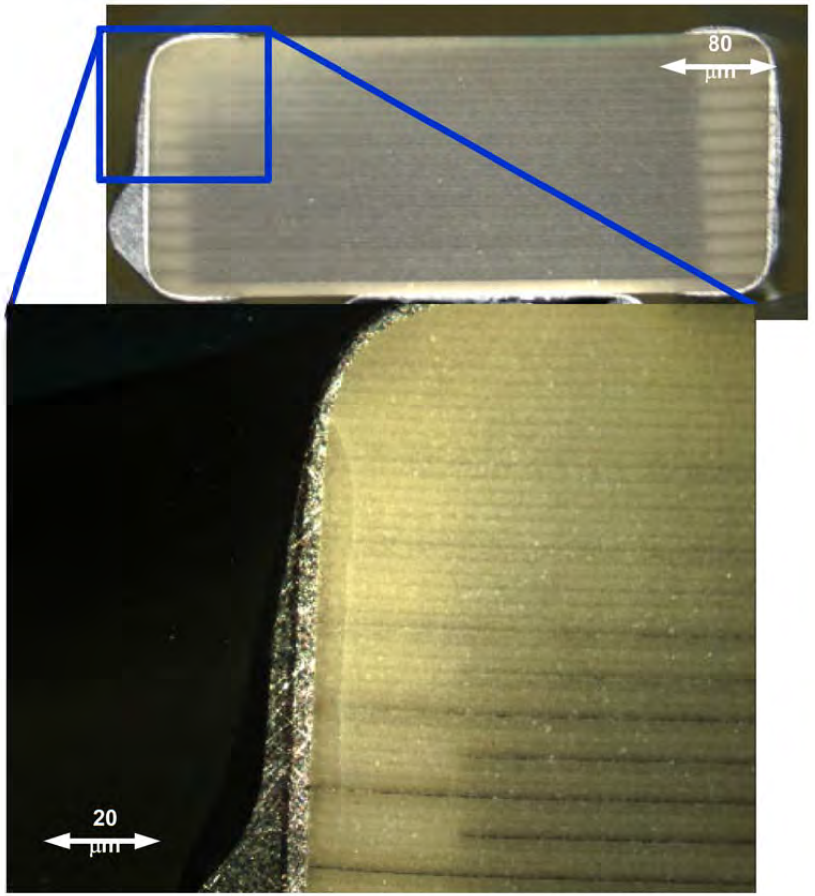
- Time to 1% failure ($t_{1\%}$) for a 50 volt MLCC is ~10 hours at 200 V and 200°C
- Equivalent to ~100 years operating at 25 volts at 25°C
- More recent work published by Kemet (Rawal, Krishnamani and Maxwell) suggest a higher activation energy (1.8 to 1.9)
  - Extends theoretical lifetime to 350 to 700 years

Intrinsic Defects

- The overwhelming percentage of MLCC's fail due to the introduction of intrinsic and extrinsic defects
- Intrinsic Defects (manufacturing)
  - Firing Cracks
  - Knitline Cracks (Delamination)
  - Voiding

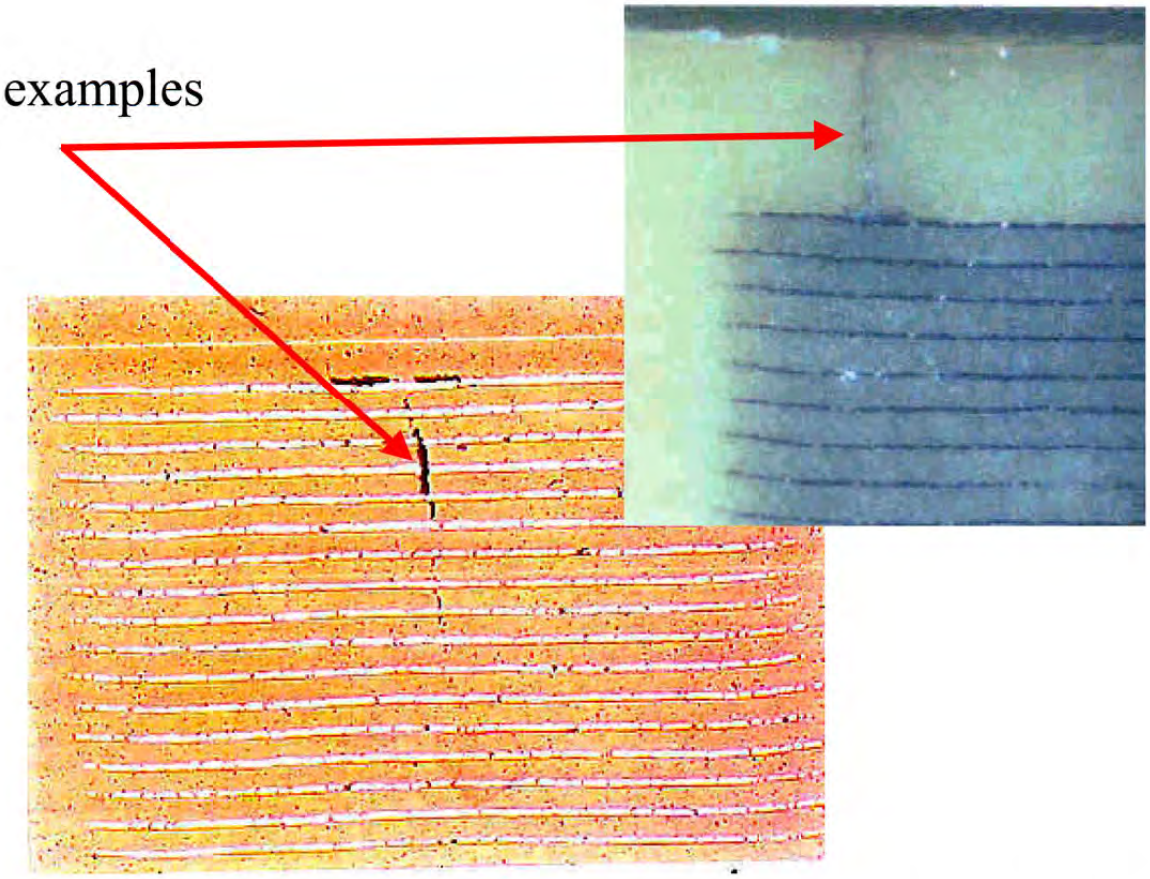
Firing Cracks

- Often originate at an electrode edge, but not always.
- Propagation path is perpendicular to the electrodes
- Root cause
  - Rapid cooling during capacitor manufacturing



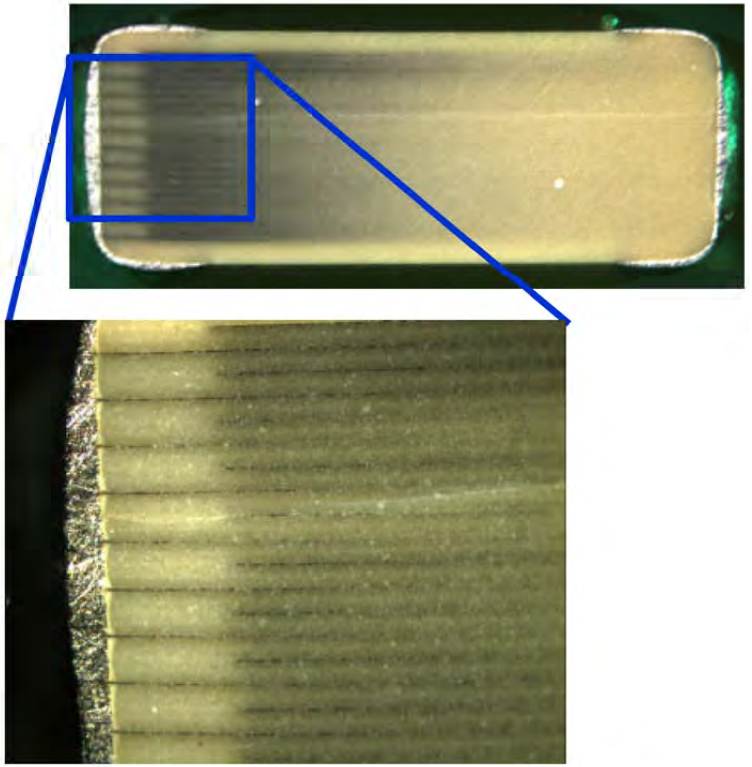
Firing Cracks (cont.)

Additional examples

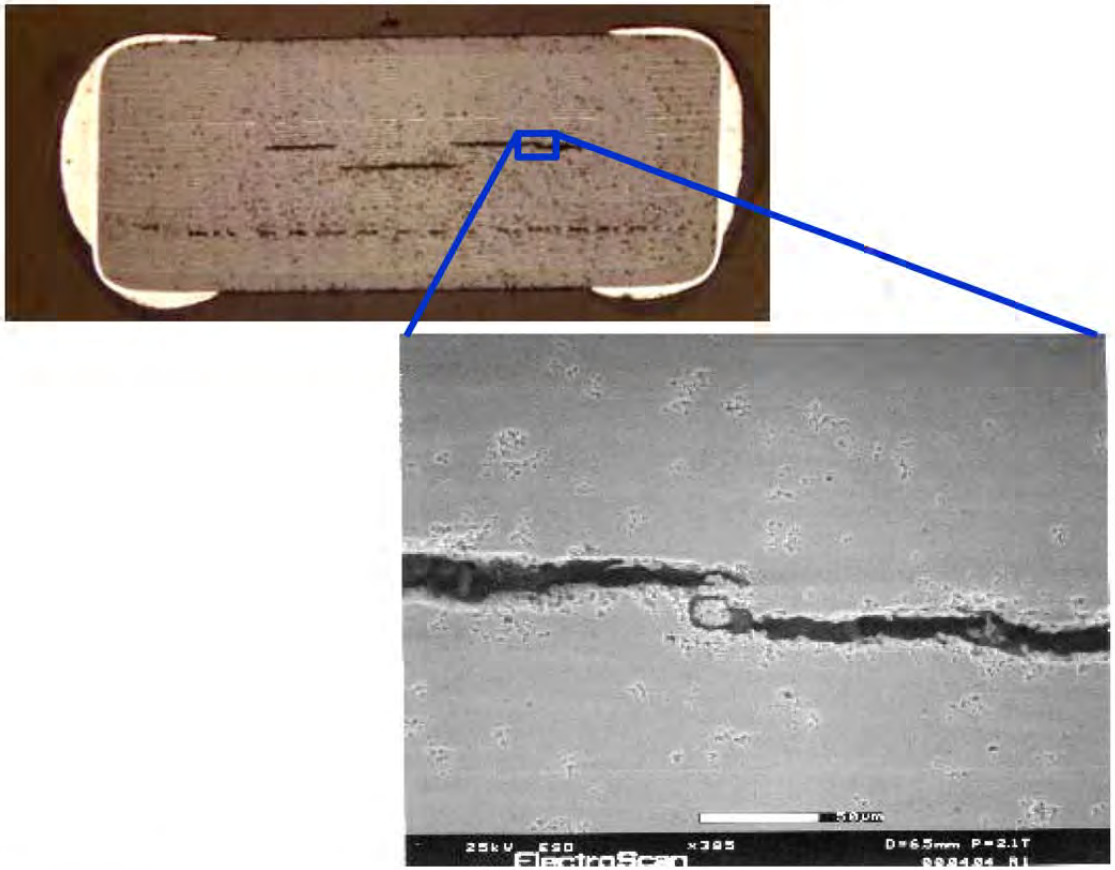


Knit Line Cracks

- Knit line cracks extend parallel to the electrodes
- Occur post-densification
  - Large crack openings
  - Jagged propagation paths
- Root causes
  - Non-optimized pressing or sintering
    - •Insufficient binding strength/Delamination
    - •Trapping of air or foreign material
    - •Internal sublimation of burnout material

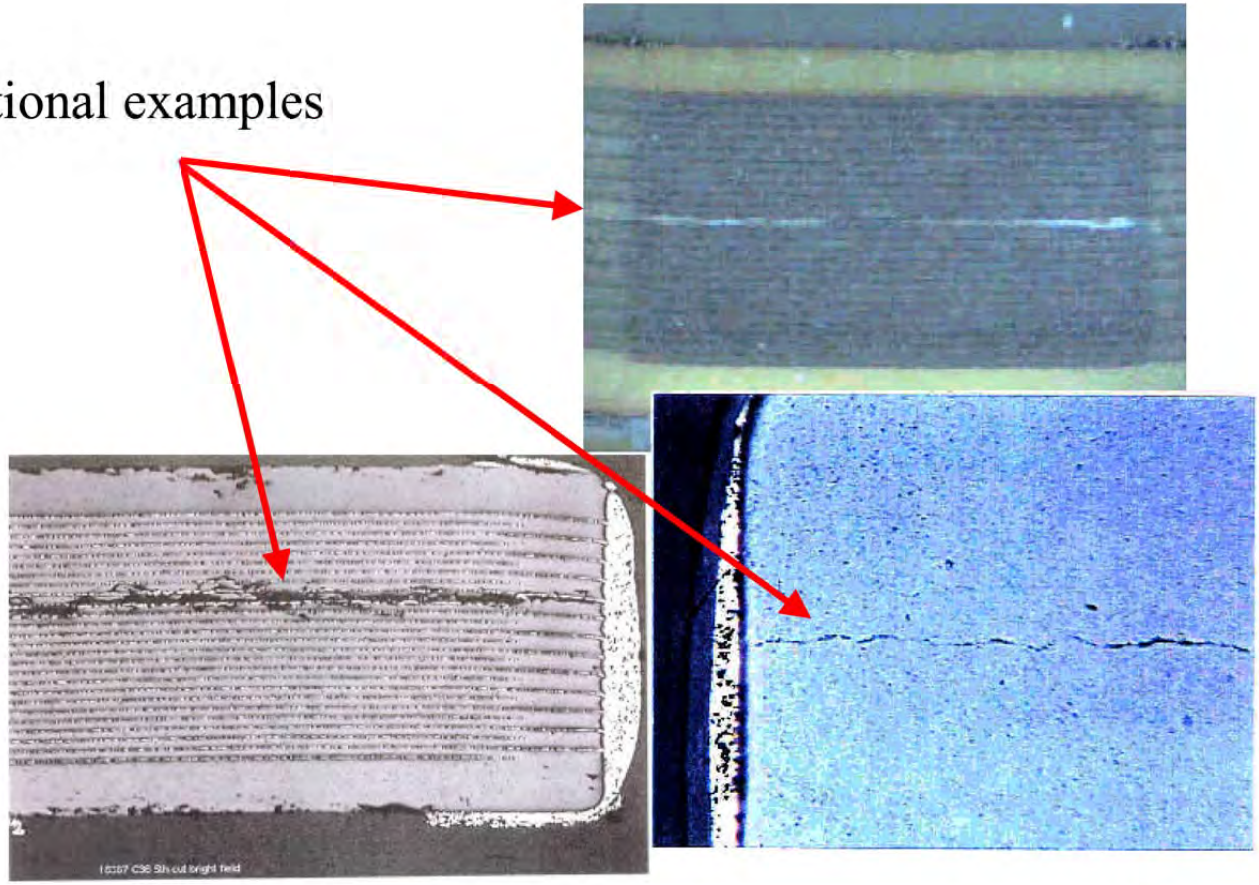


Knit Line Crack (Delamination)



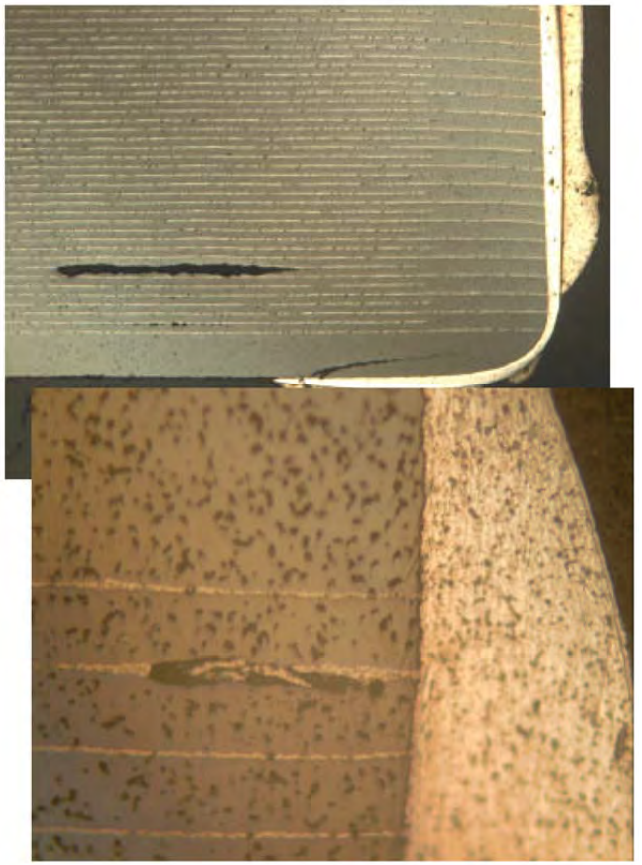
Knit Line Cracks (cont.)

Additional examples



Voiding

- Voids bridging two or more electrodes can become a short leakage current path and a latent electrical defect
- Large voids can also lead to a measurable reduction in capacitance
- Root causes
  - Contamination, both organic and inorganic, in the ceramic powder
  - Non-optimized burnout process

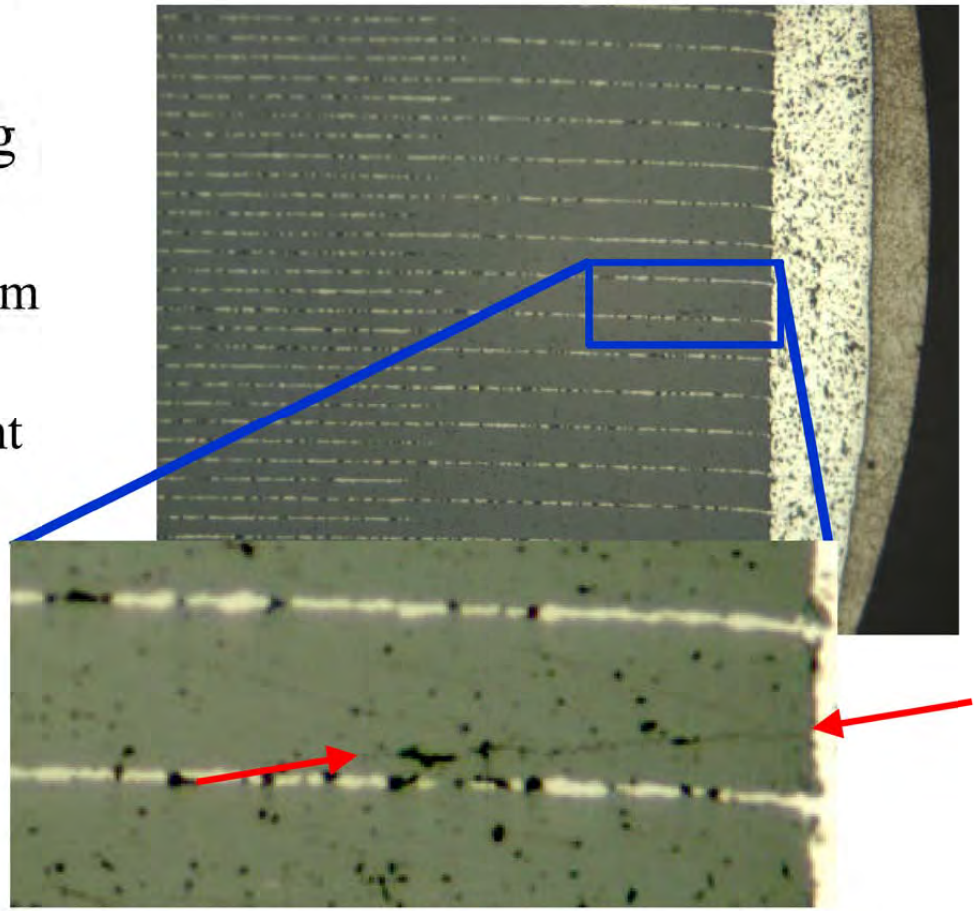


Extrinsic Defects

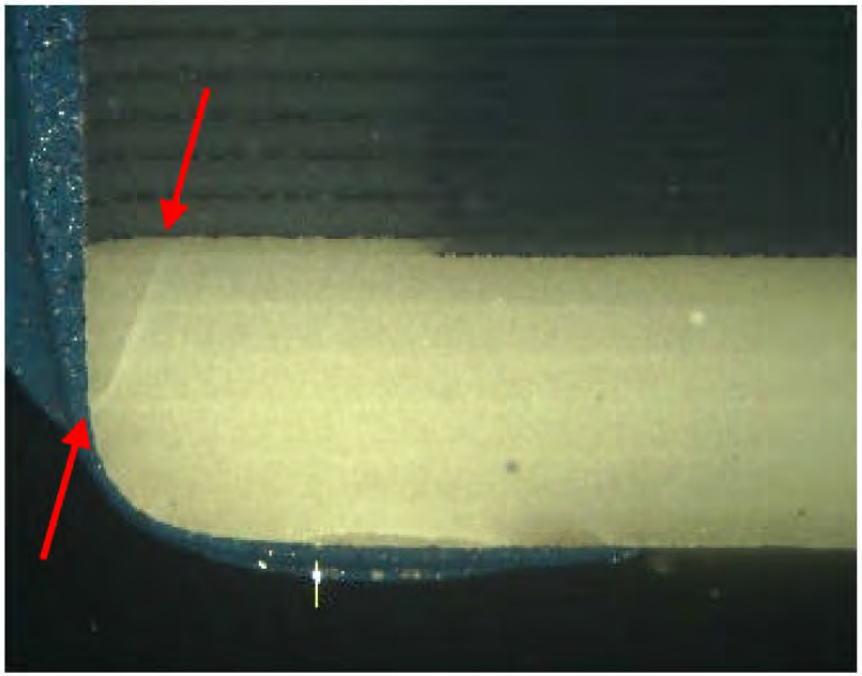
- Extrinsic Defects
  - Handling Cracks
  - Thermal Shock
  - Flex Cracks
  - Silver Migration
  - Tombstoning

Handling Cracks

- Occur during component handling and placement
  - Excessive stress from centering jaws
  - Excessive placement stresses



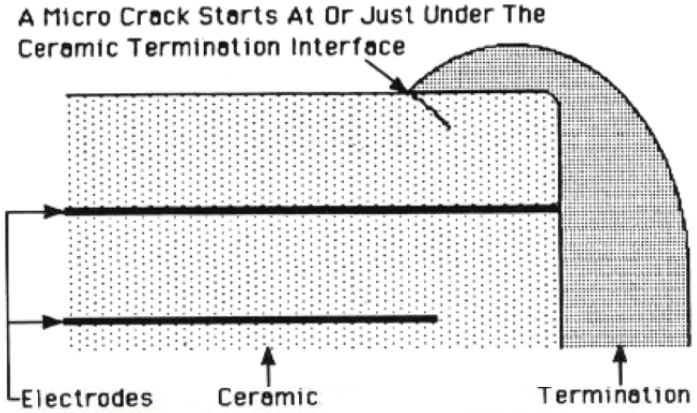
Handling Cracks (cont.)

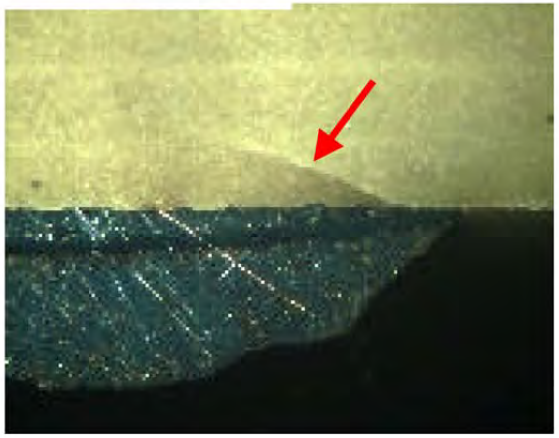


Thermal Shock Cracks

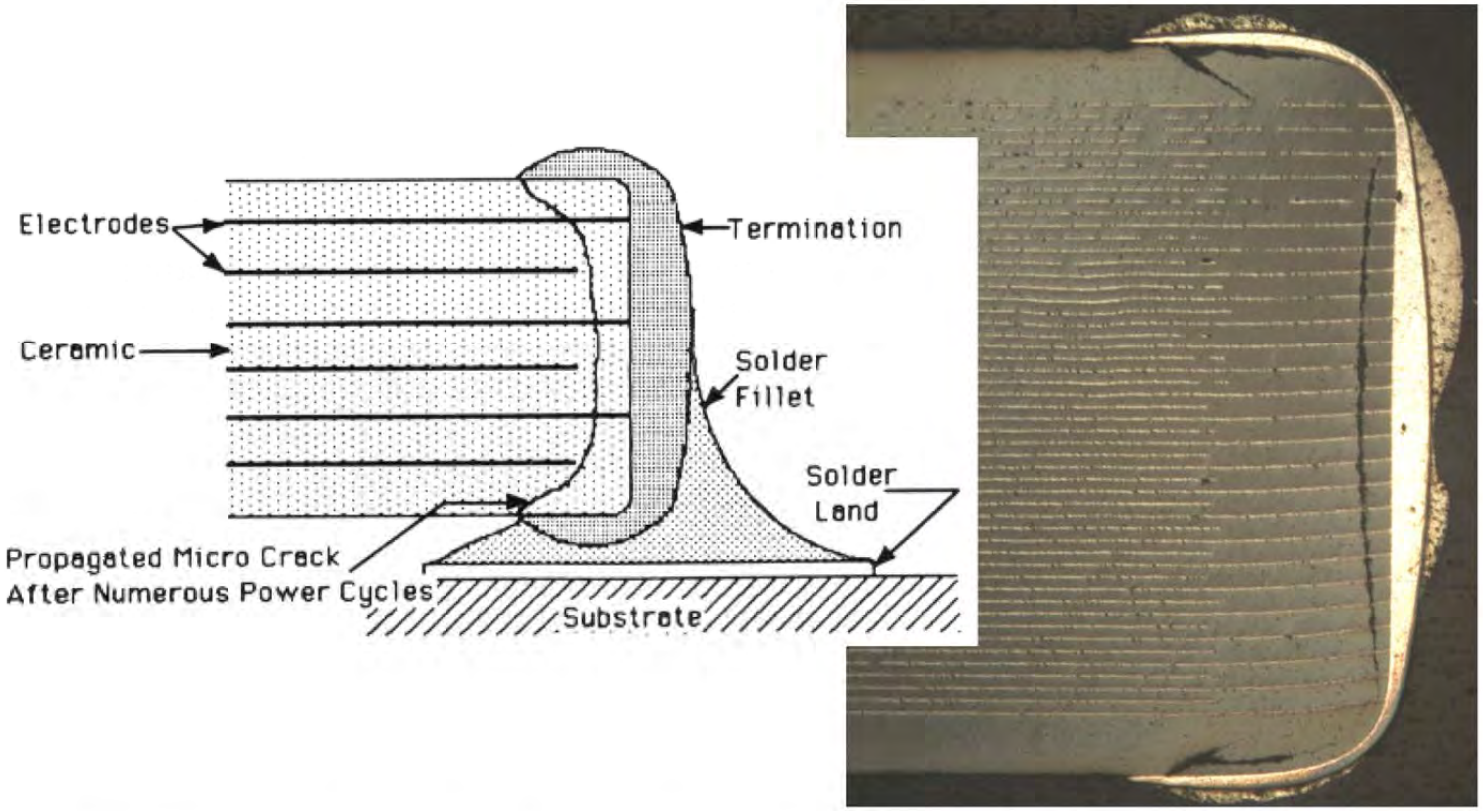
- Occurs due to excessive change in temperature during wave solder, solder reflow, cleaning or rework
- Three manifestations
  - Visually detectable (rare)
  - Electrically detectable
  - Microcrack (worst-case)

Thermal Shock (microcrack)





Microcrack (cont.)



Thermal Shock Solutions

- If possible, avoid wave soldering
  - Highest heat transfer rate and the largest temperature changes.
- Minimize rapid temperature changes
  - Room temperature to preheat (max. 2-3^{o}C/sec.)
  - Preheat to approximately 150^{o}C
  - Preheat to maximum temperature (max. 4-5^{o}C/sec.)
  - Cooling (max. 2-3^{o}C/sec.).
- Make sure assembly is less than 60^{o}C before cleaning

Optimum Reflow/Wave Profiles

- Infrared Reflow (IR)
  - Peak temperature of 215-219°C
  - 45-60 seconds above melting point
  - Pre-heat zone at 100° and at 150°C to activate the flux and to allow uniform heating of the board respectively
- Forced Air Convection
  - Better heating efficiency, less sensitive to material properties than IR
  - Temperature gradient across the board becomes much less significant
  - Long soak time not as important
- Wave Solder
  - Belt speeds of 1.2 to 1.5 meters/minute
  - Wave temperature should be 232° ± 2°C
  - Preheat of ~140°C with a dwell time not to exceed 10 seconds

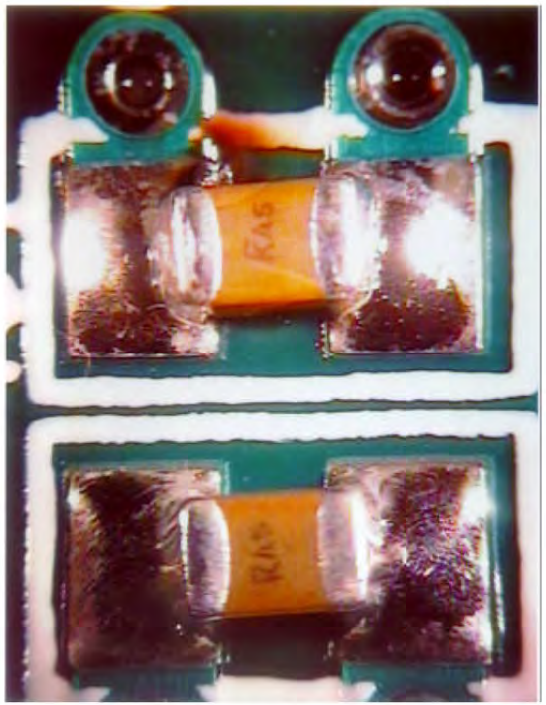
Thermal Shock Solutions

- Use best practices of rework on MLCC's
  - Preheat to 150°C
  - Hot air vs. Solder iron
- Change the capacitor
  - Thinner capacitors
  - Smaller capacitors
  - Choose a dielectric material with a higher fracture toughness (C0G, NP0 > X7R > Z5U, Y5V)
- Change the board
  - Smaller bond pads (reduced thermal transfer)
  - Smaller solder joint fillets

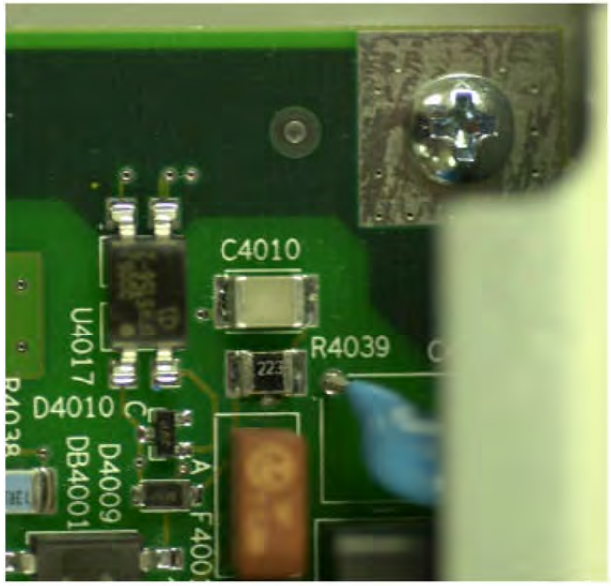
Flex Cracks

- Due to excessive flexing of the board
- Occurrence
  - Depaneling
  - Handling (i.e., placement into a test jig)
  - Insertion (i.e., mounting insertion-mount connectors or daughter cards)
  - Attachment of board to other structures (plates, covers, heatsinks, etc.)

Flex Cracks

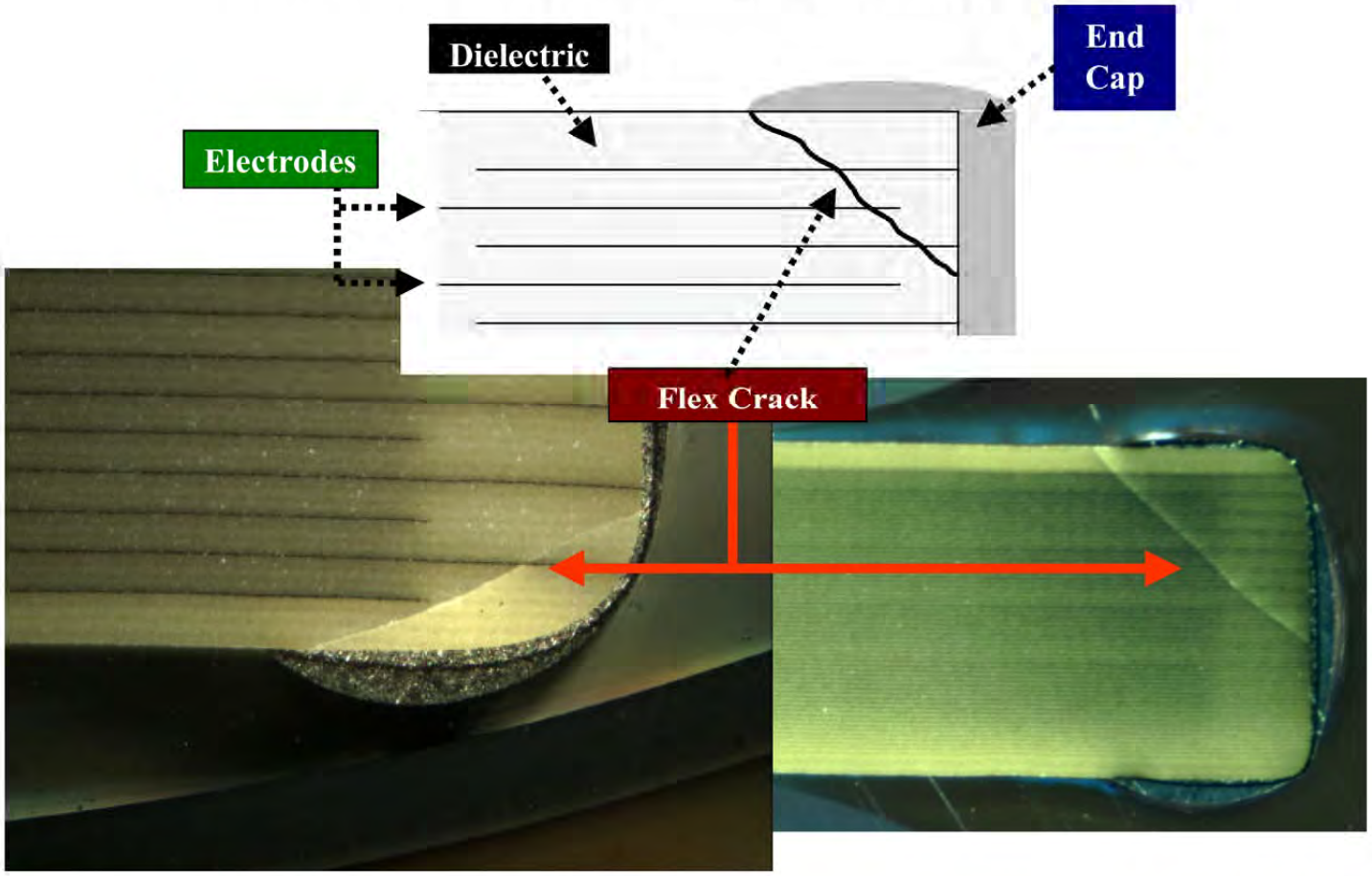


Root Cause:
Connector Insertion

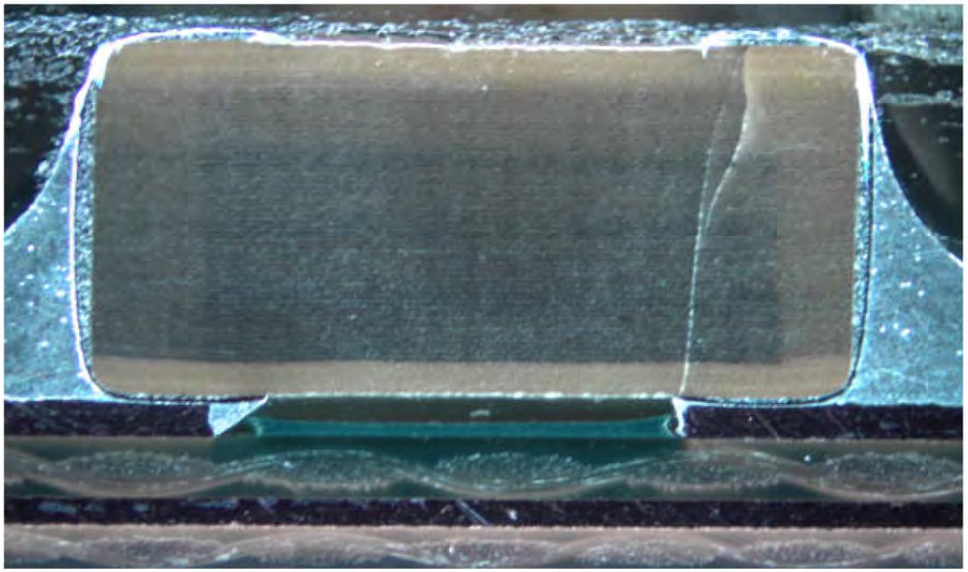


Root Cause:
Tightening of Screw

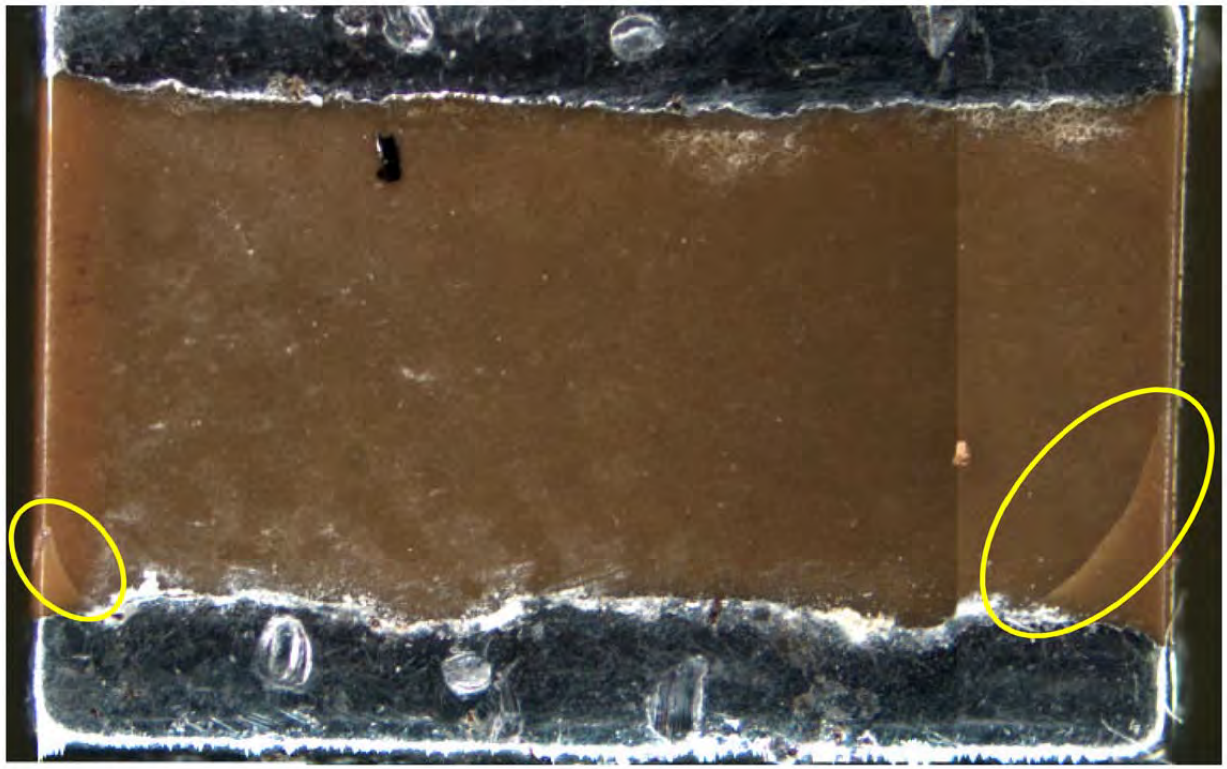
Flex Crack (examples)



Flex Cracks (extreme)



Flex Crack (examples – cont.)

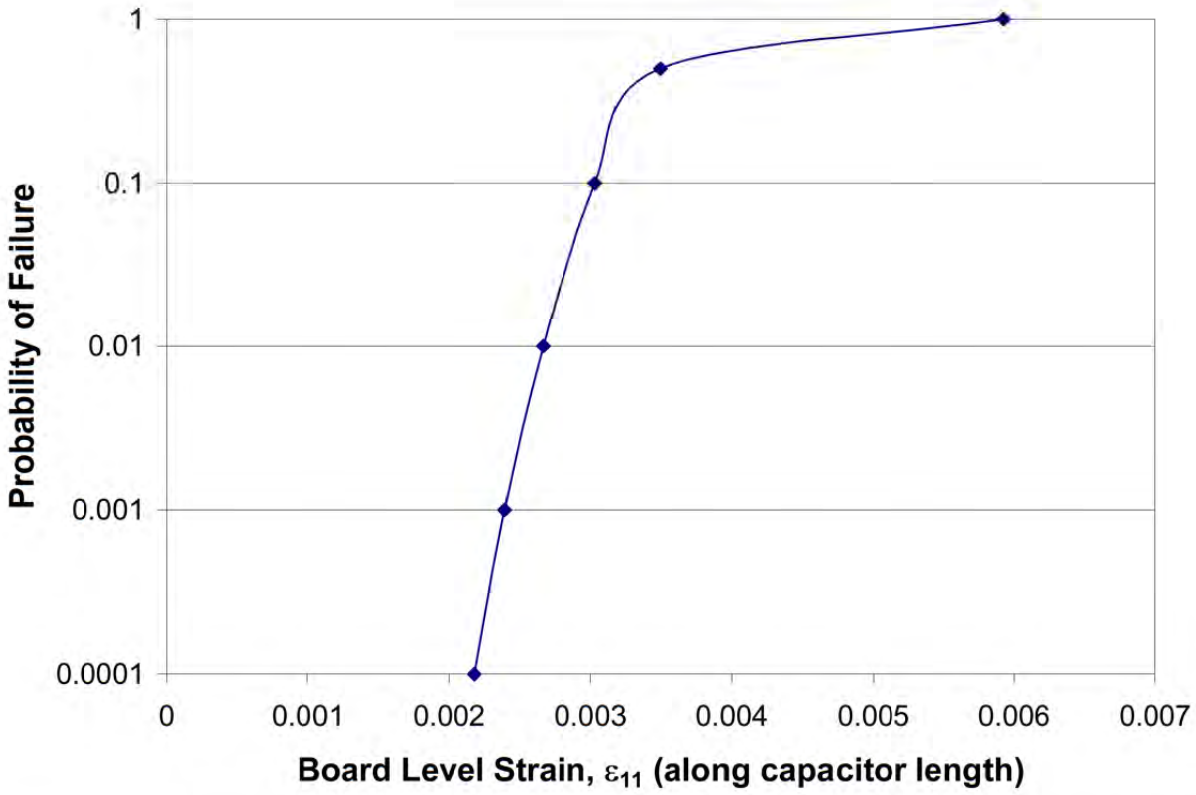


When does Flex Cracking Occur?

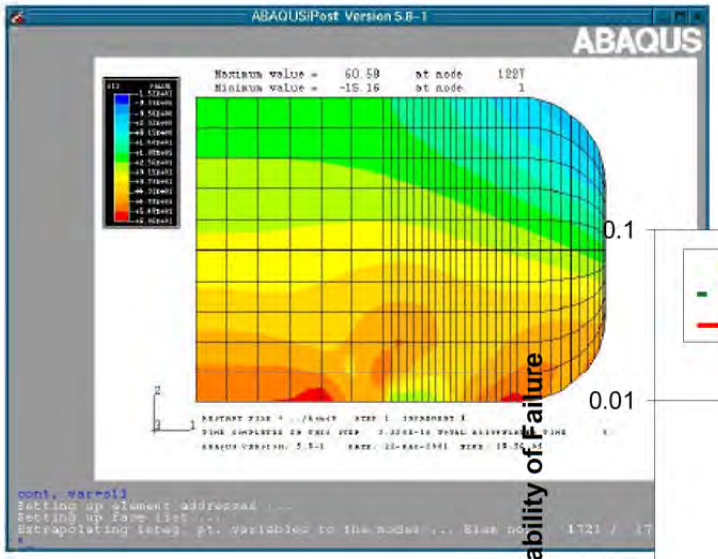
Failure Rate	100ppm	0.1%	1%	10%	50%
Displacement (mm/in.)	1.84 / 0.07	2.02 / 0.08	2.25 / 0.09	2.56 / 0.10	2.95 / 0.12
Radius of Curvature (mm/in.)	367 / 14.4	334 / 13.4	300 / 11.8	264 / 10.4	229 / 9.0
Board-Level Strain	2.18E-03	2.39E-03	2.67E-03	3.03E-03	3.50E-03

Based on bend test performed by Kemet

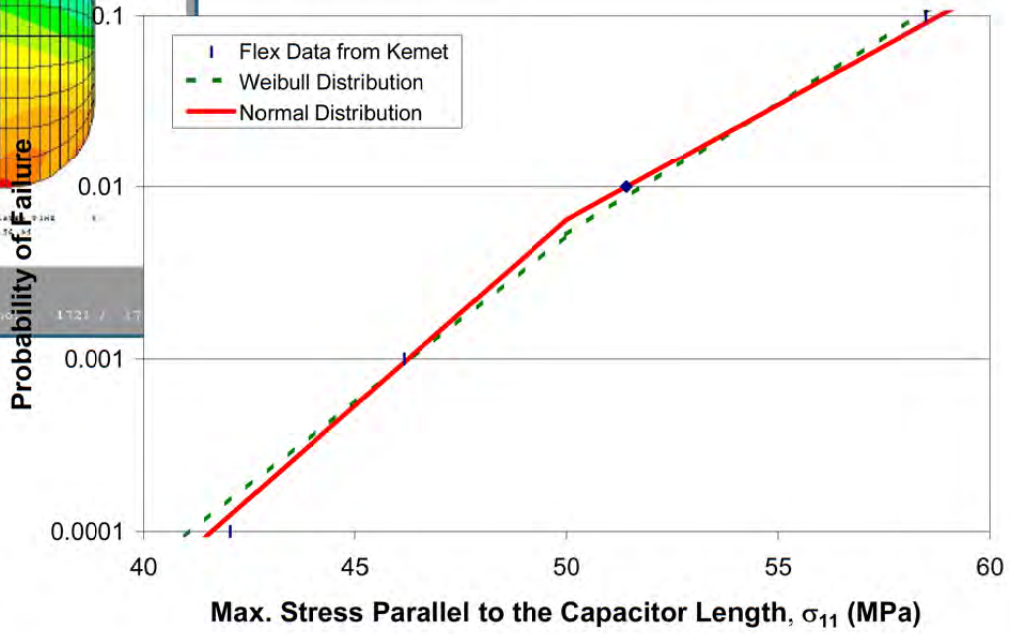
Flex Cracking (board strain)



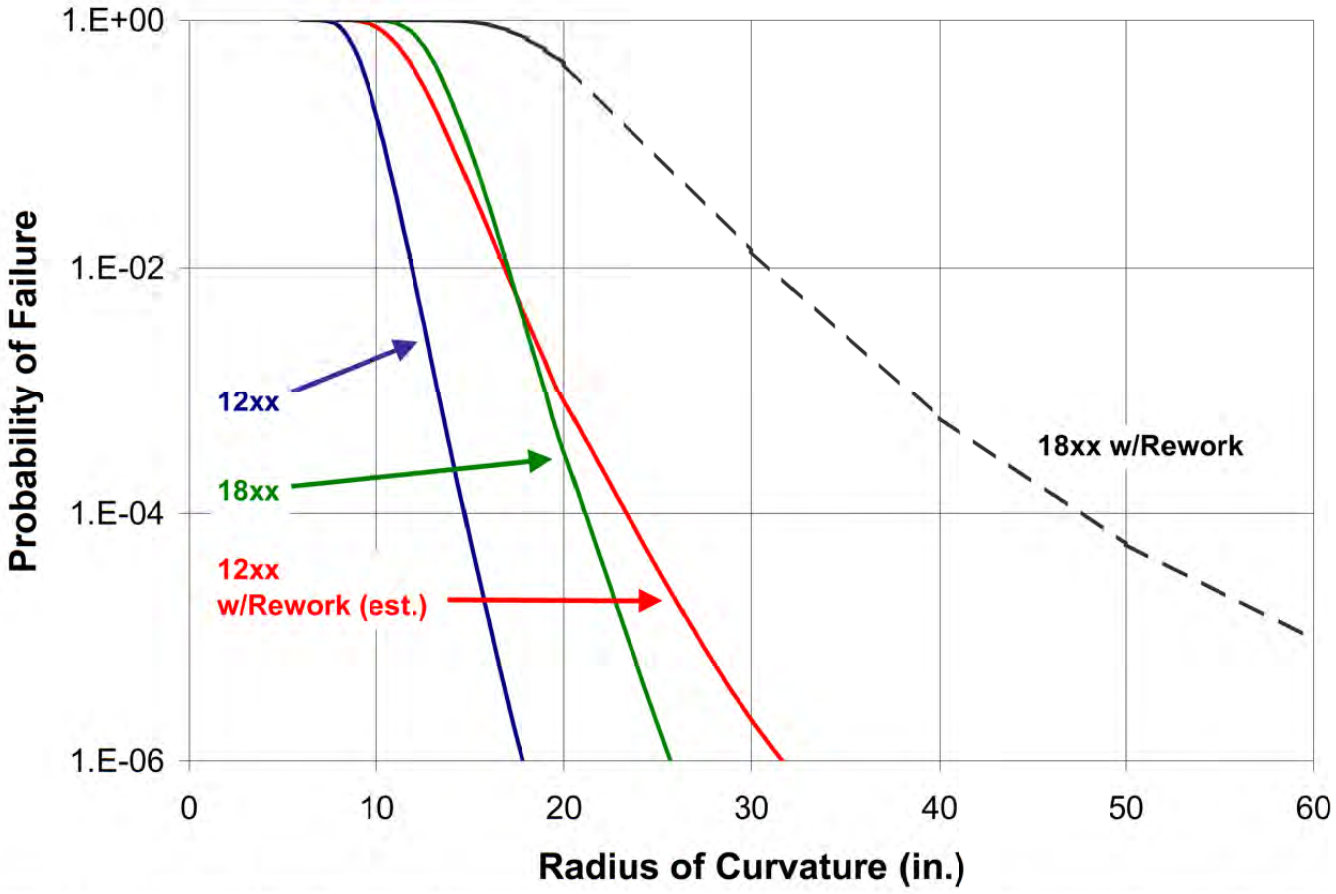
Flex Cracking (internal stress)



CALCE used FEA to determine the internal stress that induces flex cracking



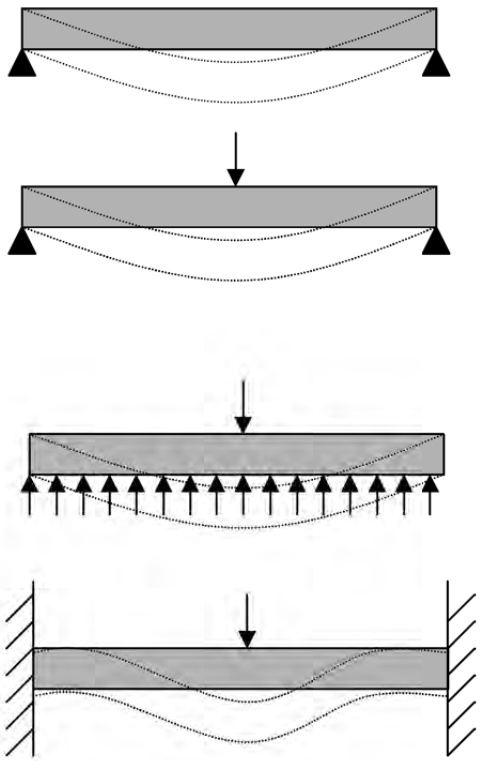
Probability of Flex Cracking



Bend Radius Calculations

Note: Bend radius will be strongly dependent upon attachment configuration.

The same displacement can result in 1/3rd the bend radius.



$$\Delta_{max} = L^2/8\rho$$

$$\Delta_{max} = L^2/12\rho$$

$$\Delta_{max} = L^2/16\rho$$

$$\Delta_{max} = L^2/24\rho$$

Flex Crack Solutions

- Design Changes
  - Smaller capacitors
  - Choose a dielectric material with a higher fracture toughness
  - Reduce bond pad width
  - Replace with tantalum capacitors
  - Improve insertion and bolt tolerances
  - Avoid placing MLCC's near board edges and holes

Flex Crack Solutions

- Process Changes
  - Minimize board warpage
  - Use of board stiffeners
  - Avoid high stress depaneling methods, such as manual break, shear or "pizza cutter". Routing is preferred.
  - Use of torque limiters
  - Appropriate fixturing of in-circuit testing (ICT)
  - Additional training

Silver Migration

- Low standoff height of MLCC's can result in high halide ion concentration
  - Causes migration of the silver-glass frit
  - Can lead to excessive current leakage
- Can be resistant to cleaning

Tombstoning

- Also known as drawbridge
- Root Causes
  - Excessive solder
  - Solder Mask Overthickness
  - Orientation

Screening Strategies

- Primarily dependent upon the defect type
- Avoid if possible (low return on investment)
  - Uses scarce resources (time, money, manpower)
  - Push down the supply chain
- Select non-destructive over destructive

Purpose of Screening

- To prevent failures
- Capacitors store a high amount of energy
  - Charring of the MLCC
  - Damage to adjacent components
  - Destruction of the board or product
  - Damage to customer site

Screening (Intrinsic Defects)

- Visual
  - Low success rate (most defects are internal)
- Xray
  - Very low success rate
- Scanning Acoustic Microscopy (SAM)
  - Includes variants, such as scanning laser acoustic microscopy (SLAM)
  - Very successful on voids and delamination (less so on cracks propagating at 45^{o} or greater)
  - Can be performed internally or through contract work
    - Sonoscan has analyzed over 1 million chip capacitors
    - $65K capital + several days of training

Electrical Screens (Intrinsic)

- Functional Test
  - Medium success rate
  - Most intrinsic defects, except for gross defects have not initiated failure mechanisms, such as increased current leakage or reduced capacitance
- Overvoltage
  - Two modes: High voltage and ionization voltage
    - High voltage (2x rated voltage)
    - 15 volts corresponds to the ionization potential of nitrogen (14.5 eV)
- Piezoelectric testing
  - Recently demonstrated (not widely adopted)
  - Effective on voids and delamination
  - Requires specialized equipment ($??) and training

Environmental Screens (Intrinsic)

- High Temperature Operating Life (HTOL)
  - "Dry" silver migration occurs at temperatures > 120°C
  - Migration behavior well known
- Temperature/Humidity/Bias (THB)
  - "Wet" silver migration will not occur below 65%RH
  - Kemet recommends 24 hours at 85°C/85%RH at 50 volt bias
  - Other research (Hing and Jackson, 1989) suggests a more thorough screen might be 35 hours at 85°C/ 85%RH at 100 volt bias (assumes a 25 micron electrode spacing)
- Both screens are destructive

Screens (Extrinsic)

- Acoustic microscopy is not recommended for extrinsic defects
  - Cracks propagate at 45° or greater
  - Shadowed by the end cap
- Functional test has a medium success rate
- Environmental screens can be very effective
- Methanol soak
  - Methanol is an electrically conductive liquid.
  - Capillary action and low viscosity allow methanol to wick up any surface cracks
  - Conductive film between adjacent electrodes (increase in current leakage)

Summary

- Ceramic chip capacitors can fail
  - Choose a quality supplier
  - If necessary, choose high reliability MLCC's
  - Optimize and control your assembly process
  - Always identify the root-cause of failure

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Exhibit H

TECHNICAL INFORMATION

CRACKS: THE HIDDEN DEFECT

by John Maxwell
AVX Corporation

Abstract:

Cracks in ceramic chip capacitors can be introduced at any process step during surface mount assembly. Thermal shock has become a "pat" answer for all of these cracks, but about 75 to 80% originate from other sources. These sources include pick and place machine centering jaws, vacuum pick up bit, board depanelization, unwarping boards after soldering, test fixtures, connector insulation, final assembly, as well as defective components. Each source has a unique signature in the type of crack that it develops so that each can be identified as the source of error.

CRACKS: THE HIDDEN DEFECT

by John Maxwell
AVX Corporation

Introduction

Cracks in ceramic surface mount technology (SMT) components limit assembly reliability and yields. These cracks manifest themselves as electrical defects: intermittent contact, variable resistance, loss of capacitance and excessive leakage currents. Large visible cracks and the insidious micro crack are usually blamed on the soldering process by component vendors and the components themselves by the users. The actual sources of cracks include both solder processing and to a lesser extent, defective components; but other very significant sources exist as well.

Cracks can be introduced at any process step used to manufacture an assembly. These sources include thermal shock by the soldering and cleaning processes, pick and place machine centering jaws and vacuum pick up bit, board depanelization, unwarping boards after soldering, test fixtures, connector installation, final assembly, defective or wrong value components and cracked or missing solder joints due to board design. Many production areas will have most if not all crack sources present so one may obscure the others. Luckily each source of cracks has a unique signature such that even the type of pick and place machine is easily identified.

Thermal Shock

"Thermal shock" is the pat answer for all cracks but is responsible only 20-25% of the time with the other sources of defects making up the balance. When thermal shock is present, it can easily obscure all other crack sources so an understanding is needed for each type of defect to identify and eliminate them. Thermal shock is mechanical damage caused by a structure's inability to absorb mechanical stress caused by excessive changes of temperature in a short period of time. This stress is caused by differences in CTE (coefficient of thermal expansion), δT (thermal conductivity) and the rate of change of temperature. CTE and δT are a function of the materials used in the component's manufacture and the rate of change of temperature is dependent on the soldering process. Thermal shock is a complex issue that has been covered earlier in detail[1,2] so only an overview of those cracks is presented.

Multilayer ceramic capacitors are sensitive to thermal shock due to device construction consisting of interleaved layers of ceramic dielectric and metal electrodes with metal terminations for electrical contact. This structure has been described earlier.[3] (See Figures 1 and 2)

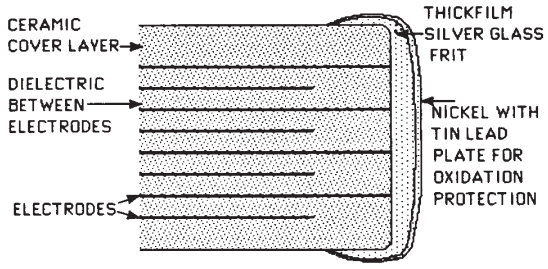


Figure 1. MLC Structure

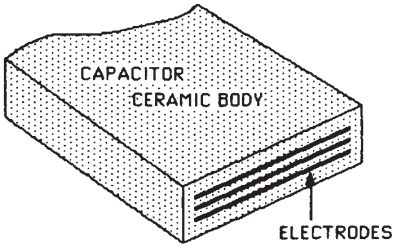


Figure 2. MLC Monolithic Structure Without Termination

TABLE I
CTEs AND δTs OF
COMPONENT MATERIALS

Material	CTE (ppm/°C)	δT (W/m°K)
Alloy 42	5.3	17.3
Alumina	≈7	34.6
Barium Titanate	9.5-11.5	4 to 5
Copper	17.6	390
Filled Epoxy	18-25	≈0.5
$Si0_2$	.57	3.4
Nickel	15	86
Silver	19.6	419
Steel	15	46.7
Tantalum	6.5	55
Tin Lead Alloys	≈27	34

Compatible materials used in MLC manufacture have differences in CTE and δT that cause internal stress. When the temperature rate of change is too great, thermal shock cracks occur. These cracks are initiated where the structure is weakest and mechanical stress is concentrated. This is at or near the ceramic/termination interface in the middle of the exposed termination. Mechanical stress is greatest at the corners where the chip is strongest but cracks tend to start where the structure is weakest. When temperature rates of change are excessive, as in uncontrolled wave soldering, large visible U-shaped or thumbnail surface cracks are formed.

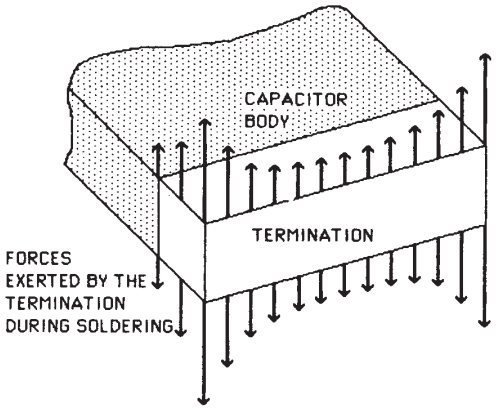


Figure 3. Stress Risers Caused by the Termination on the MLC Body

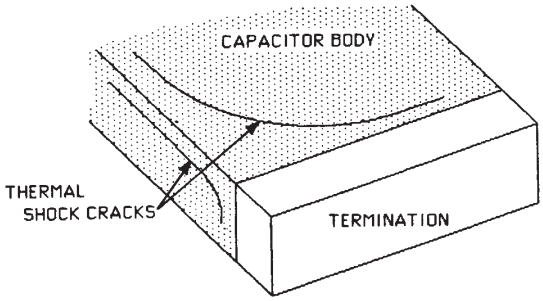


Figure 4. Extreme Thermal Shock Cracks in MLCs

Thermal shock has two manifestations, obvious visible cracks (Figure 4) and the more insidious, invisible micro crack (Figure 5). The same forces are involved but on a smaller magnitude so smaller cracks are formed. Again it starts in the middle of the exposed surface at or just under the ceramic/termination interface and propagates slowly with temperature changes or assembly flexure during handling. In a matter of weeks a micro crack can propagate through the ceramic causing opens, intermittents or excessive leakage currents, a time bomb due to processing (Figure 6).

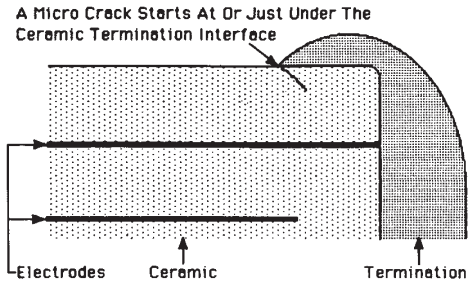


Figure 5. The Micro Crack Location

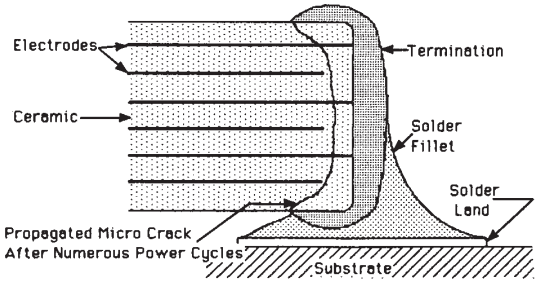


Figure 6. A Propagated Micro Crack After Power Cycling

Thermal shock cracks are always caused by improper solder processing or cleaning. Wave soldering is the biggest culprit because it has the highest heat transfer rate (using liquid metal) and the largest temperature changes which cause both visible and micro cracks. Vapor phase soldering has the second highest heat transfer rate and temperature changes which can induce micro cracks when inadequate preheat is used. Infrared (IR) reflow soldering has the lowest heat transfer rates and thermal shock is unheard of for this soldering technique. Assembly cleaning cannot be ignored because thermal shock can occur during heating or cooling. An assembly should be allowed to cool to less than 6O°C before it is subjected to the cleaning process.

Pick and Place Machine Damage

Pick and place machine damage constitutes the largest source of defects in a manufacturing environment today. These defects are usually erroneously called "Thermal Shock Cracks" sending both the vendor and manufacturing groups down the wrong path looking for a solution. This damage is caused by the centering jaws or vacuum pick up bit with the frequency of damage time and shift dependent. With the exception of gross damage, pick and place machine cracks do not appear until after the part has been subjected to the soldering process but are very unique. These too are large, visible cracks and invisible internal damage that is also a processing time bomb.

Vacuum Pick-Up Bit

Damage or cracks caused by vacuum pick-up bits is straightforward and obvious (Figure 7). It usually consists of a crushed circular- or halfmoon-shaped area on the exposed surface of the chip and is usually quite rough with ragged edges or can be a visible impression of the placement bit. Additionally the halfmoon or circular areas will match the bit diameter. Another manifestation of bit damage occurs where solder paste is used on reflow soldered boards. Tensile cracks may be found originating on the board side of the component going from side to side in the middle of the part. These cracks may propagate to the top surface and will be rough or ragged with possible pieces of the capacitor burst from its bottom surface and trapped between the capacitor and board. This is a case where the solder paste has supported the capacitor ends but not the middle, allowing the unsupported component body to crack.

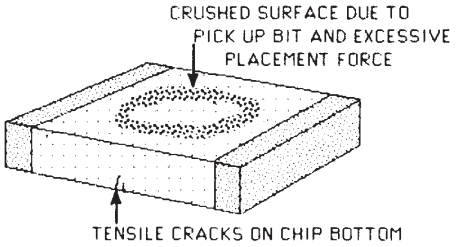


Figure 7. Placement Bit Damage With Tensile Cracks

This type of damage is caused by excessive Z-axis placement force of the bit that exceeds the rupture strength of the ceramic. Many pick and place machines use small bits (increased pounds/sq. inch) which compounds the problem by reducing the process window to avoid damage. There are two basic methods used for placement force: programmed Z-axis displacement, and pneumatic actuators. When Z-axis displacement is used for parts placement, component thickness variations, board (substrate) warpage, component land plating and solder paste thickness variations are the usual culprits. Pneumatic actuators have a separate set of problems that also include component thickness variations and warped boards. Air pressure variations within the plant can be a major cause of excessive placement pressure cracks. Also as the air cylinders age, they get sticky or suffer pressure loss, both of which are compensated for with increased air pressure and excessive force placement defects. Z-axis placement force is a process parameter that requires mandatory monitoring and control.

Centering Jaw Damage

Pick and place machines have gone through an interesting evolution from no centering jaws to centering jaws and now back to machines with no centering jaws. The newer machines are much faster and use machine vision to properly place parts instead of using mechanical alignment. Centering jaws (or mechanical alignment) will be with us for some time and will continue to cause problems. Pick and place machines come with two varieties of centering jaws: top centering, and bottom centering. Each type has its own unique crack signature and will be discussed separately.

Top Jaws

Top centering jaw machines have the alignment jaws or tweezers as part of the pick up mechanism (Figure 8) such that the part is centered (aligned) when plucked from the component carrier (embossed tape, etc.) or during the travel time between pick up and placement. Capacitors, resistors, transistors and integrated circuits (IC) require different sizes of centering jaws which slow production rates with jaw changes. It is common practice to adjust a single jaw set to accommodate the full range of components which results in higher forces on smaller parts when the jaws are adjusted to center large ICs. Not only are higher forces used but the jaw contact areas are reduced so centering is done only on the IC body and not the leads. Now only a small portion of a capacitor's side and end surface area is used for centering which gives rise to pressures that exceed the rupture or tensile strength of the ceramic causing internal defects and visible cracks (Figure 9).

Barium titanate ceramics have tensile strengths in the range of 8-10,000 psi and rupture strengths of 10-15,000 psi. These numbers seem high until one realizes that a phonograph stylus exerts similar forces on vinyl records. A few ounces of force translates to thousands of psi when small surface areas are involved. Typical pick and place machine centering jaws are rather narrow, 40 mils (1 mm) is very common, which packs all of the force onto a small surface. Not only do the centering jaws have small contact area viewed from the top, the jaws only extend to a depth of 10-20 mils from the top surface to accommodate plastic molded transistor or IC bodies without interfering with their leads. We have the recipe for high speed assembly of cracked components.

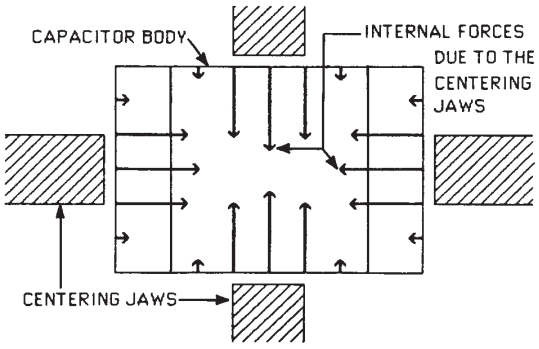


Figure 8. Top View of Capacitor Body, Centering Jaws and Force Concentration

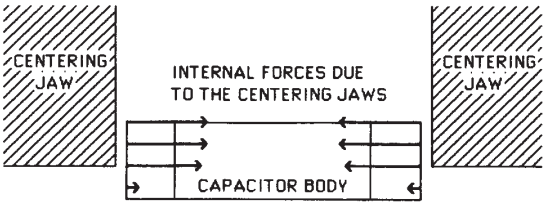


Figure 9. Side View of Capacitor Body, Centering Jaws and Force Concentration

These force concentrations from narrow centering jaws create large force or shear gradients where cracks develop. These cracks manifest themselves as visible surface cracks or internal cracks between two or three electrodes. Surface cracks originate along lines of maximum compression and ceramic displacement (Figure 10).

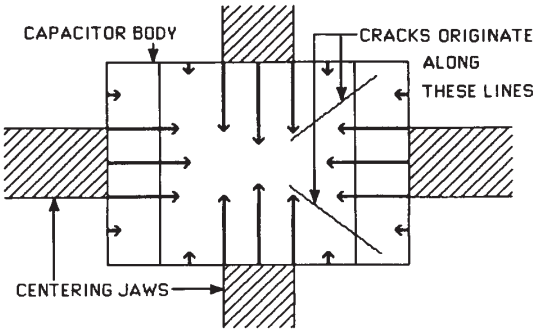


Figure 10. Surface Crack Origins

Top centering jaw machines generate surface cracks that typically originate or end under the termination while thermal shock cracks radiate away from the termination with a thumbnail- or U-shape. Centering jaw cracks will typically not extend beyond 1/3 to 1/2 of the chip length. These are quick clues to determine the source of cracks. Figure 11 illustrates typical top centering jaw damage after soldering.

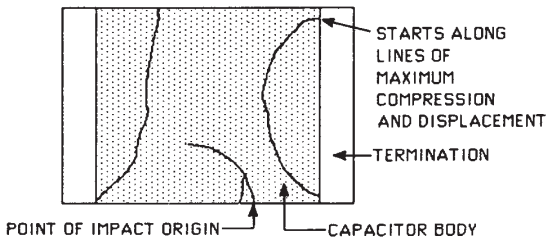


Figure 11. Typical Surface Cracks from Top Centering Jaws

As with thermal shock, there is the insidious internal crack from centering that is generated when the process is just a little out of control which is like being just a little pregnant, it doesn't show up until later (Figure 12). This defect manifests itself as excessive leakage that shows up many months after assembly. There are no external visible signs and these cracks are very difficult to find with DPA (destructive physical analysis) techniques. This is because the crack is very small and only extends across two or three electrodes in the capacitor body making it very easy to polish past the defect site.

Some impact site cracks are easy to find with DPA when the centering jaw forces are low enough to just cause invisible damage. Typically these cracks have obvious origins 10-15 mils below the top surface which will be the bottom of the centering jaws, again the region of maximum stress gradients. These cracks may be deeper than 10-15 mils depending on the centering jaw depth but they will have their origins at the bottom of the jaw.

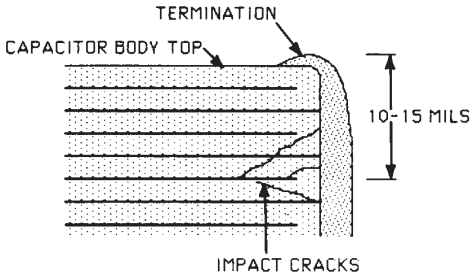
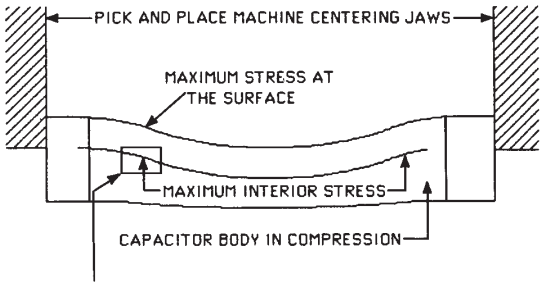


Figure 12. Typical Internal Centering Jaw Damage

Inter-electrode defects are the most difficult to find with DPA but they too occur at the same depth as the more obvious cracks, at the bottom depth of the centering jaws. These small cracks are again 10-15 mils below the surface (or jaw depth), near the maximum stress gradients exerted by the centering jaw. The capacitor body is slightly deformed by the compressive forces of the centering jaws. This deformation is similar to pressing on the ends of a deck of cards, and has three inflection points for this type of compression. A small crack will form between two or possibly three electrodes when the ceramic layer ruptures, relieving the stress. A small internal defect that is very difficult to find but can still kill reliability (Figures 13 and 14).



See Figure 14.

Figure 13. Capacitor Under Compression from Centering Jaws

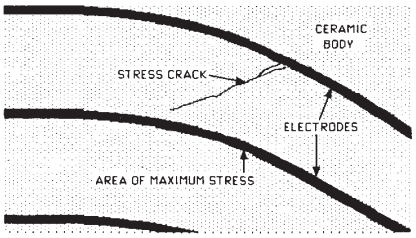


Figure 14. Exaggerated Inter-Electrode Distortion

Ceramics used to make MLC capacitors have excellent abrasion characteristics which cause centering jaw wear (Figure 15). Once this wear becomes pronounced (a tenth of a mil or so), a new type of crack can appear even though the equipment has not generated defects in the past. This problem shows up when capacitor lots or vendors are changed and the parts are now slightly thicker. Now all of the force is concentrated in the top few mils, the rupture strength is exceeded and the part cracks. Worn centering jaw induced cracks are typically in the middle of the part extending from side to side on the top surface (Figure 16).

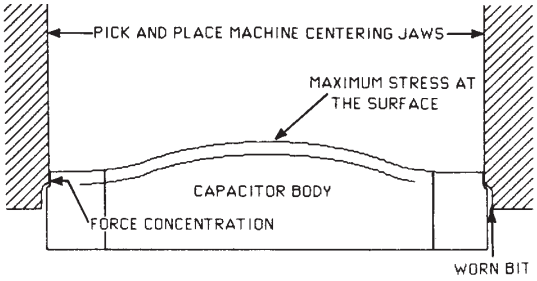


Figure 15. Worn Centering Jaws and Capacitor Distortion

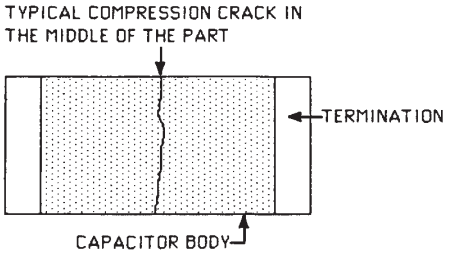


Figure 16. Typical Worn Centering Jaw Crack

Another type of damage caused by narrow top centering jaws comes about when the part is slightly rotated in its embossed tape pocket. Now all centering or alignment forces are concentrated at the sharp corners of the jaws causing chip-outs at the impact sites. There may be cracks radiating away from the impact sites on the top surface that show up after exposure to soldering temperatures (Figures 17 and 18).

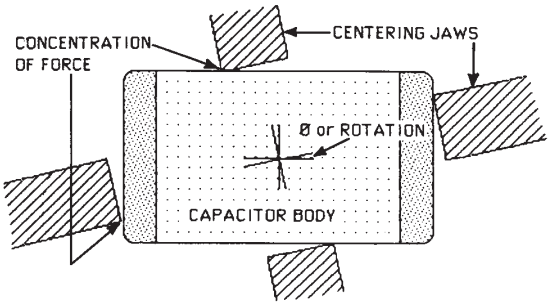


Figure 17. Misalignment of Component

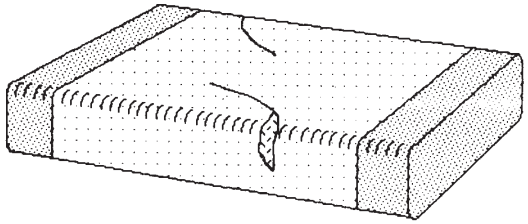


Figure 18. Resulting Damage

Botton Centering Jaws

We're not out of the woods yet with pick and place machine damage. Bottom centering jaws found on some high volume chip shooting machines also have a unique centering stress crack. These cracks appear and disappear at random intervals and have been tracked to debris buildup on the component pedestal (Figure 19). When debris is present, the component will not be flat or square to the centering jaws, concentrating the alignment forces on a corner causing a displacement crack.

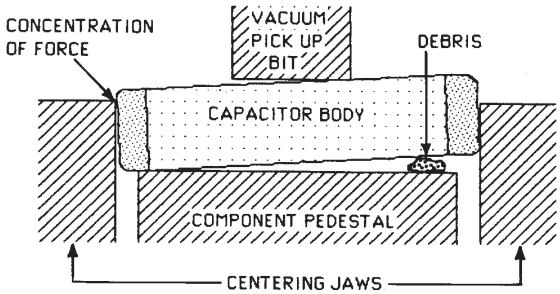


Figure 19. Bottom Centering Jaws With Debris

This crack propagates from side to side on the top surface (Figure 20) and is similar to surface rupture cracks caused by worn top centering jaw machines. Bottom centering cracks also extend along one or both sides of the part near the surface into the termination. These cracks are eliminated with a rigid cleaning and maintenance regime.

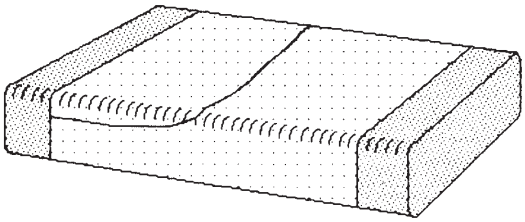


Figure 20. Typical Bottom Centering Crack

Complete process control is mandatory in the placement process to eliminate damage. This includes proper periodic maintenance and monitoring of all process variables. Using mechanisms the largest possible pick up bit, lowest possible placement force and centering jaws that spread alignment forces over the entire side surfaces of the component are changes that may slow the placement process but it is preferred to high speed assembly of damaged components.

Plant air pressure, board warpage and thickness variations, solder paste thickness on land patterns, uniformity of solder paste thickness after screening, adhesive volume control and placement force are parameters that may need control. It is always best to monitor all in the beginning and decide later which are not important for a manufacturing area instead of controlling none and trying to find what is important when failures occur.

Warp Cracks

Cracks caused by bending a soldered assembly during depanelization, test, component placement on the opposite side, connector assembly, final product assembly or unwarping a board after soldering all fall under the heading "WARP CRACKS" and are as unique as thermal shock or placement cracks. In each case, the tensile strength of the ceramic has been exceeded and a crack is formed. These cracks do not need thermal processing such as soldering to propagate but occur with an audible snap.

The primary cause of cracks is the actual board warpage but solder joint mass has an effect on when cracks occur. Excessive solder transfers all stress to the component and too little solder causes early fatigue in the joint. Proper solder joint formation is a function of the soldering process, pad design and mass of solder present and will be covered in another paper.

Allowable bending of finished assemblies is another specification that cannot be an extension of thru hole technology because the entire component is exposed to stress. There are two possible approaches to board bending specifications: a linear mils/inch, or a more realistic minimum bend radius. (See insert.)

Minimum bend radius has a very small allowable deflection in a short segment length but allows a large deflection in long assemblies. For example, a one-inch long segment can have no more than 8.4 mils of uniform bend with a 60-inch minimum bend radius but a four inch long board can have 124 mils of uniform bend. Uniform bend is where the board fits smoothly along the radius of a circle. If there are rigid components like large ICs (integrated circuits), transformers or connectors, then less deflection is allowed for a given board length to eliminate defects. A derivation of allowable deflection based on assembly length and bend radius is in the box below.

Board Depanelization

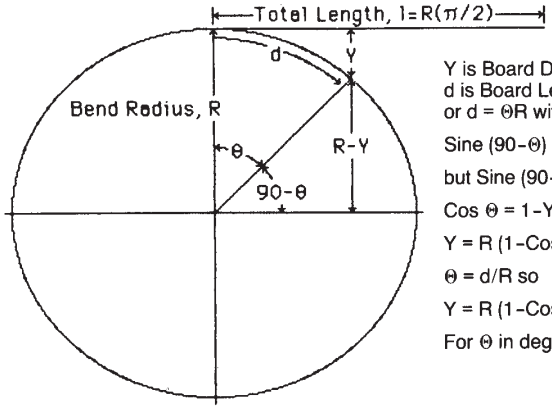
Manufacturing efficiency requires multi-up or multiple assembly panels but the potential for damage dictates single module assembly. Multi-up panels are possible but care must be taken in the depanelization process. There are six basic schemes to breakout multi-up panels but each has disadvantages.

1) Hand break out modules: Typically this approach uses perforations or a scribed line between modules so they can be broken apart by hand after soldering and cleaning. This technique has no uniformity in applied pressure or pressure application and will have erratic quality and yields. Not a viable process for volume production when operators have different yields.

2) Scissor shear: This is a carry-over for thru hole

Insert

MAXIMUM BOARD DEFLECTION FOR A GIVEN MINIMUM BEND RADIUS



Y is Board Deflection
d is Board Length
or d = ΘR with Θ in radians

Sine (90-Θ) = (R-Y)/R = 1-Y/R

but Sine (90-X) = Cos X so

Cos Θ = 1-Y/R or

Y = R (1-Cos Θ)

Θ = d/R so

Y = R (1-Cos (d/R))

For Θ in degrees, Θ = 90 (d/R)/(π/2))

EXAMPLES

MINIMUM BEND RADIUS = 60″

A) 4″ Long Board

Ymax = 60 (1-Cos (4/60))

= 60 (1-.99794)

= .1236″

B) 1″ Segment

Ymax = 60 (1-Cos (1/60))

= 60 (1-.99986)

= .0084″

assembly techniques and is actually an extension from a sheet metal shop. There is a great deal of board bending and tearing near shear blades that can crack components and solder joints. This shearing technique can be used with care but at the loss of board real estate by placing components away from flexing edge and corners. Components located near assembly corners will receive the greatest stress because the corners are the least supported portion of the board and each corner is cut twice, once in the X direction and once in Y. Cracks generated during board shearing typically run diagonally across the top surface from corner to corner.

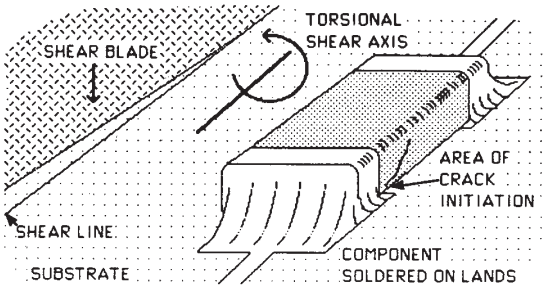


Figure 21. Typical Board Shearing Crack

Isolating components from board corners and away from edges is the best way to minimize shear damage and leave room for fixturing to reduce movement during the shearing process. Prerouting corners will further reduce stress and flexure in the critical corner areas. Leaving a 200-mil margin has been used successfully to eliminate damage while a 20-mil margin has always failed (Figure 22).

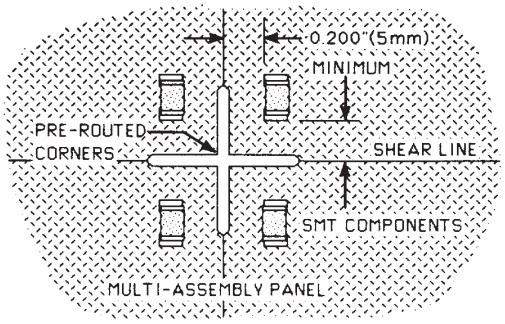


Figure 22. Prerouted Corners to Relieve Stress

3) Rolling blade shear (pizza cutter): Too much flexure occurs when a rolling cutter is used because all cutting forces are concentrated in a small moving area. It is very difficult to fixture a board to minimize damage when rolling shears are used; they are best reserved for pizza parlors.

4) Blanking or die shearing: Board flexure is still a problem but not to the extent of scissor or rolling shears because there is no tearing of the substrate or bending of corners. The entire edge of the module is supported during the shearing process which restricts movement. Components still need to be isolated from the edge and to use thinner substrate material. (.031" or possibly .047") which is weaker and easier to cut. Large boards are difficult to support and fixture while thick substrate material transfers too much stress to the components. This process is best used on blank boards or small modules on thin substrates with isolated components.

5) Sawing: Board sawing does not induce the extreme board flexure during the cutting process, eliminating component stress and damage. Gang saws are available that are very fast, two passes and the assembly is done. Semiconductor industry needs have been supplied with a wide variety of programmable saws that fill the needs of small runs or prototyping of SMT assemblies. Unfortunately saws are not easily used with odd shapes or curves; these shapes need to be prerouted prior to assembly driving up substrate cost. Saws are best suited for square or rectangular boards.

6) Water jet cutting: This is the most flexible SMT assembly cutting technique available with the simplest fixturing but has the highest capital expense for equipment, but cost is coming down.

Shears should be avoided if at all possible to depanelize SMT assemblies but if they must be used, isolate components from edges and corners and prerout corner areas to minimize damage. Saws or water jet cutting do not induce damage and they are preferred methods for depanelization.

Warping Boards After Soldering

This is a broad subject area because it includes placing final assemblies in test fixtures, installing connectors or other large components, stacking assemblies in trays or 2 x 4s with slots to await further processing, final product assembly, flattening an assembly to eliminate warp after soldering or mounting components on the second side after soldering the first side. This entire class of defects has similar failure modes and induced cracks due to excessive substrate bending and component stress.

Post soldering assembly handling can be a major source of cracks because components are oriented across stress gradients instead of parallel to the gradient. When tooling holes on the assembly do not meet the respective pins on a test system or pick and place machine, the tendency is to force fit the assembly. The “use a bigger hammer to make it fit” syndrome does not work with SMT assemblies, latent defects are the only result. Improper storage of soldered assemblies can be another source of cracks if assemblies are allowed to sag or warp when placed in trays or vertical slots. Warping a board as it is screwed into a chassis or attaching connectors or other large components can have the same effect, cracked components when oriented across stress gradients.

The resulting cracks occur very quickly with an audible snap. Depending on board warp, direction and component orientation, these defects propagate to relieve stress. Cracks initiate at the ceramic termination interface where ceramic movement is restricted by the termination and solder fillet. Because ceramic fails in the tensile mode at lower forces (10kpsi tensile vs 15kpsi compression), crack initiation will typically be at maximum tensile force sites as shown in Figure 23.

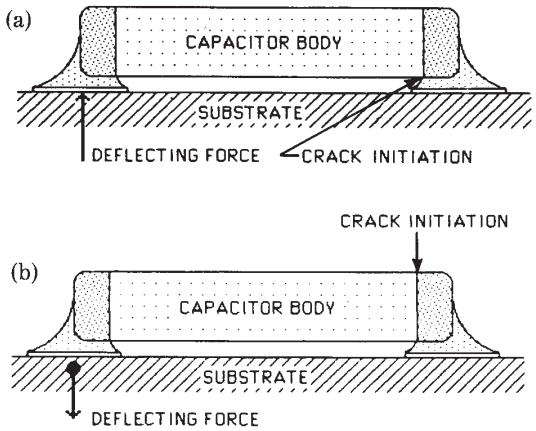


Figure 23. Crack Initiation Sites

The resulting crack propagates from the initiation site to the termination at about a 45° angle. When DPA is done on this type it is confused with thermal shock or possible pick and place damage. Thermal shock cracks typically propagate from termination to termination and pick and place cracks under the termination exhibit multiple fractures while board warp cracks typically consist of a single crack.

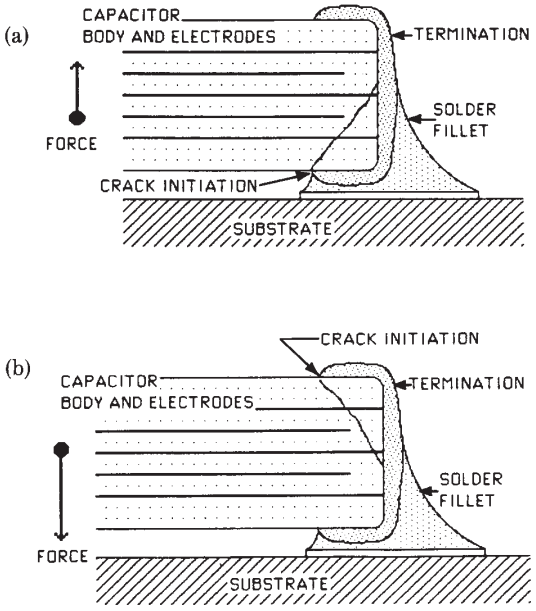


Figure 24. Typical Board Warpage Cracks

Defective Components

There are three basic types of visible internal defects in MLC (multilayer ceramic) capacitors that impair reliability: inter-electrode voids, firing cracks and knit line cracks. Each of these failures cause excessive leakage currents, impairing assembly reliability.

1) Inter-electrode voids are caused by high porosity of the ceramic or voids in the dielectric layer between opposite electrodes. This void becomes a short leakage current path and then a latent electrical defect.

2) Firing cracks have the characteristic of being perpendicular to the electrodes and typically originate at an electrode edge or end. Mechanical overstress cracks such as thermal shock and external damage originate and propagate at angles near 45°. If the DPA shows vertical cracks, then they are probably from firing.

3) Knit line cracks extend from an electrode end to the opposite termination causing a latent leakage path. Delaminations and single layer voids do not cause failures directly but are much more sensitive to mechanical stress which can rupture inter-electrode dielectric layers which then becomes the latent leakage path.

Conclusions

Every step of the SMT assembly process can induce defects. Sub ppm defects demands that these potential sources be identified and controlled to maintain high yields. Adding SMT assembly to a thru hole manufacturing area without understanding component process sensitivity leaves only a bad impression of surface mount benefits. Defective components do exist but it's only a small percentage and thermal shock is not the pat answer or major source of defects. Pick and place machines and post soldering handling induce the majority of defects.

Thermal shock cracks originate at the surface and propagate to the interior, mechanical overstress damage can start at the surface or the interior; but both thermal shock and overstress cracks propagate at angles near 45°. Defective components have voids or cracks that are perpendicular or parallel to interior electrodes.

Surface mount technology holds many benefits but there is no room for sloppy practices; now SMT assemblies need the control that semiconductor processing uses. Remember, most SMD components are the same ones found in packages that have been used reliably for decades. Now extreme care must be taken at the start of a design to identify all high stress areas and orient components to minimize possible damage. A design with minimum stress will always have higher yields and reliability.

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3. M. Kahn, "Multilayer Ceramic Capacitors - Materials and Manufacture," AVX Technical Information Series, 1981, 5 pp.

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Exhibit I

Robustness of Surface Mount Multilayer Ceramic Capacitors Assembled with Pb-Free Solder

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3 – Universal Instruments Corp., Binghamton, NY

Abstract

The movement to Pb-free soldering will result in solder joints that are significantly stiffer than those of SnPb. Of great concern to the electronics industry is the influence that this will have on some of the most common failures seen in electronic assemblies. One such failure is the cracking of surface mount multilayer ceramic chip capacitors (MLCC) when subjected to board bending events. To investigate the use of tin-silver-copper (SAC) solder on the reliability of MLCC capacitors, a series of printed wiring board flexure experiments were conducted and analyzed. The experimental design consisted of two solders and two capacitor sizes. The first capacitor tested was an 1812 X7R with samples assembled with both Sn63Pb37 and SnAg3.0Cu0.5 solder. Additional flex testing was then conducted on 0805 X7R capacitors assembled with SnAg3.0Cu0.5 solder. Results of the flex testing indicate that capacitors assembled with SnAgCu solder are more robust than those assembled with SnPb solder.

Introduction

The impact of Pb-free on the reliability of electronic assemblies is of great concern to the electronics industry. While many studies have been done to address the reliability and manufacturability of interconnects using tin-silver-copper (SAC) solder, few studies have addressed the effects on components themselves. A survey of failure analyses suggests that the majority of failures seen in electronic assemblies are related to either capacitors or printed wiring boards, as shown in Figure 1. As shown in Figure 2, a high number of the failures of capacitors are due to flex cracking of surface mount multilayer ceramic chip capacitors (MLCC).

This is not surprising given the number of such devices on a circuit board. For example, a cell phone may contain upwards of a thousand components, of which 80 to 90% are capacitors. Of these capacitors, ceramics sometimes comprise up to 60 to 70%. The high number of these devices increases their probability of failure and the probability that they will be subjected to a stress sufficient to cause failure. The concern is how the Pb-free process and materials will affect this probability of failure by printed wiring board flexure.

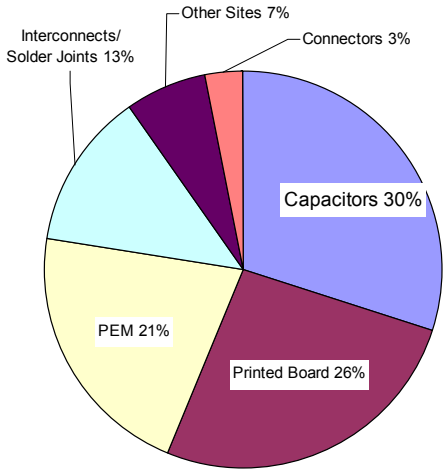


Figure 1: Most common failures by site [1]

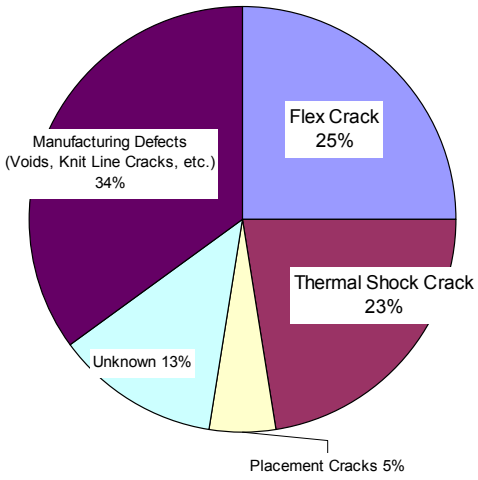


Figure 2: Capacitor failures by type [1]

The flexure of the printed wiring board can occur during de-paneling, connector insertion, screw or standoff attachment, in-circuit testing and customer use. The capacitor manufacturers recognize this and rate the robustness of the capacitors they manufacture using a standard test similar to IEC-384-1. These tests involve subjecting a test board to a three-point bend test, similar to the one shown in Figure 3.

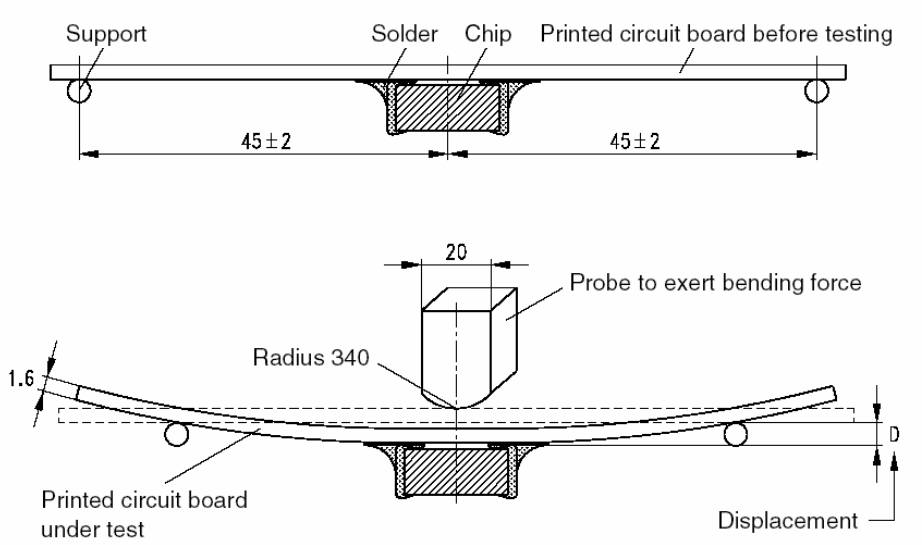


Figure 3: Industry standard capacitor bend test

Depending on the application and the class of the capacitor the displacement amount that is typically specified is either 1 or 2 mm. However, there are some manufacturers that do not provide a displacement specification on their product data sheets. A comparison of some of the displacement specifications provided by various manufacturers is shown in Table 1. The standards state that the capacitor must be able to survive the specified displacement with only a 2.5 to 20% drop in capacitance (dependent on dielectric classification).

The tests performed in this study are based upon the specifications with some minor modifications to increase the number of capacitors tested per printed wiring board coupon.

Table 1: Manufacturer deflection specifications

	Deflection Specification		
Manufacturer	1 mm	2 mm	Other
AVX [0]		X	X [1]
Vishay [4]	X	X	
SAHA/Susco Components [5]		X	
Cal-Chip Electronics, Inc. [6]		X	
TDK [7]		X	
EPCOS [8]		X	
MuRata [9]	X[2]		
Nippon Chemi-Con [10]	X[3]		
Samsung Electro-Mechanics [11]	X		
Syfer, Novacap [12]		X	X[4]
Johanson Dielectrics [13]	X[5]		X[6]
Panasonic [14]	X		
Philips, Phycomp, now Yageo [15]	X		
KOA Speer Electronics [16]		X	
Maruwa America [17]		X	X[7]
Taiyo Yuden [18]	X		
Walsin Technology Corp. [19]	X		

[1] AVX offers a soft-termination capacitor with a deflection limit of 5 mm
[2] GRM03, GRM15 capacitors, PWB thickness 0.8 mm
[3] Printed wiring board thickness 1.0 mm (1.6 is the standard)
[4] Syfer offers a polymer-termination capacitor with a deflection limit of 5 mm
[5] NPO class dielectrics
[6] X7R, Deflection specification 0.5 mm on FR-4
[7] Flexion termination, 8 mm deflection

Sample Population

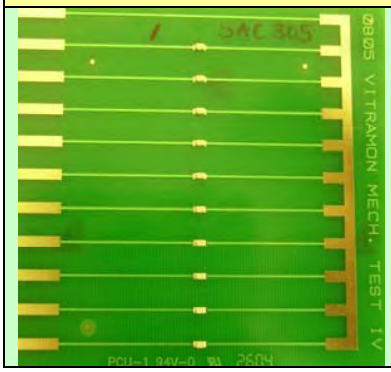
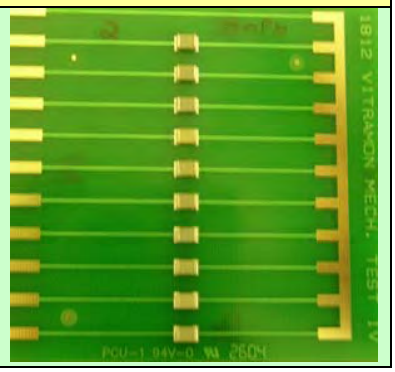
Two capacitor sizes were selected for testing, 1812 and 0805. Both capacitors have X7R type dielectric and are Pb-free parts, having terminations that are 100% tin with a nickel barrier. The nickel barrier had an average thickness of 3 µm and the tin had an average thickness of 7.5 µm before soldering. The capacitors were rated to a 1 mm board displacement specification. To prevent lead contamination the board finish selected for this study was electroless nickel - immersion gold (ENIG), a hot air solder leveled finish (HASL) is typically tin-lead solder and therefore was not selected. Test boards for the 1812 size capacitors were assembled using Sn3.0Ag0.5Cu and Sn63Pb37 solder. A summary of the sample types and quantities is shown in Table 2.

Table 2: Capacitors and solder compositions

Capacitor Type	Capacitance (µF)	Solder Composition	Samples Tested
0805 X7R	0.7	SnAgCu	100
1812 X7R	0.5	SnAgCu	200
1812 X7R	0.5	SnPb	100

The test coupons for the three types of assemblies are shown in Table 3. The boards were assembled by Universal Instruments Corporation and aside from the solder composition and reflow profile, have no other parameters varied.

Table 3: Capacitor test coupons

0805 SnAgCu	1812 SnAgCu	1812 SnPb
		

Experimental Procedure

The test coupons were tested by Vishay Vitramon using a custom three-point bend tester. The bend tester is based upon the industry standard but modified to accommodate a ten-capacitor test coupon. Capacitance measurements were taken at every 0.5 mm displacement and the boards were flexed to an end displacement of 8 mm.

Results

The results of the tests are shown in Table 4 through Table 6. Unlike the industry standard failure criteria of a 10% drop in capacitance, failure was defined as a 5% drop in capacitance. This change was instituted because the relatively stable behavior of MLCCs strongly suggests that any deviation in capacitance is due to the presence of a flex crack. An example graph of the results from one of the tests is shown in Figure 4. Even with this revised failure criteria all capacitors tested met their 1 mm displacement specification regardless of size and solder type.

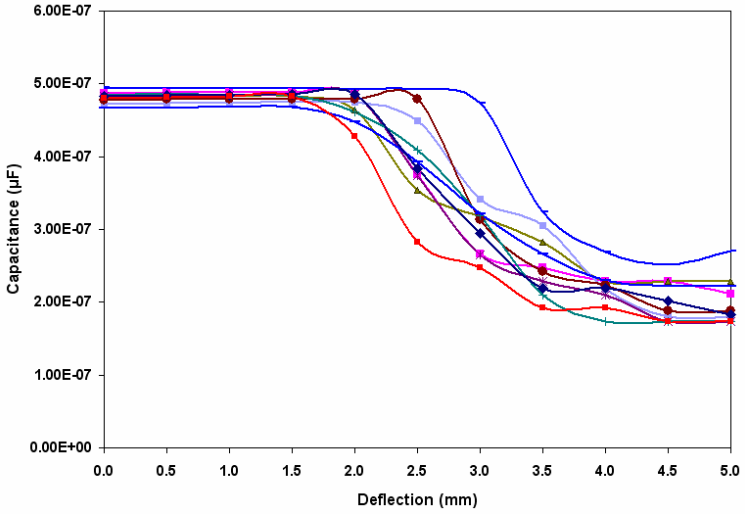


Figure 4: Example of test data, 1812 capacitor with PbSn

Table 4: Flexure failures of 1812 Capacitors with SnAgCu solder

Displacement	1.5	2	2.5	3	3.5	4	4.5	5	5.5	6	6.5	7	7.5	8
345(1)		2	3	1									1	2
346(2)		6	2			1								
347(3)		4	3											2
348(4)	3	2	1	1			1	1						
349(5)		2	3	2							2			
350(6)	1	7	1											
351(7)		4	3	2										
352(8)		2	1	3		1					2			
353(9)	1	4	2	2										
354(10)		3	6											
355(11)		4	4		1									
356(12)		5	4											
357(13)			4	1			2	1			1			
358(14)		2	2	2	1					1			1	
359(15)		8	1											
360(16)		4	2						1	2				
361(17)		5	3									1		
362(18)		3	1		5									
363(19)	1	6		2										
364(20)	1	3	3	2										

Table 5: Flexure failures of 1812 Capacitors with SnPb solder

Displacement	1.5	2	2.5	3	3.5	4	4.5	5	5.5	6	6.5	7	7.5	8
325(1)	1	5	3											
326(2)	4	3	1	1										
327(3)	3	6												
328(4)	2	4	1	2										
329(5)	6	2	1											
330(6)	2	6	1											
331(7)	1	4	4											
332(8)		5	4											
333(9)	1	6	2											
334(10)	1	7	1											

Table 6: Flexure failures of 0805 Capacitors with SnAgCu solder

Displacement	1.5	2	2.5	3	3.5	4	4.5	5	5.5	6	6.5	7	7.5	8
335(1)						2	2		1			1		
336(2)							2			1	1			
337(3)					1				1	1				
338(4)										1	1	1		
339(5)								1			1	1	1	
340(6)							1	1						
341(7)									1	1	1			1
342(8)													1	1
343(9)														
344(10)														

Comparing the data in Table 4 and Table 5, the 1812 size capacitors attached with SnAgCu appear to be more robust than those attached with SnPb solder. A plot of the full data set for the 1812 SnAgCu capacitors is shown in Figure 5.

Previous studies conducted by J. Bergenthal [22] showed that the failure data for capacitors typically exhibit a bimodal distribution. In his study, the author found it necessary to exclude failures above 50% in order to provide a

relevant statistical analysis. To avoid the same bimodal type distribution data above 90% failure (or 4.5 mm displacement) was excluded from the statistical analysis of the 1812 SnAgCu capacitors.

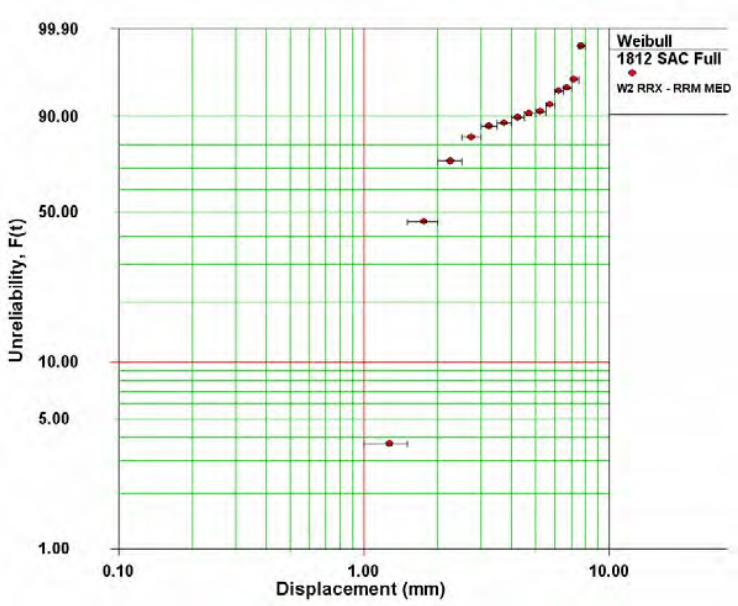


Figure 5: Failures of 1812 capacitors with SnAgCu solder

The additional robustness provided by using SnAgCu is clearly demonstrated by the 2-parameter Weibull plot shown in Figure 6. The characteristic displacement (63% failure point) of the SnAgCu 1812 and the SnPb 1812 was 2.36 mm, and 1.70 mm respectively.

The displacement necessary to induce 5% failure for 1812 capacitors attached with SnAgCu solder was 1.5 mm while those attached with SnPb was 0.85 mm.

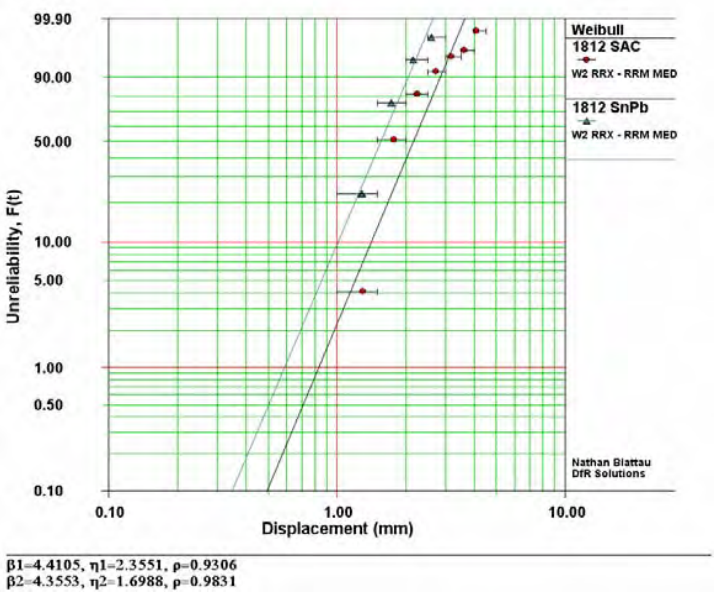


Figure 6: Weibull plot of 1812 capacitor failures

The data from the 0805 tests indicated that only 28 capacitors failed during the testing. The reason for this is discussed in the following section.

Failure Analysis

Selected capacitors from the assemblies were inspected and cross-sectioned to confirm the existence of flex cracks. Solder joint geometries were also compared between the two solder types to see if this contributed to the failure behavior.

Optical images of the failed capacitors are shown in Figure 7 through Figure 9. In these images, flex cracks can be easily identified.

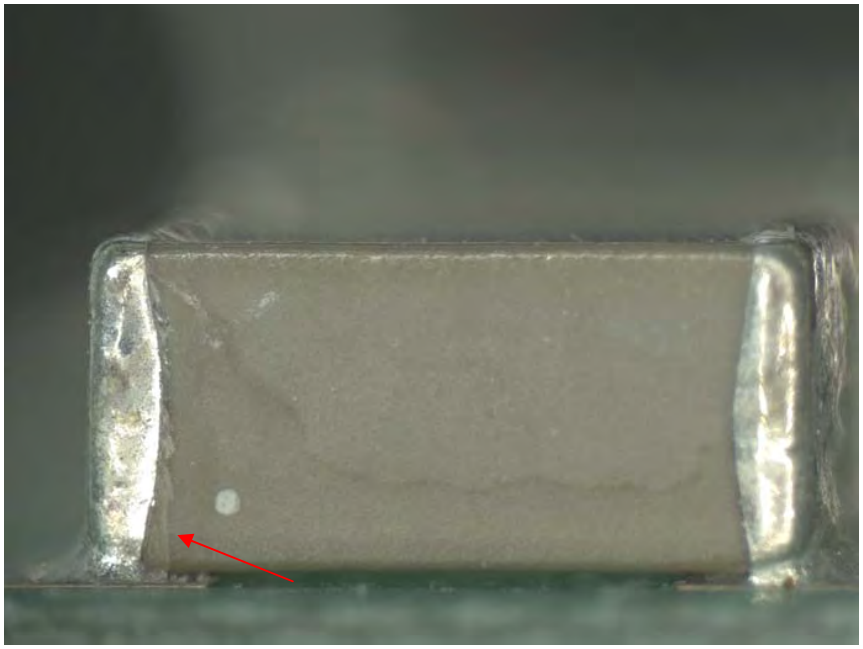


Figure 7: Optical micrograph of a 1812 capacitor attached with SnAgCu solder, flex cracks are identified with the red arrows

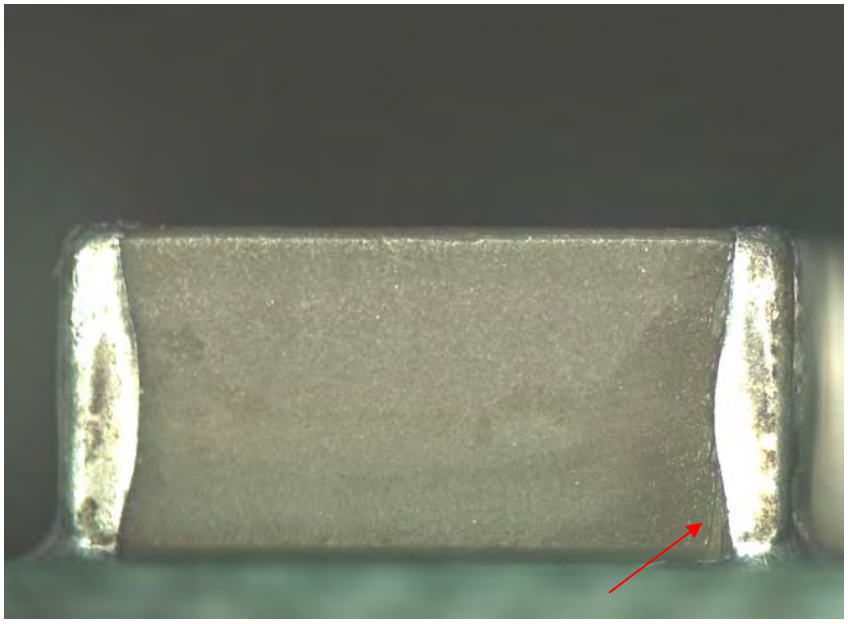


Figure 8: Optical micrograph of a 1812 capacitor attached with SnAgCu solder, flex cracks are identified with the red arrows

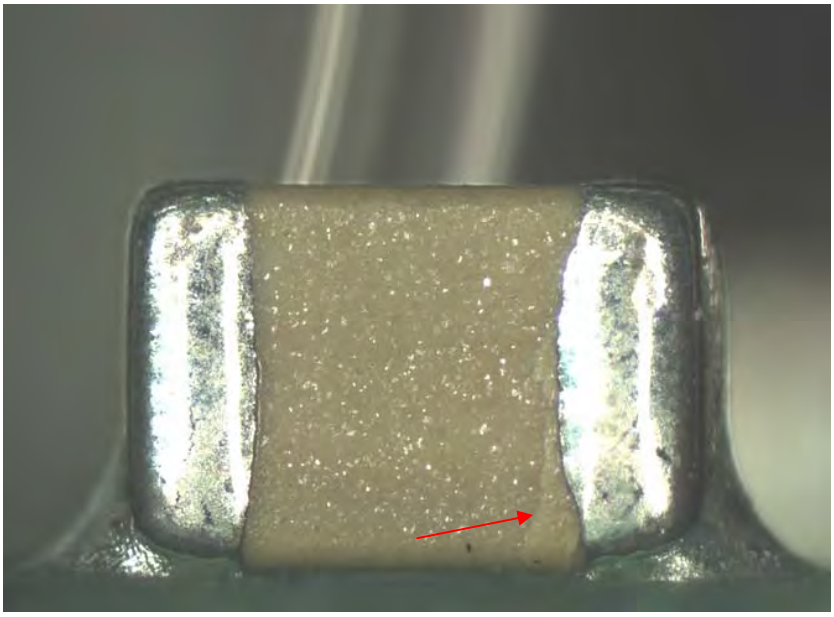


Figure 9: Optical micrograph of a 0805 capacitor attached with SnAgCu solder, flex cracks are identified with the red arrows

Failed 1812 capacitor cross-sections are shown in Figure 10 and Figure 11. The first one is that of a failed capacitor with SnAgCu solder and the second is one with SnPb solder. As shown by the figures, the fillet shape and height are similar. This indicates that the failure behavior is unlikely due to geometric parameters. The morphology of the cracks is typical of flexure fractures of ceramic capacitors.

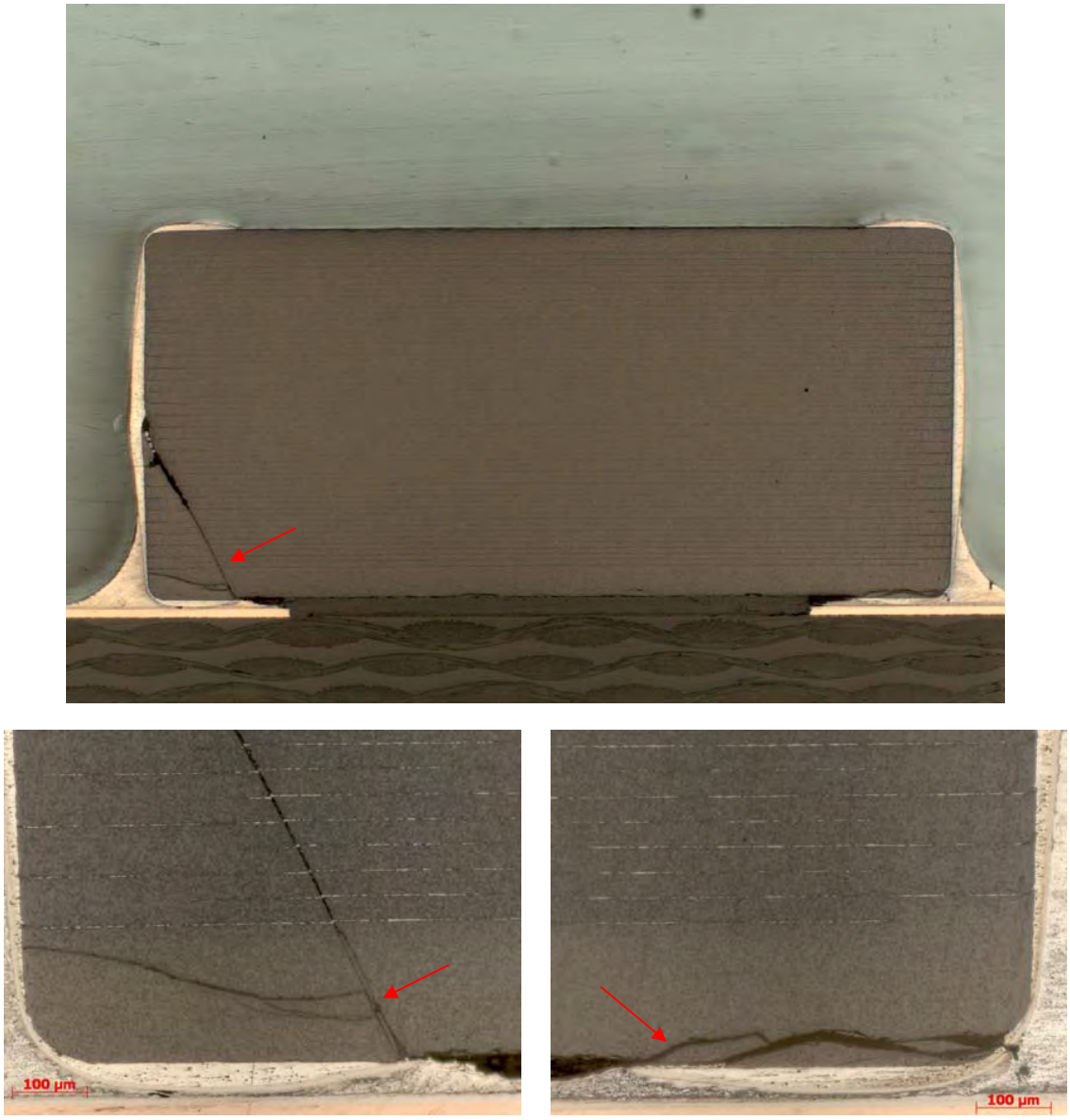


Figure 10: Optical micrograph of a cross-sectioned 1812 capacitor attached with SnAgCu solder, flex cracks are identified with the red arrows

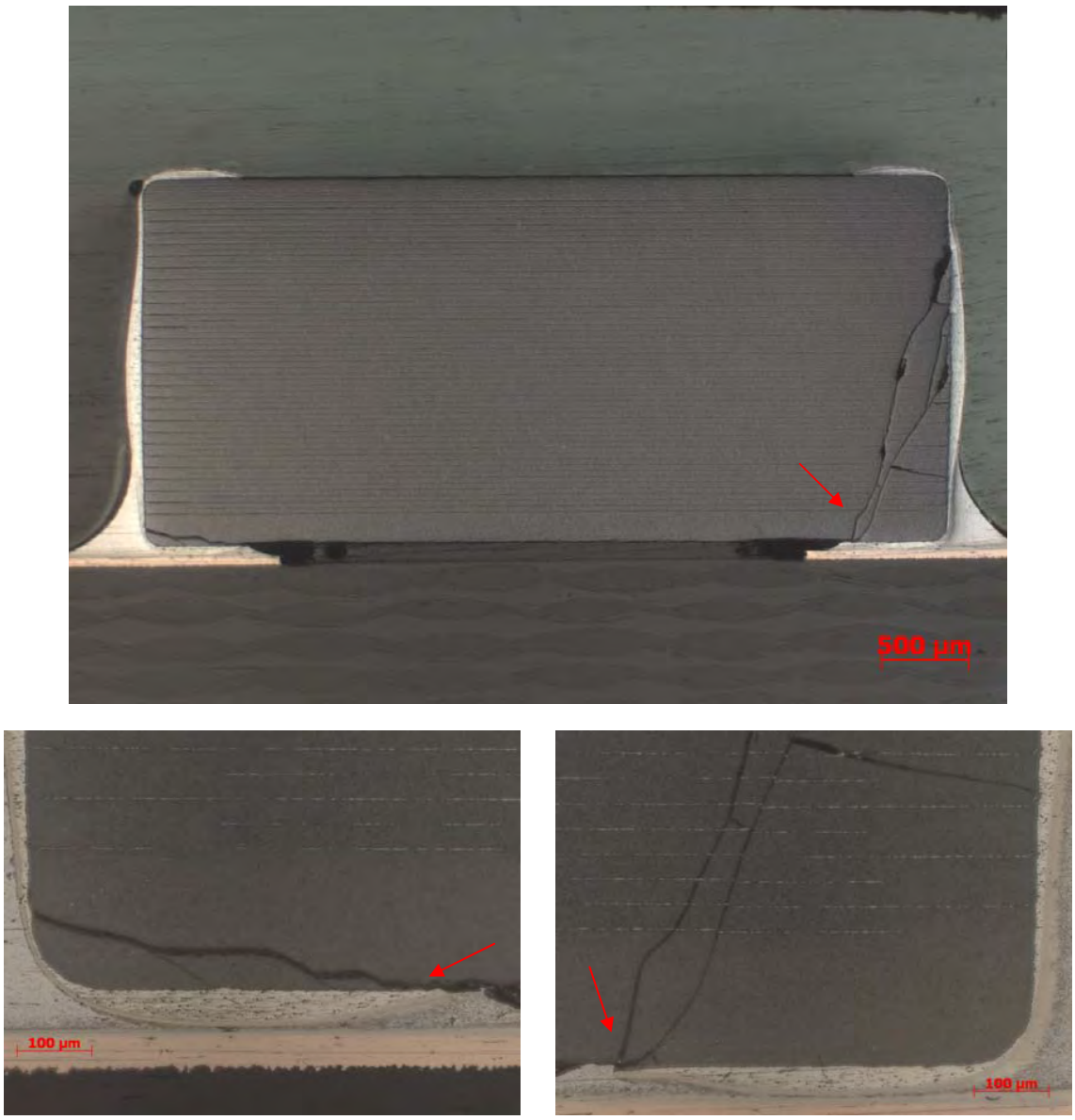


Figure 11: Optical micrograph of a cross-sectioned 1812 capacitor attached with SnPb solder, flex cracks are identified with the red arrows

A failed 0805 capacitor cross-section is shown in Figure 12. The 0805 capacitor shown in Figure 13, while cracked did not register as a failure during the testing. This is due to the orientation of the plates, which prevents the flex crack from fully separating from the terminations.

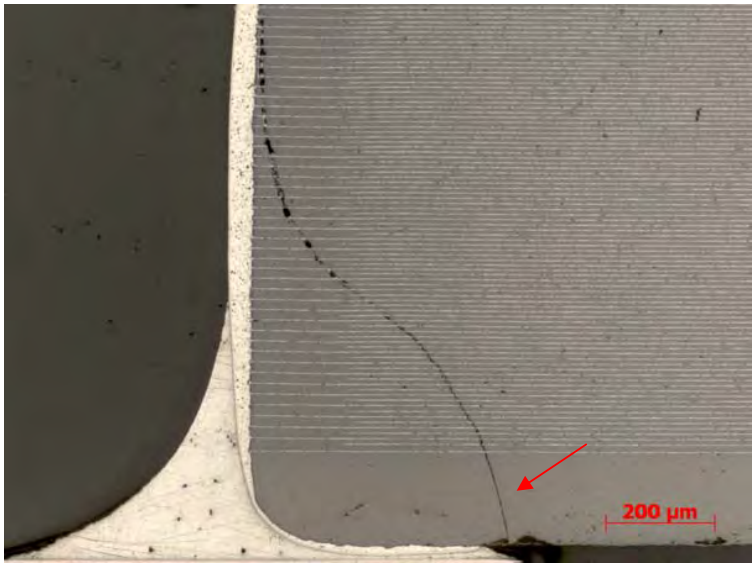


Figure 12: Optical micrograph of a cross-sectioned 0805 capacitor attached with SnAgCu solder, flex cracks are identified with the red arrows

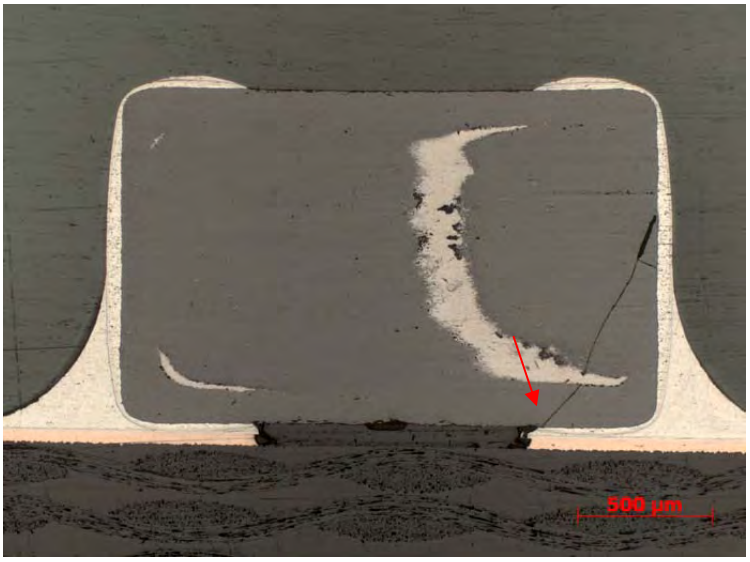


Figure 13: Optical micrograph of a cross-sectioned 0805 capacitor attached with SnAgCu solder, flex cracks are identified with the red arrows

Discussion

For a ceramic chip capacitor, failure due to printed wiring board bending usually manifests itself as a crack in the body of the capacitor, as shown in Figure 14. The crack may intersect the electrodes of the capacitor causing a decrease in capacitance or an increase in leakage current. Many times the failure is catastrophic with opposing electrodes shorting together and destroying the capacitor. The use of an open-mode ceramic capacitor can significantly decrease the probability of a catastrophic failure if a flex crack occurs.

The probability of the capacitor cracking is a function of the stress applied and the distribution of flaws present at the crack initiation site. This makes predicting the failure of ceramic probabilistic based upon the applied stress and the defects as first proposed by Weibull [20].

The results of this study indicate that the Pb-free assembly process will not have a negative impact on the reliability of the ceramic chip capacitors even though the solder is stiffer and the capacitor will be subjected to higher reflow temperatures. This contradicts some previous modeling studies.

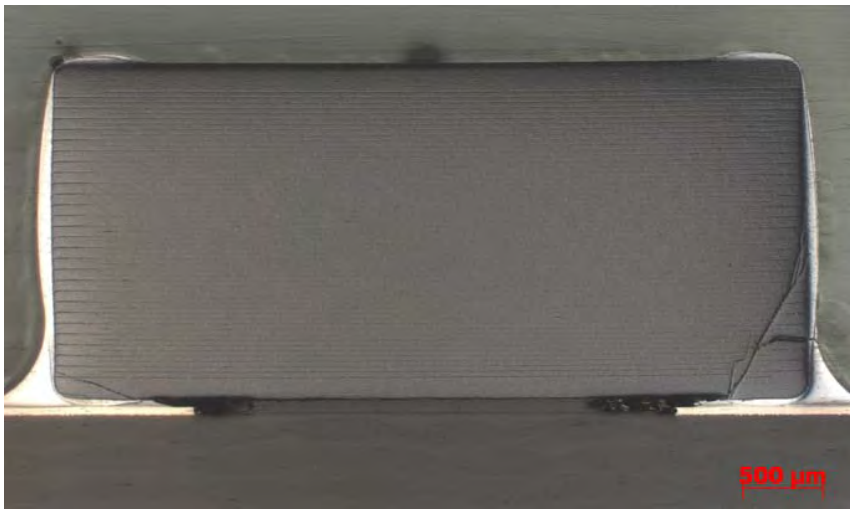


Figure 14: Flex cracking in a capacitor

Previous modeling using finite element analysis indicated that the stresses developed in the capacitor during bending would be higher due to the increased stiffness of the solder, which would lead to more flexural failures [0]. These models assumed that the solder was fully stress relaxed after the assembly process. However, this is not the case with Pb-free solder, as the creep rates for SnAgCu are much slower than that of SnPb. This places the capacitor under compression after assembly. This effectively increases the force required to fail the capacitor, much like the pre-stressed concrete beams used in bridges.

The test results and analytical equations were used to determine the relative magnitude of the residual compressive stresses. These stress and failure equations were utilized with increasing amounts of compressive stresses until the failure behavior matched that of the test results.

The analytical equations used to calculate the stress in the capacitor and have been extensively validated with finite element analysis. The failure equation then uses this stress to make reliability prediction using a model based upon the Weibull modulus and the width of the capacitor. The failure model differs from the test specification because it uses crack initiation as the failure criteria. This yields much more conservative estimates of the reliability of the capacitor.

The key is that any cracks in capacitors should be avoided, not just those that are so large as to cause a significance capacitance decrease. The existence of cracks, even small ones in the capacitor, could be a reliability concern in the

field, especially if the capacitor is subjected to vibration or thermal cycling. The analytical equations used to predict the stresses and the failures of ceramic capacitors have been incorporated into a web based calculator. The predictions of capacitor failures for 1 mm board deflection are shown in Figure 15 and Figure 16. The residual stress required to match the behavior of the test results for the SnAgCu was determined to be between 15 and 20 MPa. The 1812 SnAgCu test results verses the predictions are shown in Figure 17. The 1812 SnPb test results verse the analytical equation predictions are shown in Figure 18.

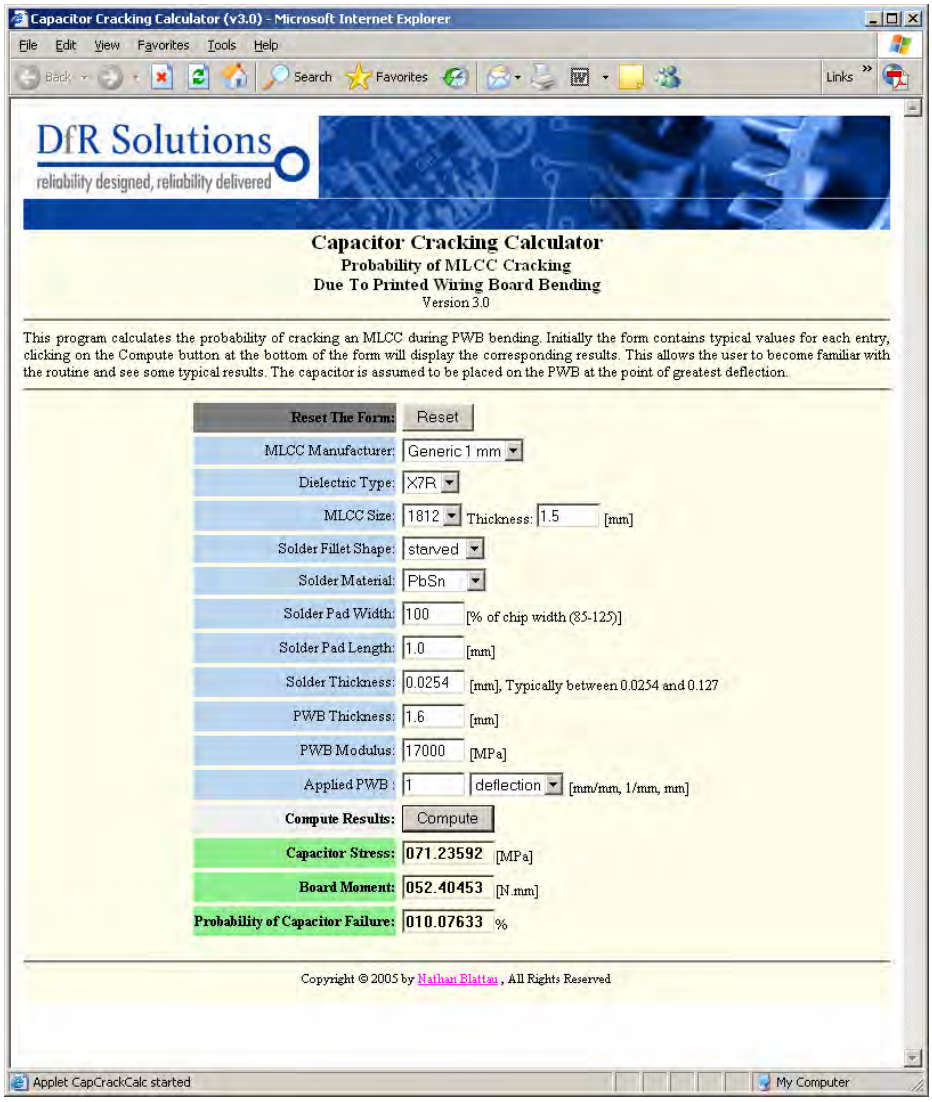


Figure 15: Capacitor calculator predictions with PbSn solder

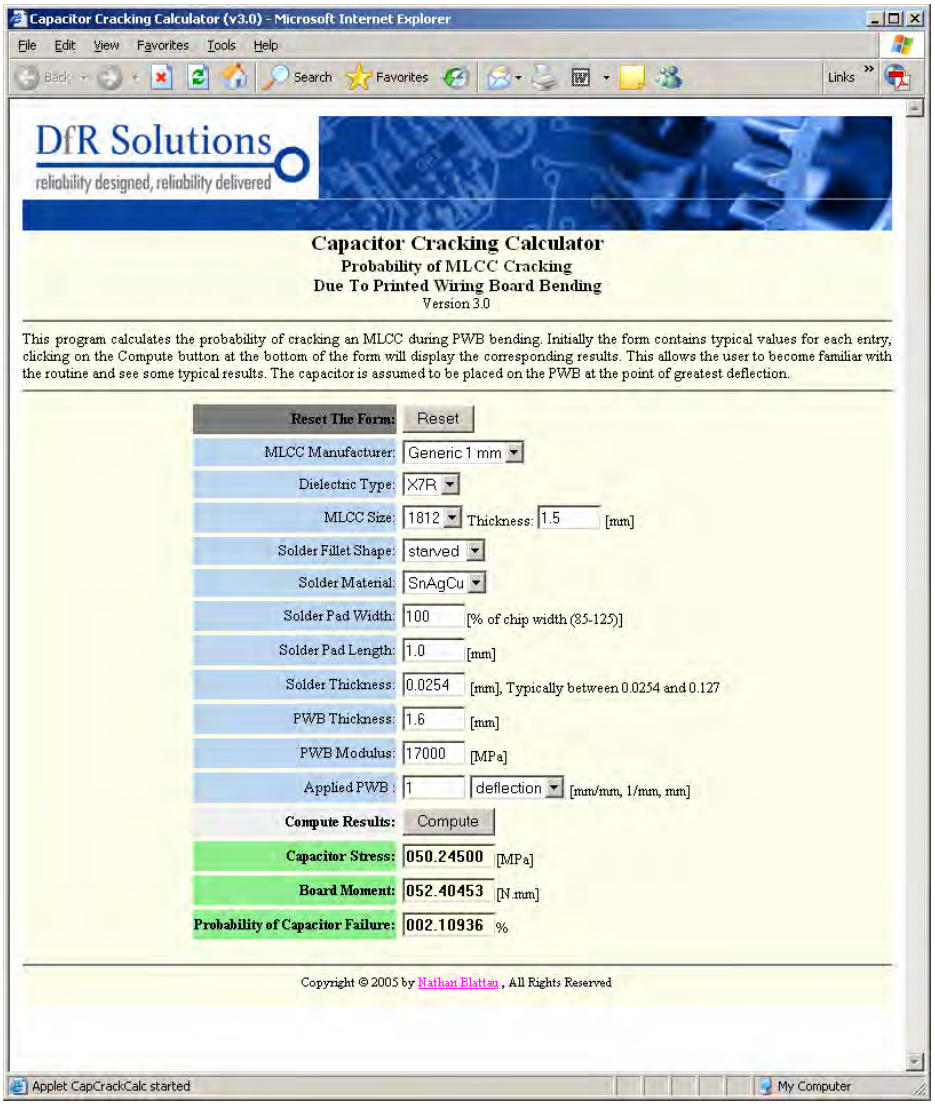


Figure 16: Capacitor calculator predictions with SnAgCu solder

SnAgCu solders can hold significantly higher residual stresses than PbSn [21]. The residual stresses reported were around 18 MPa after 8 hours at 21°C. The time between manufacturing and testing was much greater than 8 hours and further investigation is warranted. A possible additional explanation for this behavior is the amount of Ni_3Sn_4 intermetallics in the solder joint between the capacitor and the copper bond pad.

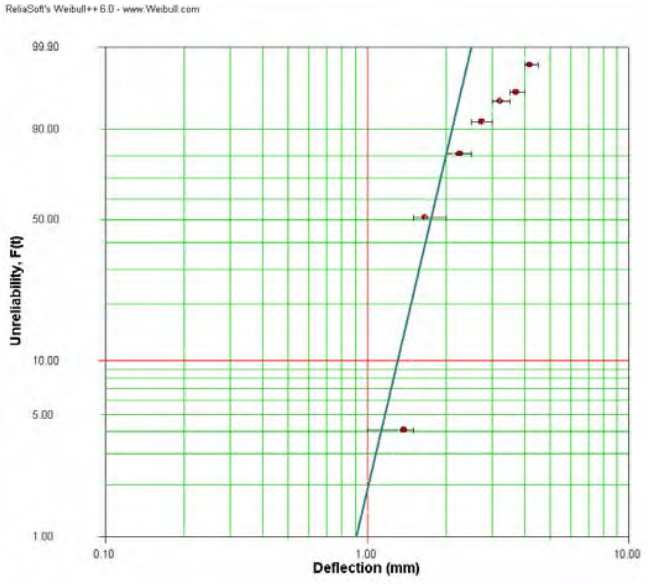


Figure 17: 1812 SnAgCu model predictions (blue line) verses test data

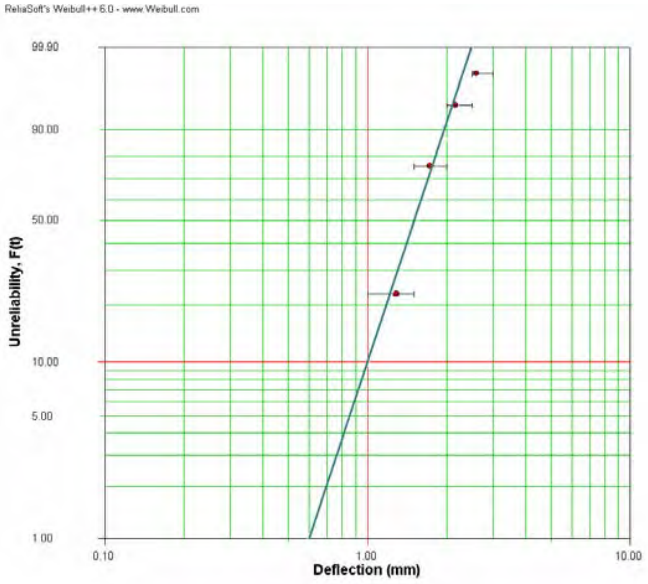


Figure 18: 1812 SnPb model predictions (blue line) verses test data

Conclusion

The extra robustness of ceramic capacitors soldered with SnAgCu is encouraging for the electronics industry. However, the role of residual stresses may raise additional concern with regards to components that may be subjected to residual tensile stresses after reflow. It also raises some concern over the reliability of reworked ceramic capacitors, since reworking may subject the capacitor to tensile residual stresses. The recommendation is that board assemblers not modify their board flexure limits with concern to ceramic capacitors when switching to SnAgCu.

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Exhibit J

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MLCC - Ceramic Chip Capacitors / Failure Mode Study

Potential Failure Causes, Accelerators, Behavior

Cause	Sources	Indications	Behavior	Remedy
Electrical Overstress; AC current or Pulse current	Poor design choice or inappropriate component selection	▪ Self heating (I^2ESR), ▪ Increased leakage current ▪ Discoloration over time ▪ In severe cases melting of solder alloy and component displacement,	Decreased IR (increased LC) typically leading to short or open condition	Alternate lower loss dielectric MLCC or film capacitor
Electrical Overstress; Voltage	Poor design choice or inappropriate component selection	▪ Micro-cracking within ceramic ▪ Dielectric puncture ▪ External flashover	Decreased IR (increased LC) typically leading to short or open condition	Higher voltage rated component or alternate capacitor type
Mechanical Stress	▪ Component test or tape operations ▪ Component placement ▪ Centering jaws ▪ Post reflow PCB Flexure or Shock ▪ PCB depanelization ▪ Impact damage to PCB	▪ Damage to MLCC body ▪ Cracking observed in ceramic	Immediate or latent IR failure; increasing LC or erratic LC leading to short	▪ Machine set-up, maintenance and operator training ▪ Placement pressure ▪ PCB Routing ▪ Flexible soft terminal MLCCs
Thermal Stress	▪ Hand Soldering ▪ PCB Rework ▪ Wave – flow soldering ▪ Forced cooling – quenching ▪ Subsequent PCB soldering processes	▪ Cracking observed in ceramic ▪ Leaching of terminal metallization	Immediate or latent IR failure; increasing LC or erratic LC leading to short	▪ Training and control ▪ Reduce heating – cooling rates
Intrinsic Defect	▪ Contamination in ceramic ▪ Improper pressing or sintering	▪ High porosity or voids in ceramic ▪ Knit-line voiding or cracking ▪ Firing cracks	▪ Immediate or latent LC; increasing LC leading to short ▪ Early HALT test failure	Material control and clean room particle control Pressing and Sintering controls
Ionic or metal conduction	PC residues, flux residues, water type, saponifier, assembly aids, sealers or coatings & external sources	Electrochemical migration (dendrite growth) or corrosion	Decreased IR (increased LC) over time and operating temp & RH	IQC, alternate materials, cleaning upgrade and alternate sealers

Exhibit K

Design Guidelines for Ceramic Capacitors Attached with SAC Solder

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DfR Solutions
College Park, Maryland

Abstract
Failure avoidance in ceramic chip capacitors has been accomplished through the development of design guidelines based on physics-of-failure principles. The transition to Pb-free solder, specifically SnAgCu, has resulted in both a change in processes and materials. This has required a review of current guidelines and modifications where appropriate. Failure mechanisms for ceramic capacitors are presented and the drivers for failure occurrence, mechanical, thermal, chemical, and electrical, are tabulated. The influence of Pb-free solder on each driver is then analyzed, with the subsequent output changes in current design guidelines with justification when appropriate.

Introduction
Avoiding failures in ceramic chip capacitors (shown in), also known as multilayer ceramic capacitors (MLCCs), is strongly driven by the ability of the designer, both electrical and mechanical, to follow guidelines based on an understanding on how surface mount ceramic capacitors fail. The transition to Pb-free has required a change in materials and processes, potentially requiring a change or modification in these guidelines. To understand how and when these guidelines must be modified, a diligent listing of potential failure mechanism must be provided. That listing is displayed below:

- Visible Intrinsic Defects
  - Firing Cracks
  - Knit Lines / Delamination
  - Voiding
- Thermal
  - Thermal shock
- Mechanical
  - Placement/handling cracking
  - Flex cracking
- Chemical
  - Dendritic growth
- Electrical
  - Resonance
  - Dielectric breakdown

Intrinsic Defects
Intrinsic defects are anomalies introduced by the component manufacturer that limit the expected lifetime of the ceramic capacitor. In MLCCs, there three basic types of visible internal defects in MLC capacitors that impair reliability: knit lines / delamination, voiding, and firing cracks. Knit lines / delamination, displayed in Figure 2 are cracks that run parallel to the electrodes and are caused by issues with the pressing or sintering processes, which include insufficient binding strength, trapping of air or foreign material, and internal sublimation of burnout material. Voids are large pockets of air between electrodes and are caused by contamination, both organic and inorganic, in the ceramic powder or a non-optimized burnout process. An example is displayed in Figure 3. Firing cracks often originate at an electrode edge, propagate perpendicular to the electrodes, and typically initiate during cooling after densification (see Figure 4).

Since these defects are introduced before the Pb-free soldering process and component manufacturers transitioned to Pb-free plating several years ago, the preponderance and severity of these defects is not expected to change.

Thermal Shock
Thermal shock cracks occur due to the inability of the ceramic capacitor to temporarily relieve stresses during transient conditions. The most common signature of thermal shock is a 45-degree microcrack emanating from the termination of the end cap (see Figure 5). While the initiation of a thermal shock crack will not induce failure, if the capacitor is exposed to varying levels of voltage or temperature, the crack will eventually growth, cutting off the electrodes from the termination and

inducing an electrical open (see Figure 6). The susceptibility of MLCCs to thermal shock is dependent upon the MLCC architecture, the dielectric material, the solder pad geometry, and the parameters of the soldering process. For example, MLCCs with plated terminations wet about a hundred times faster compared to MLCCs with Pd/Ag or Ag terminations. This results in situations where Ni-plated parts can experience 100% failure compared to standard thick film terminations of Ag and Pd/Ag would have no failures when subjected to the thermal shock testing using wave solder reflow technique [4]. In another study,1206 X7R MLCCs made from ceramic A with a fracture toughness of (K_{Ic}) value of 1.3 MPa·$m^{1/2}$ and from ceramic B with (K_{Ic}) value of 0.9 MPa.$m^{1/2}$ were compared using wave solder reflow [5]. The results in the last column clearly show, the susceptibility to thermal shock changes ranging from no failures in the chips with the higher K_{Ic} to about a 75% failure rate in those with the lower K_{Ic}. This shows that ceramic materials with higher K_{Ic} are desirable.

For reflow, no design changes are necessarily required. All existing sizes and designs of MLCC's are reflowable with Pb-free solder and board bond pad dimensions do not need to be altered. One Pb-free manufacturing concern is the tendency for contract assemblers and industry organizations to promote reflow profiles with higher ramp rates to ensure sufficient throughput (see Figure 7). To prevent thermal shock, ceramic capacitor manufacturers typically provide the following recommended ramp rates

- Room temperature to preheat (max. 2-3ºC/sec.)
- Preheat to maximum temperature (max. 4-5ºC/sec.)
- Cooling (max. 2-3ºC/sec.)

However, as seen in Figure 7, some part manufacturers and assemblers have higher cooling rates, upwards of 5 to 6C/second, to increase the throughput lost from the longer times for preheat and ramp to maximum temperature. In addition, the assembly should be less than 60ºC before being subjected to any cleaning processes such as an aqueous wash.

Design changes should be considered for the more severe reflow processes of wave soldering and hand soldering. Thermal shock is typically prevented during wave soldering by limiting the case size to a maximum of 1210. Due to the more severe conditions of Pb-free wave soldering, designers should consider reducing this maximum case size to 1206 or 0805. Previous experimentation has also shown that thicker capacitors and wider bond pads increase the likelihood of cracking. Therefore, designers should pay attention to these parameters and consider placing limitations, such as no ceramic capacitors thicker than 1.25 mm, or modifying existing specifications, such as reducing bond pad dimensions to below manufacturer's recommendations. As with solder reflow, the parameters of the wave solder should also be maintained. Preheat temperatures should be increased to maintain the same change in temperature upon contact with the solder wave.

Designs that intentionally require hand soldering of MLCCs should be eliminated with the transition to Pb-free and any rework should be performed with a hot air knife instead of a solder iron as the increase in tip temperature from 300ºC to 350ºC greatly increases the chance of thermal shock during touch up.

Of special importance is understanding when MLCC failures are not due to thermal shock. Transient thermal analyses performed by Scott[1] and Panchwagh[2] found that the maximum tensile stress during thermal shock events occurs on the board-side of the capacitor, near the termination of the end cap. These model results were validated through the cross-sectioning and inspection of ceramic capacitors believed to have been exposed to thermal shock conditions. Maxwell[3] has also stated that thermal shock cracks occur at or near the ceramic/termination interface (as seen in Figure 5).

There have been some discussions in the literature about the shifting of the crack location away from the termination/ceramic interface. Dematos[4] found that when microdelaminations are present along the electrode/dielectric interface, the location of maximum stress shifts away from the termination to the defect sites. This modeling result was correlated during thermal shock testing, where they found that occurrence of thermal shock failure was strongly correlated with defect population. Those capacitors with fewer and less significant defects were less likely to experience thermal shock cracking. A similar

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finding was reported by Anderson[5]. Capacitors were subjected to best-case and worst-case wave solder profiles, with cooling rates of 0.5C/sec and 15C/sec respectively. No correlation was observed between failure rate and cooling rates. Acoustic examination of all failed capacitors identified internal delamination parallel to the electrodes as the dominant crack morphology (shown in Figure 9).

Placement/Handling Cracking

Placement and handling cracks typically occur during component placement. Since the parameters of this activity are not expected to change with the introduction of Pb-free solder, no changes in design guidelines are necessary.

Flex Cracking

Flex cracking in ceramic capacitors occurs when there is excessive flexure of the printed circuit board. An example of a flex crack is displayed in Figure 10. Once the flex crack initiates, it tends to propagate at a 45 degree angle from the edge of the termination to the dielectric/termination interface. The creation of a crack path between adjacent electrodes creates the opportunity for internal dendritic growth, shown in Figure 11, resulting in increased leakage current and eventually an electrical short.

Flexure of the printed wiring board can occur throughout the product lifecycle, including depaneling, connector insertion, screw or standoff attachment, in-circuit testing and customer use. Flex cracking of ceramic capacitors is a major driver for field returns due to the ubiquitous nature of ceramic capacitors on today's low voltage designs and high density designs that place ceramic capacitors near potential flex points.

Transitioning to Pb-free was initially a major concern for flex cracking due to the higher modulus and higher yield strength of the SnAgCu compared to SnPb. This stiffer material would theoretically provide a greater transfer of stress for a given displacement (see Figure 12). Initial calculations suggested that the potential failure rate from flex cracking could increase by three orders of magnitude. However, subsequent testing did not prove this to be the case. Experimental studies by DfR Solutions and Kemet demonstrated that ceramic capacitors assembled with Pb-free solders consistently showed similar or improved robustness to flex cracking compared to capacitors assembled with SnPb solder (displayed in Figure 13).

Further investigations identified two potential rationales for the deviation from prediction. First, the reduced wetting of SnAgCu solder creates a greater standoff, imparting additional compliance to the interconnect. Second, the greater stiffness of the SnAgCu solder joint allows the ceramic capacitor to retain a much higher compressive stress after reflow. Any stress arising from board flexure has to effectively overcome this residual stress to induce flex cracking.

While the transition has to Pb-free has not resulted in any changes to existing design rules, mechanical designers should be aware of current design rules to avoid flex cracking. These consist of

- The board bond pad width should be equal to or less than the capacitor width (eliminate side fillets)
- Maintain a minimum 30 – 60 mil distance from potential flex points (V-score edges, breakoff tabs, separable connectors, attachments)
- If this distance can not be maintained, rotate the capacitor to be perpendicular to the bend radius
- If the capacitor can not be rotated, consider the use of capacitors with flexible terminations (AVX, Syfer)

Dendritic Growth

Dendritic growth, also known as electrochemical migration, is the migration of metallic filaments under bias through an aqueous solution. It typically requires the presence condensed moisture or contaminants. The presence of condensed moisture can be eliminated through case design or the use of conformal coating and is independent of SnPb or SnAgCu. The presence of contaminants, however, can be very dependent upon the solder material and flux composition being used. Pb-free solders and board platings are much less solderable than SnPb and therefore require fluxes with higher activity to ensure sufficient wettability.

[5] T. Anderson, "Study of high rate temperature change effects on cracks and DCL failures on MLCs," 16th CARTS Symposium Proceedings, p. 177-180, 1996

For smaller MLCCs with smaller distances between opposing terminations, care should be taken to avoid using excessive levels of solder paste or flux. If cleaning is desired and a batch process will be used, MLCCs should be placed in areas where they will not be blocked by larger components.

Resonance

The barium titanate based dielectric material used in MLCCs is piezoelectric in nature, which results in elastic expansion and contraction with changes in the applied electric field. Typically this displacement is on a microscale and has minimal influence on capacitor behavior. However, at certain resonant frequencies, the capacitor can begin to vibrate along its length. This vibration, if at sufficient magnitude, can induce scattered internal microcracking, resulting in a decrease in capacitance and an increase in leakage current.

The frequencies of concern are typically in the hundreds of kHz to tens of MHz (see Figure 15). The frequency of concern decreases with increasing case size and increasing capacitance. It is currently unknown if exposure to Pb-free reflow will change this behavior as most characterization of resonance behavior is performed on loose parts.

Dielectric Breakdown

The primary mechanism that induces wearout in MLCCs is dielectric breakdown, also known as punch-through. Punch-through is an iterative process, where areas of current leakage experience self-heating, which deteriorates the insulation resistance of the dielectric, which in turn increases the current leakage. Eventually, a conductive path is formed between adjacent electrodes. To assess the risk of this mechanism, Mogilevsky and Shin developed a time to failure equation

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n \exp\frac{E_a}{K_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)$$

where V is voltage, n is a voltage exponent (1.5 – 7), T is temperature (K), E_a is an activation energy (1.3 to 1.8) and K_B is Boltzman's constant (8.62 x 10^{-5} eV/K). Using previous MLCC designs and highly accelerated testing, this formula predicted that time to 1% failure would not occur for several decades. More recent MLCC designs that incorporate sub-2 micron dielectric thickness have displayed much shorter times to failure. Using data from published literature, time to 1% failure can occur in less than 10 years even under relatively benign use environments (50% derating, 45ºC ambient temperatures).

Most test data on this behavior, as with resonance, has been acquired from loose capacitors that have not been subjected to reflow. Possible changes in this behavior with the application of higher reflow temperatures required for SnAgCu has not been assessed. To ensure sufficient lifetime, designers may wish to consider additional characterization for those capacitors on the board with capacitance/volume (C/V) ratios of approximately 2 – 10 uF/mm^3.

Conclusion

As ceramic capacitors are the most common component in today's modern electronics, designers should be made aware of appropriate design rules and potential modifications necessary with the introduction of Pb-free solder to ensure sufficient reliability.

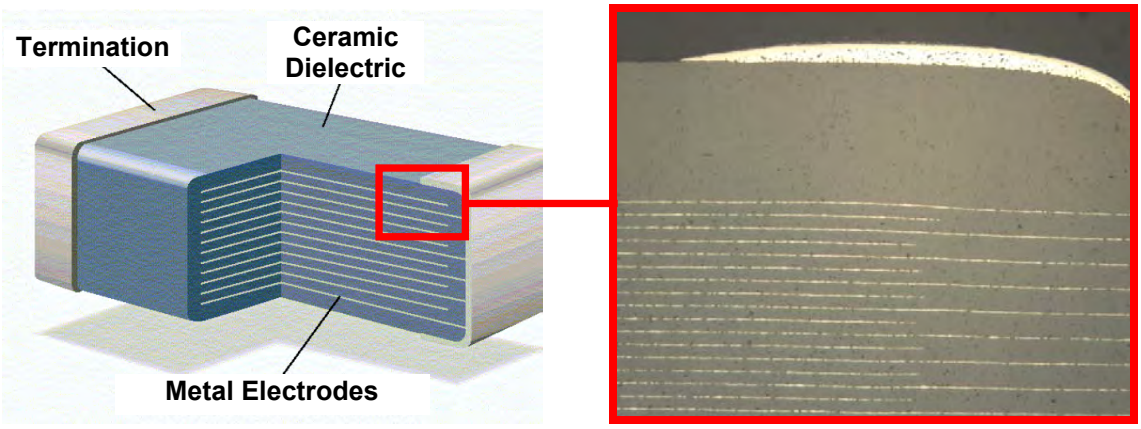


Figure 1: Cross-section of a multilayer ceramic chip capacitor (MLCC)

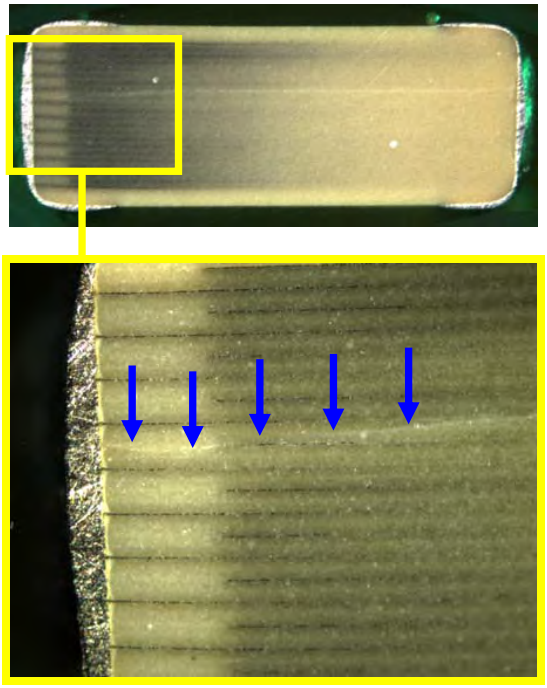


Figure 2: Optical micrograph of a knit line crack in a MLCC

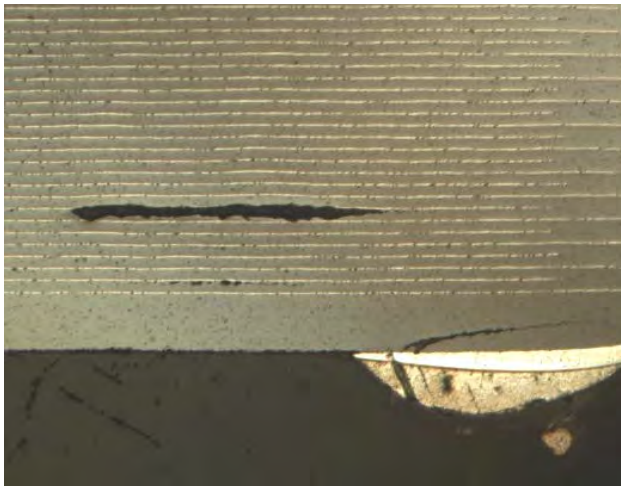


Figure 3: Optical micrograph of voiding in a MLCC

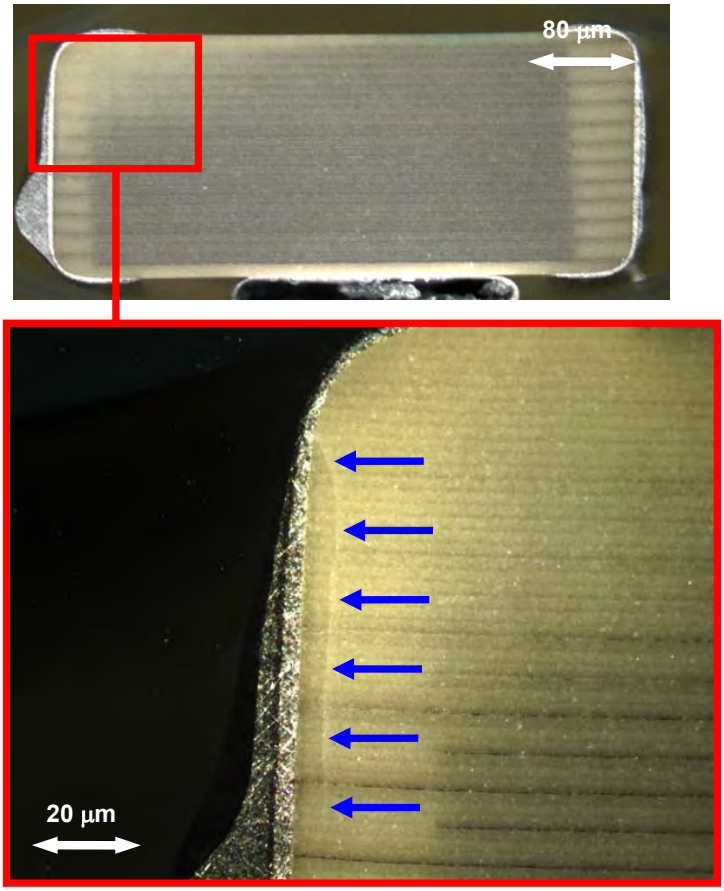


Figure 4: Optical micrograph of a firing crack in a MLCC

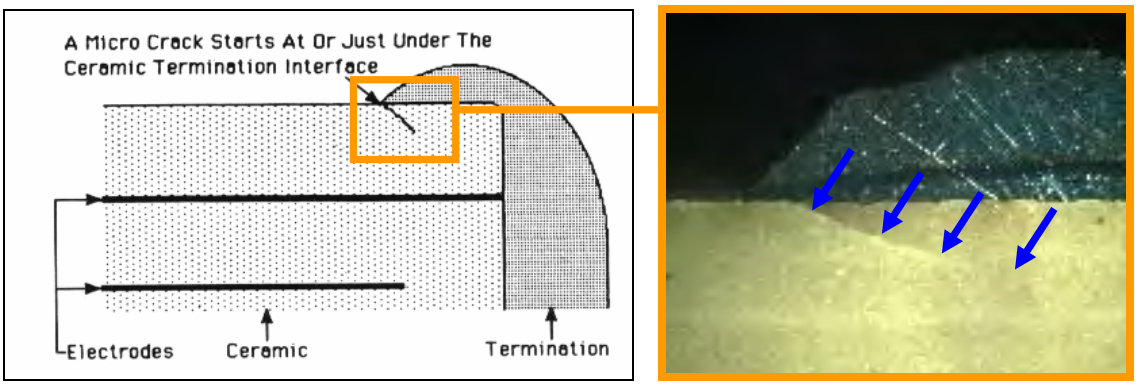


Figure 5: Thermal shock crack in a MLCC (schematic courtesy of J. Maxwell, AVX)

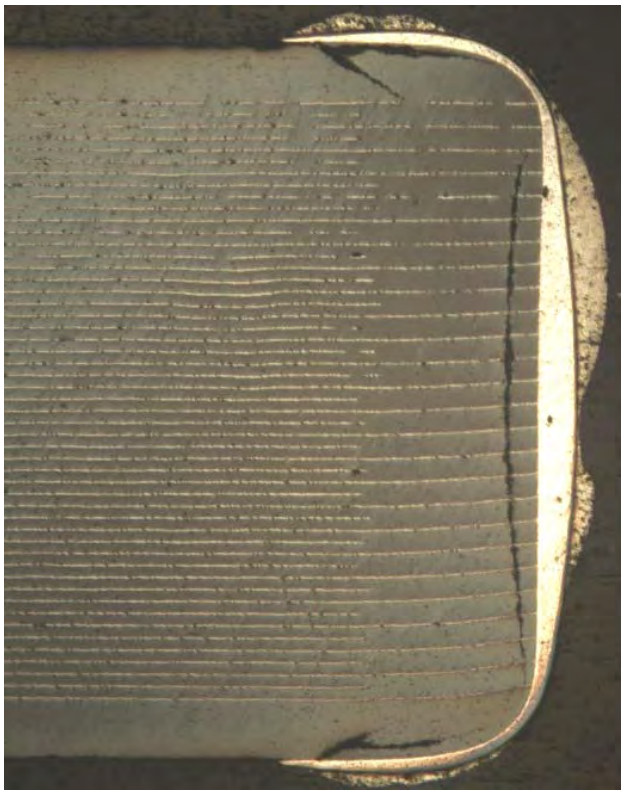


Figure 6: Optical micrograph of a thermal shock crack in a MLCC that has propagated through the metal electrodes

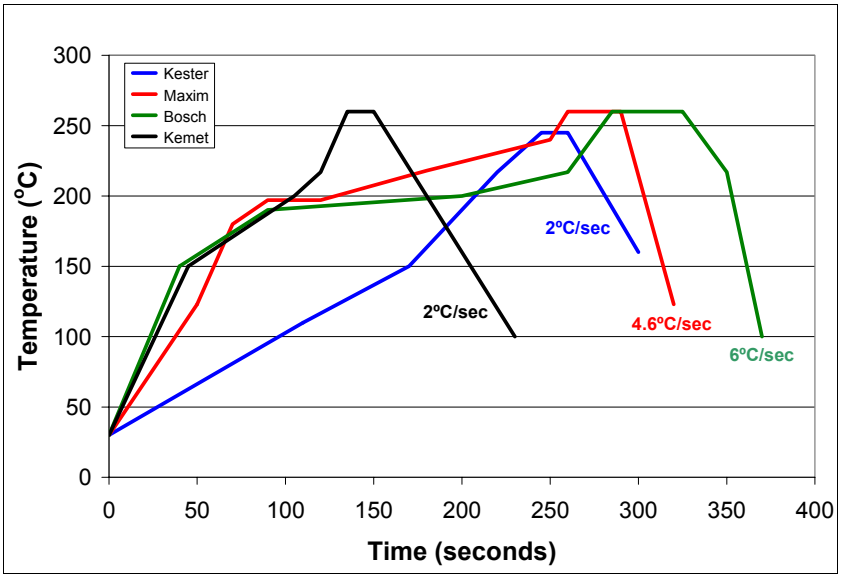
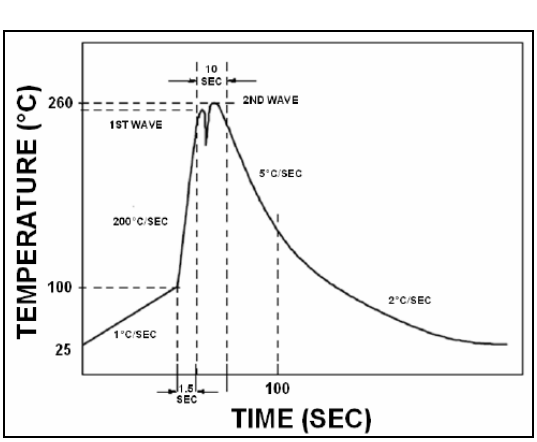


Figure 7: Pb-free reflow profiles from solder supplier, part manufacturer, assembler, and capacitor manufacturer



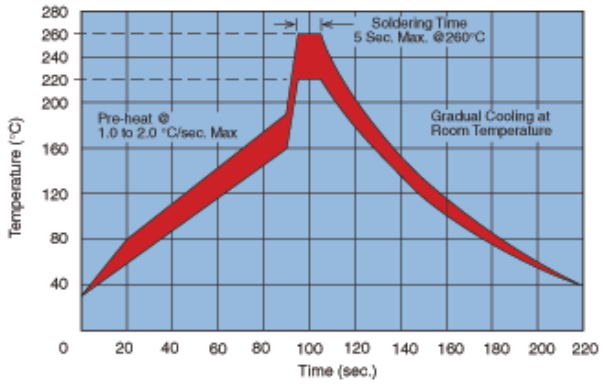


Figure 4: Wave Solder Profile for MLCCs

Figure 8: Wave solder profiles for SnPb and SnAgCu solder

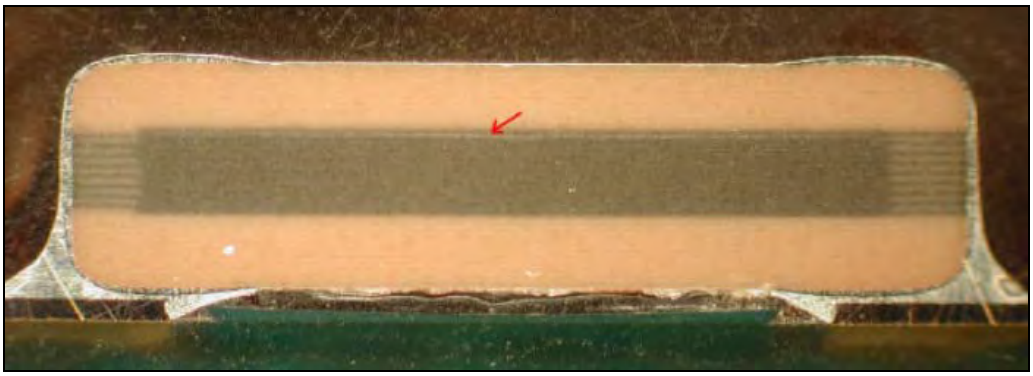


Figure 9: Cracking in a MLCC initially misdiagnosed as a thermal shock crack

Figure 10: Optical micrograph of flex crack in MLCC

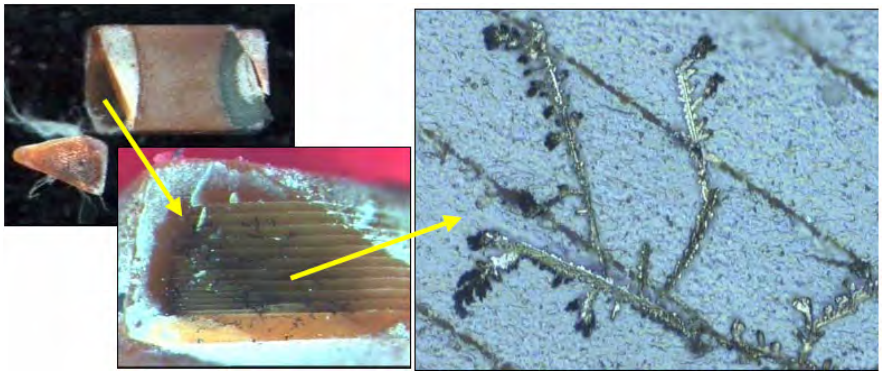


Figure 11: Optical micrograph of dendritic growth in flex crack (courtesy of G. Vogel, Siemens)

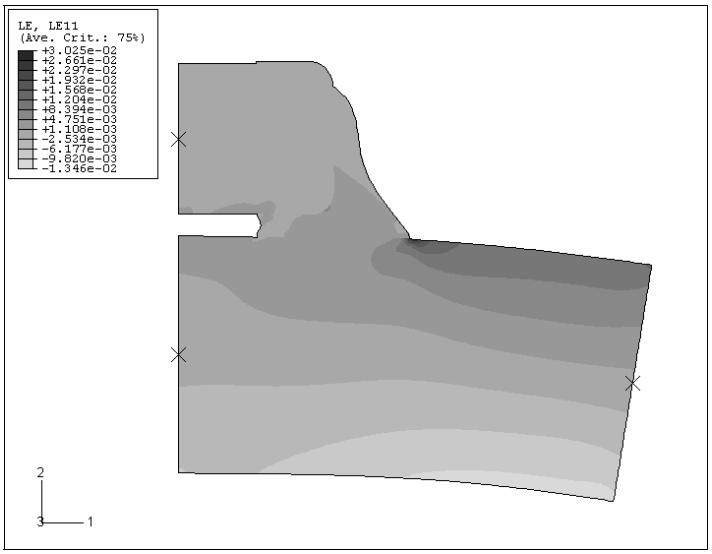


Figure 12: Transfer of stress into the capacitor during board flexure

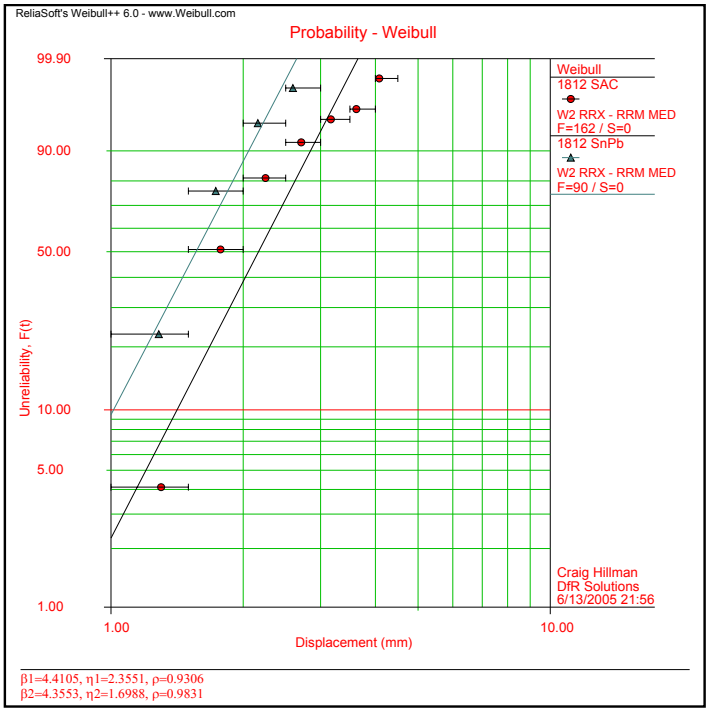


Figure 13: Failure as a function of displacement for 1812 capacitors assembled with SnPb and SnAgCu solder

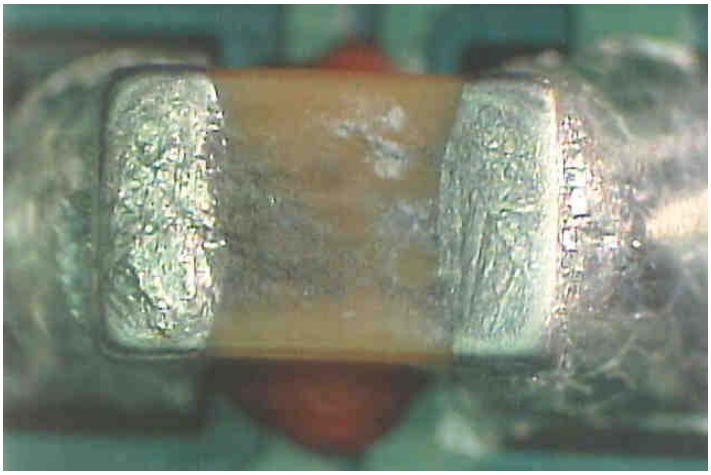


Figure 14: Optical micrograph of dendritic growth on the surface of a MLCC

Case Size		Resonance Frequency
English	Metric	
3025	7563	250 - 750 kHz
2220	5750	300 - 900 kHz
1812	4532	400 - 1200 kHz
1210	3225	600 - 1200 kHz
1206	3216	600 - 1600 kHz
0805	2012	900 - 1800 kHz
0603	1608	N/A
0402	1005	N/A

Figure 15: Resonance frequencies for various case sizes of MLCCs (courtesy of Nippon Chemi-con, CAT No. E10021)

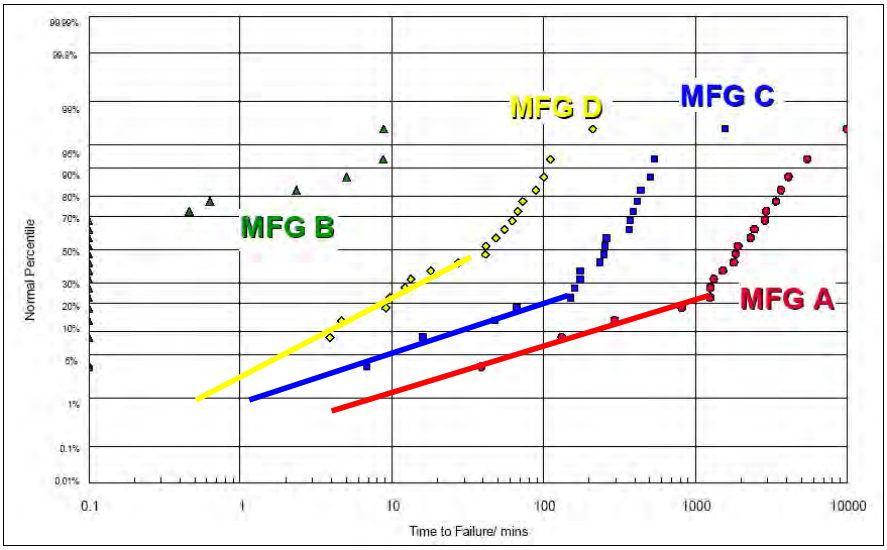


Figure 16: Time to failure behavior of MLCCs with sub-2 micron dielectric (courtesy of Randall, et. al., CARTS 2003)

Exhibit L

Ceramic Capacitor Failures on the Rise

Since their introduction in the late 1990s, surface mount multilayer ceramic capacitors (MLCCs) gained rapid acceptance by the electronics industry and today are among the most common components on a circuit card assembly. The reliability of an MLCC can be extremely high, with an expected operating lifetime of decades. Problems occur when defects are introduced, either during manufacture or the assembly processes. Due to the large amount of energy stored by capacitors, internal shorts resulting from defects can cause explosions and dramatic temperature increases, which not only destroy the MLCC, and any evidence of root cause, but can also damage surrounding components, the printed board, adjacent circuit card assemblies, and may even lead to fires. Over the last eighteen months, CALCE laboratory services have assisted a number of companies in finding MLCC root cause failures.

Failure Analysis. When MLCC failure is catastrophic, the failure investigation starts by examining the MLCCs adjacent to the failure site and those in the same failure area on similar circuit card assemblies.

The first step in the failure analysis (FA) process is to confirm that electrochemical migration (ECM) underneath the capacitor was not the root-cause of failure. If samples of non-catastrophic failures exist, ECM can be investigated by washing the area around and underneath the capacitor and examining the solution for high levels of chlorides or bromides. Once ECM has been ruled out, the MLCCs are examined using scanning acoustic microscopy (SAM), with a 110 MHz transducer. This is very effective in locating voids, delaminations, and horizontal cracks, although it is not as successful in identifying flex cracks, thermal shock cracks, or other types of vertical cracks causing MLCC failures.

Flex cracks and extensive thermal shock cracks can be identified through methanol testing. Due to its polar nature, methanol is an electrically conductive liquid. Capillary action and methanol's low viscosity allow methanol to become quickly absorbed by any surface cracks present in the capacitor. If the crack has propagated across opposing electrodes, the absorbed methanol will temporarily form a conductive film between the two electrodes, creating an observable rise in current leakage.

All suspect capacitors are eventually subjected to cross-sectioning. This is because some defects, such as small thermal shock cracks and vertical cracks caused by poor handling, are otherwise hard to detect. Cross-sectioning can be performed on capacitors attached to the board or on single capacitors. Sectioning of the board can create additional defects in the capacitor and confuse the FA process, so care must be taken. Air can also become trapped between the capacitor and the board during the potting process leading to damage during grinding and greater difficulty in getting an optimum image.

MLCCs can be removed from the board, preferably with a 150^{o}C preheat and with hot air, to prevent the removal itself from introducing a defect and confusing the FA process. Next, the MLCCs are labeled so that top/bottom and left/right directions are identified, and then mounted in room-temperature cure epoxy for ease of handling and to minimize damage during cross-sectioning. For maximum efficiency and minimum damage, MLCCs are ground using 600-, 800-, and 1200-grit silicon carbide paper and periodically checked for anomalies. Beginning with a fine grit greatly reduces the amount of grinding-induced porosity that can mask intrinsic porosity, small cracks, and delaminations.

Thorough examination is conducted on at least four different internal planes--preferably where the end cap is ground off, at the start of the internal electrodes, and two other cross-sections. Optical examination is performed at magnifications between 50x and 200x. For maximum contrast, images are taken in bright and dark field modes. A particular emphasis is placed at the termination of the end caps, since this is where flex cracks and thermal shock cracks initiate.

Identification of Root Cause. Failures of MLCCs are often accelerated by defects introduced during the capacitor manufacturing process or by excessive stresses experienced at various stages of assembly. During manufacture, failure accelerators can arise from different root-causes. Contamination in the ceramic powder can lead to excessive porosity or voids. A void bridging electrodes can become a short leakage current path and a latent electrical defect. Non-optimized pressing or sintering can also lead to excessive porosity and voids, and to delamination (knit line cracks). Delaminations and single-layer voids do not cause failures directly but are very sensitive to mechanical stress that can rupture inter-electrode dielectric layers, which then become the latent leakage paths. Delamination can also extend from an electrode end to the opposite termination, again causing a latent leakage path. Rapid cooling can cause firing cracks, which often originate at an electrode edge, but not always. A firing-crack propagation path is perpendicular to the electrodes.

The danger of forming cracks, even microcracks, during the placement step is that the high temperatures during soldering will often induce internal cracks to grow across several electrodes. Cracking due to excessive placement force by a vacuum tweezer primarily consists of surface damage on the top of the MLCC with the potential for microcracking on the board side of the component.

Centering jaws can cause cracking due to excessive force or worn bits leading to stress concentrations. Both root-causes leave distinct crack signatures.

MLCCs are sensitive to thermal shock due to their construction and to differences in the CTEs of the materials used. Thermal shock cracks can occur during solder reflow, wave solder, cleaning and rework. Thermal shock cracks generally initiate on the bottom-side of the capacitor, at the termination of the end cap. They often propagate at a 45-degree angle and tend to range in size from 10 to 500 microns.

Capacitor failures that occur during connector insertion, depaneling, or bolting are often due to excessive flexure. Excessive flexure can cause flex cracks, which can emanate from the termination of the end cap and propagate at a 45-degree angle. This is similar behavior to a thermal shock crack. The primary difference is the size; flex cracks tend to be larger, propagating through the ceramic until the crack reaches the end cap.

For more information on ceramic capacitor failure identification and corrective actions, contact Dr. Craig Hillman of CALCE Laboratory Services at 301-405-4316 or email *chillman@calce.umd.edu*.

Exhibit M

NASA Electronic Parts and Packaging (NEPP) Program

NEPP Task:

Effect of Manual-Soldering-Induced Stresses on Ceramic Capacitors

(Part I)

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Content.

1. Introduction.

Cracking in ceramic capacitors is an old problem; it appeared in the 1970s when the first surface mount technology (SMT) chip capacitors were introduced to the market and began to be employed in NASA applications [1, 2]. According to J. Maxwell [3], one of the most experienced specialists in manufacturing of ceramic capacitors, this problem will continue to be with us in the foreseeable future. Two main factors contribute to the problem: brittleness of the ceramic materials, and thermal and mechanical stresses associated with the SMT assembly process. Both factors are intrinsic to chip ceramic capacitors and explain the persistence of the problem. Based on the analysis by the Center for Advanced Life Cycle Engineering (CALCE) of over 150 electronic product failures over a 4-year period, capacitors are responsible for a larger proportion of failures than any other component [4].

1.1. Factors affecting cracking.

Factors affecting the propensity of multilayer ceramic capacitors (MLCCs) to cracking can be divided into two categories: internal and external. Internal factors are related to the property of materials used, presence of internal defects, and the size of capacitors. Fracture toughness characterized by the critical-stress intensity factor K1C, thermal diffusivity, and Young's modulus are among the most important characteristics of ceramic materials affecting the thermal shock behavior of MLCCs [5]. Generally, the mechanical stability of capacitors and fracture toughness increase in a row: NPO > X7R > Z5U, Y5V [4, 6]. Multiple studies and manufacturers' guidelines indicate that the larger the size of capacitor, the greater the probability of cracking either due to soldering stresses or to handling after assembly [4, 5, 7-10].

External factors are related mostly to the thermal and mechanical stresses caused by the soldering process and post-soldering handling of the board. However, cracking in ceramic capacitors can occur at any step during the lifespan of the parts, starting from manufacturing and continuing through assembly and applications [11-14]. Note that the compressive strength of ceramic materials significantly exceeds their tensile strength, by five to 13 times according to the data presented in [15]. Considering that coefficients of thermal expansion (CTEs) of printed wiring boards (PWBs) are larger than those of ceramic capacitors, soldering of MLCCs onto polymer boards results in development of compressive stresses. Typically, these stresses do not cause fractures in the parts; however, bending of the board might cause tensile stresses sufficient for cracking.

A brief description of different causes of cracking is given below. In some cases the appearance of the crack can indicate its origin [11].

I Manufacturing.

- I.1 Rapid cooling of the laminates can cause so-called firing cracks that typically propagate perpendicular to the plane at the terminals.
- I.2 Insufficient binding strength and/or the presence of foreign materials might result in knit-line cracks that typically extend parallel to the electrodes.
- I.3 Oxidation of palladium electrodes in air is accompanied with volume expansion and might cause cracks and delaminations [16]. It is assumed that thermal cracks might initiate at internal flaws such as voids and delaminations, and the larger the delamination the greater the probability of thermal shock failures.

II Assembly.

II.1 Pick-and-place machines can damage parts by excessive stresses created by centering jaws or vacuum picks.

II.2 Thermal shock cracks are due to a sharp temperature increase during soldering; they originate at the surface and propagate to the interior at angles of ~45^{o}. Thermal shock stresses might form large, visible U-shaped cracks on the surface of capacitors.

II.3 Thermal shock cracks might also occur when liquid cleaners are applied to a board that has not sufficiently cooled after soldering reflow. To prevent this type of cracking the boards should be cooled slowly, preferably by natural cooling, or at a rate not exceeding 2 ^{o}C to 3 ^{o}C/sec., to temperatures below 60 ^{o}C.

II.4 Tensile stresses and cracking might develop in MLCCs after soldering them onto alumina boards. This is due to the differences in CTEs between the ceramic material and substrate, with the latter having lower CTEs. These stresses are responsible for many observed failures in ceramic chip capacitors mounted on alumina substrates [1].

III Board-level handling.

Due to the lack of stress relief in mounted chip capacitors, deformation and flexing of the PWB might create significant tensile stresses resulting in so-called flex cracking. These cracks mostly originate at the bottom surface near the edge of the termination margin and propagate inside at angles close to 45^{o} (or 60^{o} to 65^{o} per [9]). Typical sources of the flex cracking are de-paneling, test probing, screw or standoff attachments, handling during visual examinations, insertion of connectors, board-to-board vertical connections, etc.

IV Application.

IV.1 Deformation of the board caused by temperature cycling, vibration, or mechanical shocks that occur during applications might cause flexing of the board sufficient for cracking of MLCCs. Multiple guidelines for design and board layout have been developed to reduce the probability of this type of failure [3].

IV.2 Due to electrostriction in ceramic materials, voltage cycling might create mechanical stresses that would further develop preexisting microcracks, resulting in failure. This mechanism might be especially important for high-voltage ceramic capacitors [17, 18].

Board flexing and soldering-induced thermal shocks are considered major reasons of cracking in MLCCs. A breakdown of about 40 different mechanical failures of capacitors that were analyzed by CALCE shows that 25% were caused by flex cracking, 23% by thermal shock cracking, and 34% were due to manufacturing defects [4, 14].

Various designs of MLCCs have been suggested by manufacturers to decrease the probability of flex cracking [9, 19]. Most of these solutions simply involve removing the deleterious effects caused by flex cracking even though the parts are still cracking:

- Flexible termination. The application of relatively soft and/or tear-away termination layers made of conductive polymers reduces the stress in ceramic and restricts flex cracks within a safe zone away from the body of the MLCC.
- Fail open design. In this design, the end margins are widened, so if a crack occurs, it does not cross electrodes with opposite polarity, and thus prevents short-circuit failures.

- Floating electrodes. This design creates two separate capacitors in series within an individual case size, so the probability of shorting cracks is reduced substantially.
- Clip-on lead frame. Attachment of J-shaped leads mechanically decouples the MLCC from the PWB and allows for stress relief. A layer of solder resist at the bottom of the MLCC prevents solder from wicking and causing short circuits.

Because industry is now using lead-free solders, concerns regarding thermal shock cracking have increased substantially. Also, the lead-free solders are stiffer and have a higher yield stress, so changing eutectic solder to either Sn3.5Ag or Sn4.0Ag0.5Cu might lead to increased flex cracking of the capacitors [20]. However, experiments showed that the probability of flex cracking in capacitors assembled with high-temperature Pb-free solders is lesser compared to those assembled with Sn/Pb eutectic solder [4]. Cooling of assemblies after high-temperature soldering places capacitors under greater compressive stresses, and respectively more bending is necessary to create tensile stresses and cracks in the part.

Standardized test methods have been developed to assess the susceptibility of MLCCs to cracking due to board flexing and to thermal shocks. The first is performed using so-called flex-testing that is typically performed per EIAJ Specification RC-3402, Multilayer Ceramic Capacitors (Chip-type). According to these tests, the part is soldered onto a PWB made with standard material and of a standard size, and is deflected with the component face-down to the required level, while its capacitance is monitored. A decrease in capacitance below the acceptable limit (typically 0.2% or 2% [9]) is used to characterize the robustness of a capacitor to board flexing. By creating sufficiently large deflection of the board, cracking can be achieved in most cases. This makes this testing convenient and effective for analysis of factors affecting failures in capacitors related to board handling. Note that similar testing is also standardized by the automotive industry (AEC Q-200, Stress Test Qualification for Passive Components) to assure reliability of MLCCs after assembly, and it would be reasonable to include a similar standard in MIL-PRF-123 also.

The thermal shock test or so-called solder-dip testing is described in MIL-STD-202. According to this method that in MIL-PRF-123 is referred to as the resistance-to-soldering-heat test, MLCCs are immersed two times into molten solder at a temperature of +230 °C for 5 seconds. However, most capacitors are passing the standard solder-dip test without failures, and likely for this reason many manufacturers are using more stringent test conditions by increasing the temperature during this test to 260 °C. Even higher temperatures might be needed to characterize the lead-free capacitors.

A simplified model of thermal-shock-induced stresses in MLCCs predicts that the stress increases proportionally to the elastic modulus, the coefficient of thermal expansion of ceramic, and the square of the thickness of the part [5]. Based on this model, thermal shock behavior of capacitors can be dramatically improved by utilizing thinner geometries of capacitors. However, experiments showed that the thermal shock resistance is inversely proportional to the total area of the ceramic surface, rather than to its thickness [8]. This was explained by the effect of preexisting flaws on the surface of ceramic capacitors that dominate the crack initiation process, and are therefore primarily responsible for the thermal shock resistance of MLCCs.

1.2. Effect of cracks on performance of capacitors.

The presence of cracks might not affect capacitance and dissipation factors of the part substantially [9, 10], but can cause avalanche breakdown failures [21] or increase leakage currents [10, 11, 22]. The majority of field failures of MLCCs are caused by low insulation resistance that is often due to cracks. In low-impedance applications, a decrease in resistance might cause catastrophic failures. Although cracks in ceramic capacitors might not lead to immediate failures, they create defects that would cause degradation with time (hours to months) resulting eventually in field failures. In this regard, microcracks generated during assembly can be considered as a "time bomb" [11] that causes increased leakage currents, opens, or intermittent contacts as cracks propagate with time during application.

Cracks in ceramic capacitors might cause life test failures. Acceleration testing of various lots of commercial ceramic capacitors was performed in [23]. Some correlation between the life test results and the presence of delaminations in MLCCs was observed.

Increased leakage currents in MLCCs having cracks might be due to various mechanisms. A virgin surface of the crack might have increased electron conductivity due to the presence of a high concentration of surface traps; however, this conductivity is not great enough to cause failures and likely will not increase with time. A substantial increase in leakage current occurs when a conductive media fills the crack. This is possible either by moisture condensation, when the part is exposed to humid environments, and/or by formation of metal dendrites, when dry or wet electromigration of electrode metal occurs in the crack. In both cases the presence of ionic contaminations substantially enhances the degradation process.

Moisture can penetrate inside the capacitor along a crack if it is initiated from the surface, or along the micropores. It is also possible that moisture can enter the part though the porous termination and electrode interfaces [24]. Note that due to a capillary effect, as well as polarity and affinity of ceramics to water molecules, the condensation can develop with time even at relatively low-humidity environments.

Silver was initially used as a metal of choice for electrodes in MLCCs. However, this metal has a high propensity for electromigration in humid and even in dry environments. In the absence of moisture, silver can migrate through glasses at relatively high temperatures (more than 150 ^{o}C) by a field-induced diffusion mechanism [25]. This behavior is likely unique for silver, but in the presence of moisture a variety of metals, including gold, palladium, and nickel, are susceptible to migration and might form shorting dendrites. It is assumed that the replacement of silver with Pd/Ag alloys or nickel in contemporary capacitors somewhat inhibited electromigration. However, electromigration in humid environments is still possible, and for this reason biased high-humidity/high-temperature testing is still considered an effective technique to inspect capacitors for dielectric cracks [21].

Excessive degradation of the parts with microcracks in humid environments might be related to so-called low-voltage failures in ceramic capacitors [2, 26]. Although the occurrence of this type of failure is substantially decreased, and most manufacturers believe that their parts are now impervious to this effect [27], there are some indications that this effect is still present [21]. Recent results on biased MLCCs at 85 ^{o}C/85% RH reported by CALCE showed that intermittent failures do happen, but they are more likely to occur at higher voltages [28]. More study is necessary to assess the probability of failures of contemporary ceramic capacitors in humid environments and to understand the effect of electrode materials and voltage acceleration factors.

1.3. Techniques for revealing cracks.

According to Tarr [13], the cracks might be visible in less than 2% of affected parts, so only a small minority can be identified as potential failures before use. This requires development of more effective methods to reveal cracks in MLCCs. A variety of techniques have been suggested for screening of capacitors during mass production, during post-soldering examinations, or for investigation purposes. A brief description of these techniques is given below.

- Visual inspection. This is the most simple and inexpensive test, but unfortunately it is not very effective due to the insidious character of most cracks in MLCCs. Nevertheless, thorough optical examination is necessary as a screening procedure. The effectiveness of this test can be increased substantially by application of the vicinal examination technique [29, 30].
- X-ray radiography. Radiography has a low success rate in revealing cracks [13, 31]. X-ray microcomputer tomography might be more effective, but it is not suitable for large-scale screening [32]. Also, termination layers with high absorption (e.g., solder) may shield the minor changes in X-ray intensity resulting from the crack.
- Acoustic microscopy. This technique was proven to be effective in some cases, and scanning laser acoustic microscopy (SLAM) testing was implemented as a screen for incoming capacitors [12]. Acoustic microscopy can successfully reveal large voids and delaminations, but it is much less successful on cracks, especially those propagating at 45^{o} or more [31]. Also, ultrasonic systems have difficulties penetrating through the multiple layers of the device under the curved surface of the termination. Most of the defects detected by acoustic microscopy have been caused by delaminations or cracks that occur before attachment, and in the center section of the capacitor.
- Laser ultrasonic and interferometric measurement. According to this technique, a pulsed infrared laser excites a specimen into vibration through laser-generated ultrasound, and the vibration displacement is measured using an interferometer [31]. Although this method is able to detect cracks, further testing and refinements are required to account for the process-induced manufacturing variations in different part sizes.
- Electrical measurements. Measurements of insulation resistance (IR) are considered more sensitive to the presence of cracks compared to measurements of capacitance and the dissipation factor. According to Tarr [13], IR measurements can reveal approximately 60% of damaged capacitors, and this technique is considered as having a medium success rate [31]. The effectiveness of capacitance measurements can be increased substantially if the part is mechanically loaded during the test. This was achieved in [32] by exploiting the thermal mismatch between the capacitor and the organic board. During these measurements, the part was heated up so that the capacitor experienced a tensile force, thus causing opening of the existing cracks. The crack openings manifested themselves as a capacitance decrease in discrete steps over temperature. However, ceramic capacitors have pronounced temperature dependence of capacitance that might mask the presence of cracks and overlay the decay in capacitance caused by cracking.
- Environmental testing. The presence of microcracks can be detected if a conductive liquid fills the crack, thus substantially increasing leakage current in the capacitor. Water is

obviously a suitable liquid, and direct quenching of preheated capacitors in ice water has been successfully used to reveal cracks in MLCCs [8]. A standard 85 ^{o}C/85% RH test has been widely used to evaluate reliability of ceramic capacitors. However, conductivity of water might be not sufficiently high, and likely for this reason no failures in parts after solder-dip test were revealed by this technique in [5], whereas 1 hour of boiling the parts in 1.3 N NaCl solution resulted in IR failures.

- Methanol test. Methanol is a conductive, low-viscosity liquid with a perfect capillary action for allowing penetration into tiny cracks in ceramics. This test has been extensively used for revealing cracks in MLCCs. However, several other factors may also lower the insulation resistance, thus obscuring the effect of cracks. These factors include contaminated cleaning solvents or large amounts of dissolved flux residue [13].

1.4. Manual soldering.

Volumes of literature have been written over the years about cracks in ceramic capacitors, mechanisms of their formation, and factors affecting the probability of their occurrence. Based on the studies performed, substantial progress in the quality of materials and manufacturing processes has been made. This, together with development of detailed application guidelines, resulted in a significant decrease in cracking-related failures, and allowed for application of MLCCs in high-reliability systems including space instruments. Still, failures related to cracking in capacitors after assembly onto PWBs do occur, and further analysis is necessary. Several cases of crack-related failures in large ceramic capacitors were observed recently by the aerospace community [29]. In some cases, cracking was observed after manual soldering of MLCCs that is often used during assembly of cards for space projects.

Manual soldering of ceramic capacitors is known to have a high risk of causing cracks in the parts. The major reason for this is that hand-soldering does not allow for proper control over the process, and is subject to variability of individual operators and mistakes. Of particular concern are the variability of temperature, the possibility of overheating, touching the part with the soldering iron tip, and an excessive amount of applied solder [7, 33, 34]. The risk of cracking during hand-soldering is increasing with the size of capacitors, so J. Maxwell [3] plainly stated to "never use soldering irons" for parts with a case size of more than 1210.

All manufacturers are warning against manual soldering of MLCCs and provide detailed guidelines to reduce the risk of cracking in case rework or hand-soldering has to be used. These guidelines can be summarized as follows:

1. Direct contact by a soldering iron tip often causes thermal cracks, so the tip should be applied to the contact pad only. Use a soldering tip no greater than 0.120" [3.0 mm] in diameter (Vishay), and apply the transmission of heat through the soldering material so as not to allow the tip to make contact.
2. Preheat the chip capacitor to + 150 °C minimum. Use a hot plate or hot air flow for preheating.
3. Use the lowest tip temperature setting possible and a maximum soldering time of 5 seconds. The tip temperature should be less than 300 °C (280 °C maximum per Vishay guidelines, and 285 °C per ATC [33]). Note that according to MIL-STD-202 TM 210, condition A regarding use of a soldering iron, the testing should be performed at a much higher temperature of the soldering iron, 350 °C ±10 °C.

4. The wattage of the soldering iron should not exceed 30 W.
5. If lands are different, solder the smaller land first, and remove the tip quickly when the fillet is formed [33]. The fillet should have a concave profile and be at least 25% of the chip height.
6. Excess solder might cause mechanical stresses on components, thereby diminishing reliability. All thermal shock studies supported a moderate amount of solder, with excessive solder leading to a greater susceptibility to fault [7].
7. When removal of a chip capacitor is necessary, a hot air pencil is the preferred tool.
8. After soldering, allow the chip to cool at room ambient conditions. Using forced cool air or refrigerated air for expediting the cooling process is not recommended and can create thermal shock cracks.

1.5. Purpose of work.

Unfortunately, manual soldering has to be used sometimes for unique space assemblies or during rework. To estimate the risk associated with manual soldering, it is important to obtain a better understanding of the mechanism of soldering-induced cracking and factors affecting the probability of its occurrence. An obvious reason for the risk associated with manual soldering is poor reproducibility of the process and the possibility of operator mistakes. Still, it is not clear whether there are any intrinsic deficiencies in this process that would increase the probability of failures compared to solder reflow processes even when all the necessary precautions are used, and assembly is carried out according to the most stringent guidelines for manual soldering.

Possible factors causing increased cracking of MLCCs during manual soldering include the following:

1. Insufficient preheating resulting in thermal shock. Contrary to the chamber soldering that stresses the whole surface of the capacitor, during manual soldering the shock might be experienced mostly by the terminals.
2. Excessive solder resulting in increased stresses caused by the mismatch of CTE between solder and ceramic.
3. Specifics of the PWB deformation caused by local heating might result in local deflection of the board that would cause flex-like cracking upon cooling.
4. Heating of the ceramic to a higher temperature than the board that might cause formation of tensile stresses and cracking upon cooling.

Note that in the two last cases, the rate of cooling is likely a decisive factor affecting the probability of cracking because solder creeping allows for stress relaxation when the system slowly cools down from the melting temperature. These factors will be analyzed in next year's (2009) part of the work conducted on soldering-induced stresses in ceramic capacitors. In the 2008 part of the work reported below, effects of thermal shocks and thermomechanical stresses caused by excessive solder were studied using seven types of large-size MLCCs. The capacitors have been characterized mechanically by measurements of CTE, hardness, and fracture toughness. External visual examination, electrical characteristics, and methanol tests were used to evaluate the susceptibility of the parts to cracking under multiple thermal shock and thermal cycling conditions.

2. Experiment.

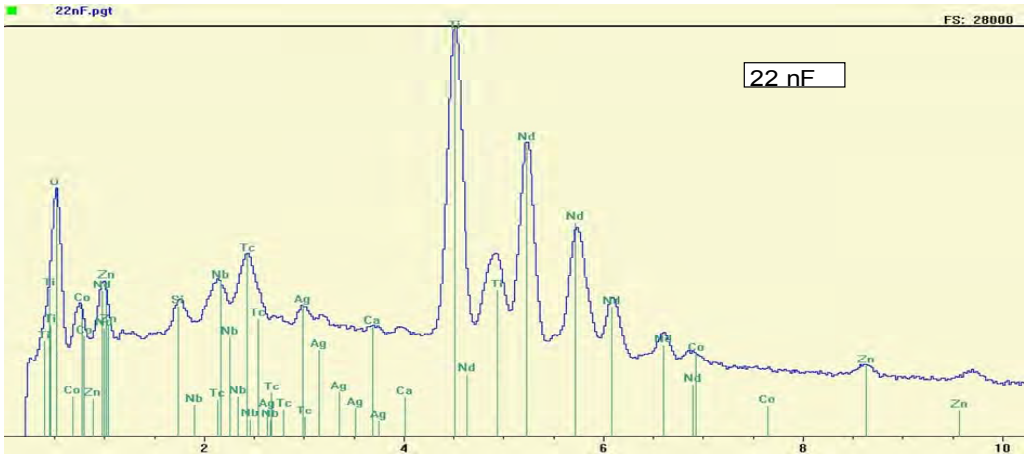
Seven types of large-size ceramic capacitors with sizes varying from 2220 to 2225 were used for this study. Table 1 displays vendors and characteristics of the part types used; W, L, and H indicate the width, length, and thickness of the parts. Six out of seven parts had high CV values and were made using X7R or X5R dielectrics (EIA class II) and one part, 22 nF 50 V, was made using a stable, temperature-compensating COG (or NPO) dielectric (EIA class I).

Table 1. Characteristics of MLCCs used.

Part	C and V	Vendor	Mater.	Size	W, mm	L, mm	H, mm
GRM55RR71H105KA01L	1.0 µF, 50 V	Murata Electronics	X7R	2220	4.79	5.78	1.85
GRM55FR60J107KA01L	100 µF, 6.3 V	Murata Electronics	X5R	2220	4.82	5.79	3.21
C2225C225K5RACTU	2.2 µF, 50 V	Kemet	X7R	2225	6.22	5.49	1.27
C5750X7R1H106M	10 µF, 50 V	TDK Corp.	X7R	2220	4.95	5.61	2.21
C5750X5R1C476M	47 µF, 16 V	TDK Corp.	X5R	2220	5.36	5.9	2.37
N2223H223K5GAC	22 nF, 50 V	Kemet	NPO	2223	6.11	5.71	1.05
C5750X7R1E226M	22 µF, 25 V	TDK Corp.	X7R	2220	5.28	5.89	2.47

Energy dispersive spectroscopy (EDS) analysis showed that the major component in the 22 nF capacitors was neodymium titanium oxide ($Nd_2Ti_2O_7$), while most EIA class II capacitors were made of barium titanate ceramics (see Figure 1).

To estimate post-soldering thermomechanical stresses in capacitors, coefficients of thermal expansion were measured using a thermal mechanical analyzer, TMA2940, manufactured by TA Instruments. The measurements were carried out at a rate of 3 °C/min. during several cycles of heating and cooling from room temperature to 350 °C. The CTE values were calculated after the first cycle was completed to anneal the samples and eliminate possible errors related to the built-in mechanical stresses. Measurements of deformation were carried out in three directions, along (X and Y) and across (Z) the plates. These directions corresponded to the length, width, and thickness of the part. Prior to the measurements, metal terminals were ground off and polished to avoid errors related to the presence of metal layers and solder.



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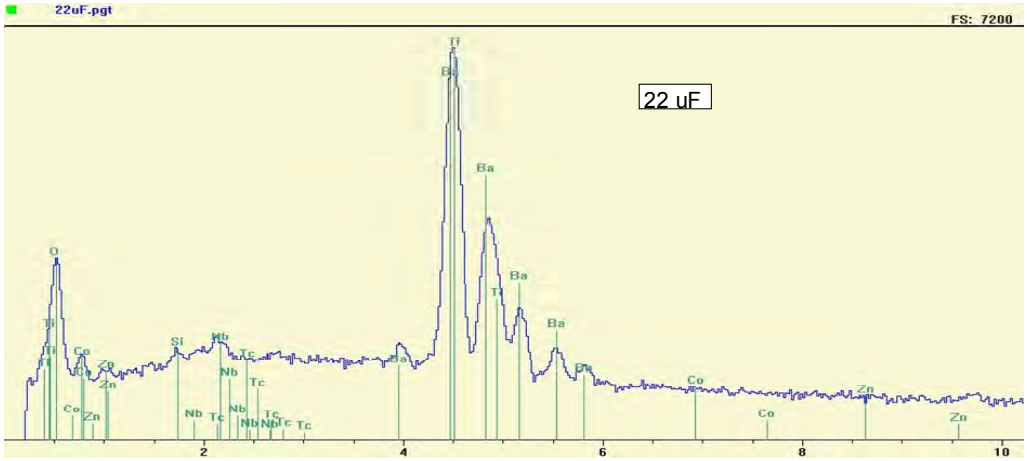


b)

Figure 1. Results of X-ray microanalysis of 22 nF 50 V (a) and 22 µF 25 V (b) capacitors.

Hardness and fracture toughness of the ceramic materials were measured using Vickers microindention tests. Prior to the testing, the parts were molded in epoxy low-stress room-temperature cure compound, ground using sand papers up to #2400 grit, and polished using a 0.5 µm diamond paste. The indenter was attached to a Metek AccuForce III gauge, and the testing was carried out on three samples of each type of capacitor at four load levels: P = 2 N, 4 N, 6 N, and 10 N. From five to 12 indentions were made on the cover layers at each force, and the size of the impressions (indent prints) and the length of cracks were measured in each of the capacitors using a scanning electron microscope (SEM). Figure 2 shows molded capacitors after Vickers testing, and Figure 3 shows typical optical and SEM views of the indents and radial cracks emanating from the corners of the imprints. The sizes of each imprint and crack were measured using Photoshop software, and the respective average values were used for calculations of the hardness and fracture toughness of the parts.

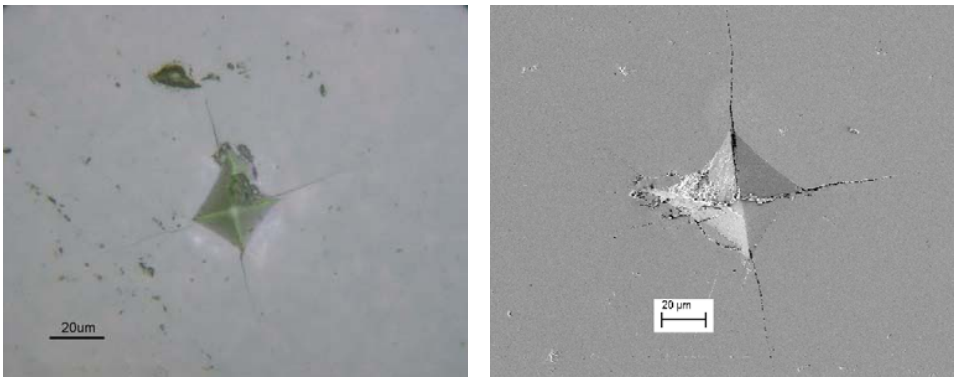
Figure 2. 22 μF 25 V capacitors after Vickers hardness testing. Dots indicate marks after indention testing made at different levels of the load.

The Vickers hardness (VH) and fracture toughness (K1C) were calculated based on the average diagonal size of the imprints, D:

$$VH = \frac{1.854 \times P}{D^2}, \quad (1)$$

$$K_{1c} = \varsigma \left[\frac{E}{H}\right]^{0.5} \left[\frac{P}{c^{1.5}}\right], \quad (2)$$

where E is the Young's modulus (~200 GPa [1, 35, 36]), c is the radial crack length measured from the center of the indent, and ζ is an empirically determined ''calibration'' constant usually taken equal to 0.0167 for Vickers indents.



(a) (b)

Figure 3. Typical optical (a) and SEM (b) views of imprints after Vickers indention testing.

It should be noted that measurements of the fracture toughness based on the Vickers indention testing have been criticized recently by Quinn and Bradt [37] because the results are not reliable and differ significantly compared to the standard fracture toughness tests. However, the Vickers indention fracture test allows in-situ evaluation of mechanical parameters directly on small

components, and ceramic capacitors in particular, and it is still widely used for analysis of mechanical behavior of MLCCs [35, 38] and of various high-brittleness materials [39-41].

To assess the probability of cracking, the parts were subjected to multiple thermal shocks and temperature cycles, and their characteristics, including capacitance (C), dissipation factor (DF), equivalent series resistance (ESR), and leakage current (DCL) were measured periodically through the testing. Although not specified for ceramic capacitors, ESR values were measured at 100 kHz to assess possible variations in the contact resistances of the parts.

To increase the sensitivity to cracking, DCL measurements were carried out at twice-rated voltages. Considering that per MIL-PRF-123 the minimum specified insulation resistance is determined as IR = 1E9*C, where C is in µF and IR is in Ohms, the maximum leakage current that is supposed to be measured after 2 minutes after voltage application can be calculated as DCL_{max} = 0.002*VR/C, where DCL is in µA, rated voltage (VR) is in volts, C is in µF.

Figure 4 shows typical examples of current relaxation with time for 20 samples in each part type. The results indicate that leakage currents decrease with time by one to two orders of magnitude, and they continue decreasing even after 1,000 seconds of electrification. To evaluate possible effect of cracking, the leakage currents were monitored for 1,000 seconds after voltage application to assure that no interruptions occurred, and the DCL reading for further analysis was taken after 1,000 seconds.

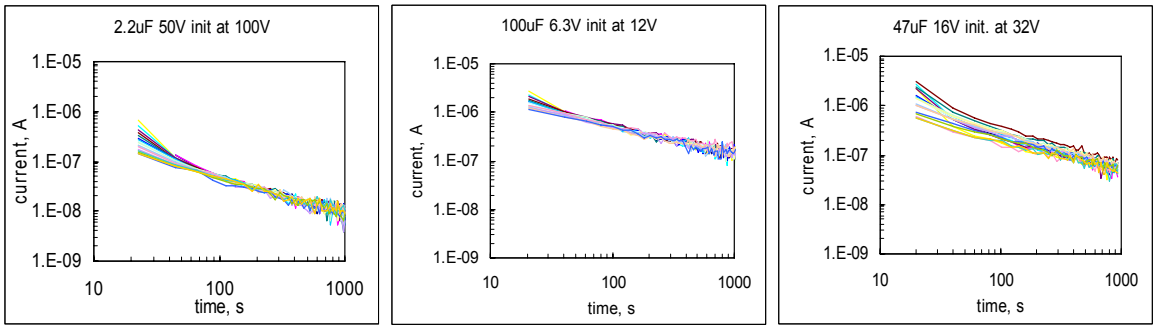
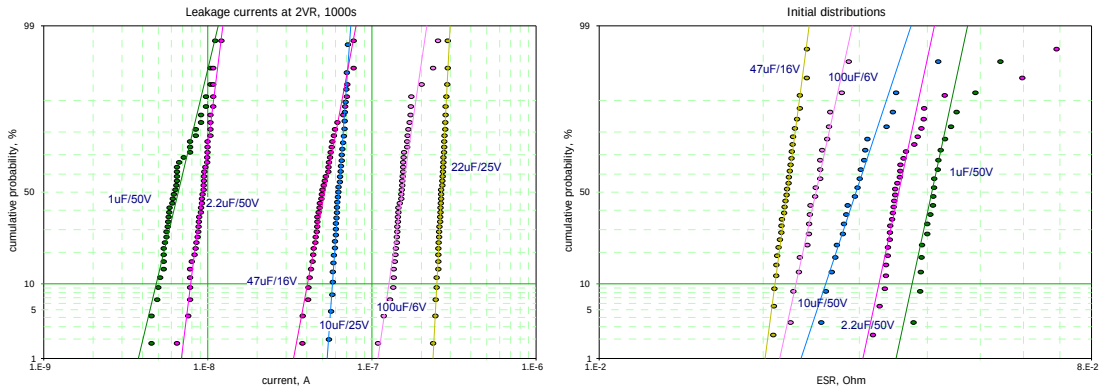


Figure 4. Current relaxation in three types of capacitors at twice-rated voltages.

Typical distributions of DCL and ESR values for six types of capacitors are shown in Figure 5. Note that for both parameters, DCL and ESR, the best fit was obtained using log-normal functions. Distributions of DCL values had relatively low standard deviations, varying from 0.05 to 0.18, indicating good reproducibility of the measurements. The leakage currents were five to 20 times below the specified limits, and the lots had no outliers. This increases the probability of revealing defects during testing of the parts by using DCL measurements.

ESR distributions in some lots had a relatively large spread, and one to three samples can be considered as ESR outliers in 10 µF 50 V, 2.2 µF 50 V, and 1 µF 50 V capacitors (see Figure 5.b).



a) b)

Figure 5. Log-normal distributions of leakage currents (a) and ESR (b) for different types of capacitors.

A methanol test was used to further increase the sensitivity of leakage current measurements to cracking [26]. During this testing, the parts were preheated to 85 ^{o}C for 15 minutes and then immersed into methanol at room temperature for 3 minutes. DCL measurements were repeated after methanol removal and drying the part for ~1 minute.

3. Mechanical characteristics of capacitors.

Results of measurements of CTE, hardness, and fracture toughness of the capacitors used in this study are described below.

3.1. Thermomechanical characteristics.

Figure 6 shows variations of deformation and calculated CTE values with temperature for six types of ceramic capacitors. Analysis of these data indicates a significant variation of the rate of deformation below and above the Curie temperature (Tc). These variations result in extreme temperature dependencies of CTE that for barium titanate, class II, ceramics has a minimum in the range from 120 ^{o}C to 130 ^{o}C, which correspond to Tc values for these capacitors.

Anomalous deformation of ceramic capacitors at temperatures close to Tc were also reported by He [42]. Similar behavior is known for perovskite oxides, and is due to changes of the crystalline lattice over the ferroelectric transition. Careful examination of the thermal expansion curves revealed that within the narrow temperature range of the ferroelectric transition, the thermal expansion becomes negative [42].

Results in Figure 6 show that at temperatures above Tc, T ~140 ^{o}C, CTE values calculated for the three directions are close and vary in the range from 10 to 12 ppm/K for different part types. As temperature increases from ~130 ^{o}C to 350 ^{o}C, CTE values are slightly increasing at a rate varying from 0.008 ppm/K^2 to 0.017 ppm/K^2.

Due to relatively minor variations with temperature, CTE values below (CTE1) and above (CTE2) Curie temperature were calculated as average values for these two regions. Results of these calculations based on measurements of deformations across (Z), along the length (X), and along the width (Y) of the parts are presented in Table 2. Average high-temperature CTE values

(in the range from 140 ^{o}C to 350 ^{o}C) are close, and for different types of capacitors vary from 12.1 ppm/^{o}C to 14.4 ppm/^{o}C. These data are similar to those typically reported for $BaTiO_3$ ceramics [1, 43]. At T < Tc CTE varies with temperature significantly, but on average remains much lower (from 3.1 ppm/^{o}C to 9.6 ppm/^{o}C) than for the high-temperature region. Based on He's data, low-temperature CTE values for different manufacturers of X7R capacitors vary for 5.5 ppm/^{o}C to 7 ppm/^{o}C, and the high-temperature data are in the range from 12 ppm/^{o}C to 14 ppm/^{o}C, which is in agreement with our results.

Table 2. CTE values (in ppm/^{o}C) calculated based on measurements along three directions for ceramic capacitors.

Capacitor	CTE_Z_1	CTE_Z_2	CTE_X_1	CTE_X_2	CTE_Y_1	CTE_Y_2
1.0 µF, 50 V	8.1	12.1	8.4	12.5	8.8	12.2
100 µF, 6.3 V	3.1	13.6	11.3	13	12.3	13.1
2.2 µF, 50 V	8.7	13.8	8.9	12.2	-	-
10 µF, 50 V	7.6	12.65	9	12.3	-	-
47 µF, 16 V	4.5	12.9	-	-	-	-
22 nF, 50 V	8.9	13.3	10.3	12.2	-	-
0.1 µF, 50 V	9.6	14.4	-	-	-	-
Average	8.6*	13.2	9.6	12.4	10.6	12.7

*Calculated without data for high-C capacitors (47 µF and 100 µF).

Figure 6 shows that in most cases the CTE values measured across the capacitors (Z direction) are slightly higher than CTE measured along the plates. This difference is more significant for 10 µF and 100 µF capacitors compared to 1 µF parts and might be related to the built-in mechanical stresses in MLCCs. It has been shown that due to the difference between CTE of ceramics and metal electrodes (Ni or Pd/Ag have greater CTE), there is a compressive in-plane stress in the active layers of the MLCC [44]. The residual stress increases with the number of dielectric layers, and changes electrical characteristics of capacitors depending on the direction of applied force [45]. It is possible that these stresses result also in anisotropy of deformation with temperature that is more pronounced for parts with high capacitance value. The effect is more obvious for large-value capacitors comprised of many layers of ceramic and electrode materials, and for this reason likely the anisotropy of CTE was not observed in other studies [1, 42].

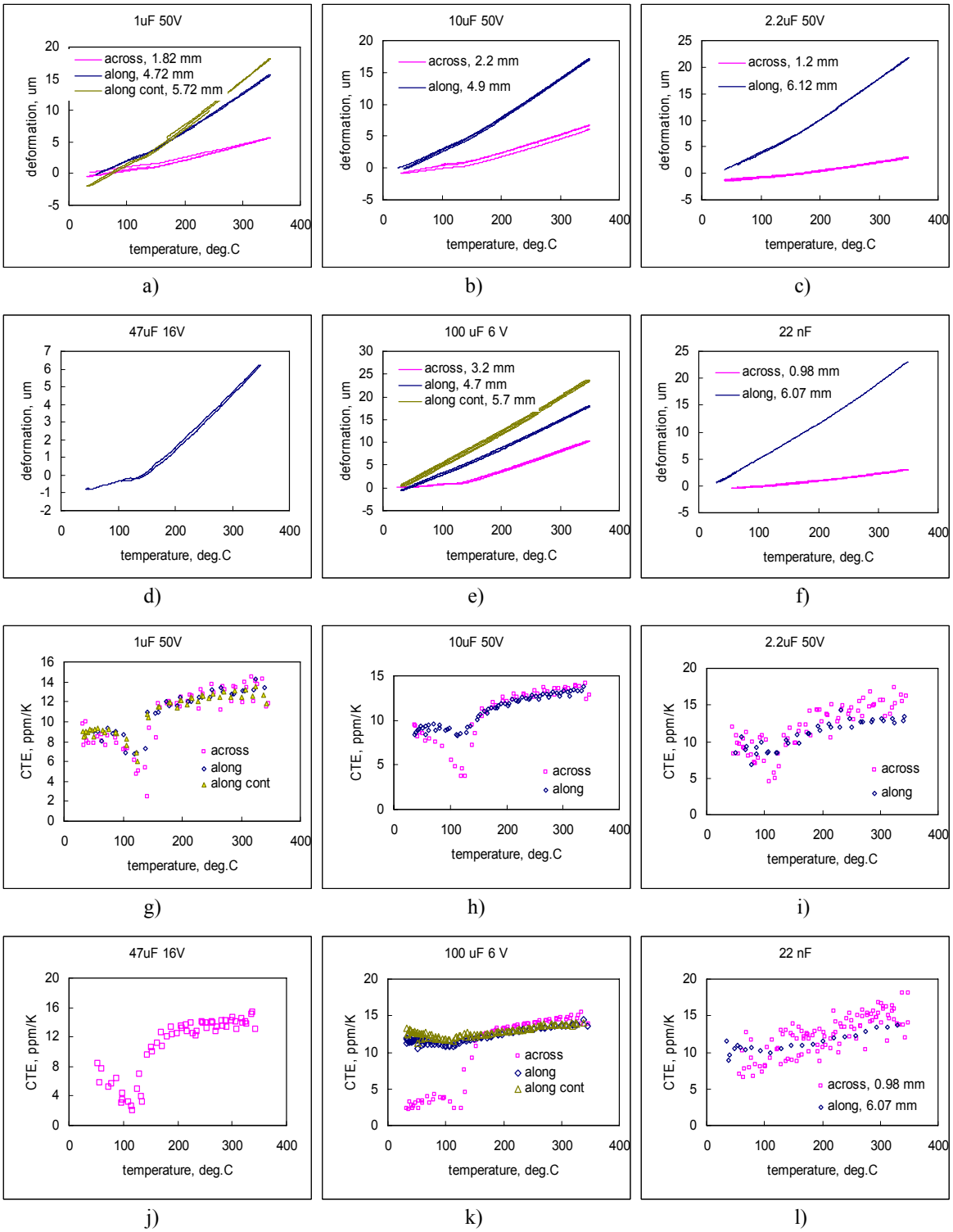


Figure 6. Temperature dependencies of deformation (a-f) and CTE (g-l) for six different types of capacitors.

3.2. Vickers indention test.

Average values of the size of imprints and crack lengths for different types of capacitors were measured using a SEM, and variations of these parameters with load are plotted in Figure 7. The imprint size increases with load sublinearly, and the spread of data obtained for three samples is relatively small, below 9%, indicating a high reproducibility of hardness measurements. As expected, the spread of the crack lengths was greater, but it still remained within 20%, indicating a reasonable level of reproducibility of the measurements. Note that cracks radiating from the corners of the imprints were observed in all samples and at all levels of the load, except for 22 nF capacitors at a load of 2 N. This is due to a higher fracture toughness of COG dielectrics compared to X7R materials.

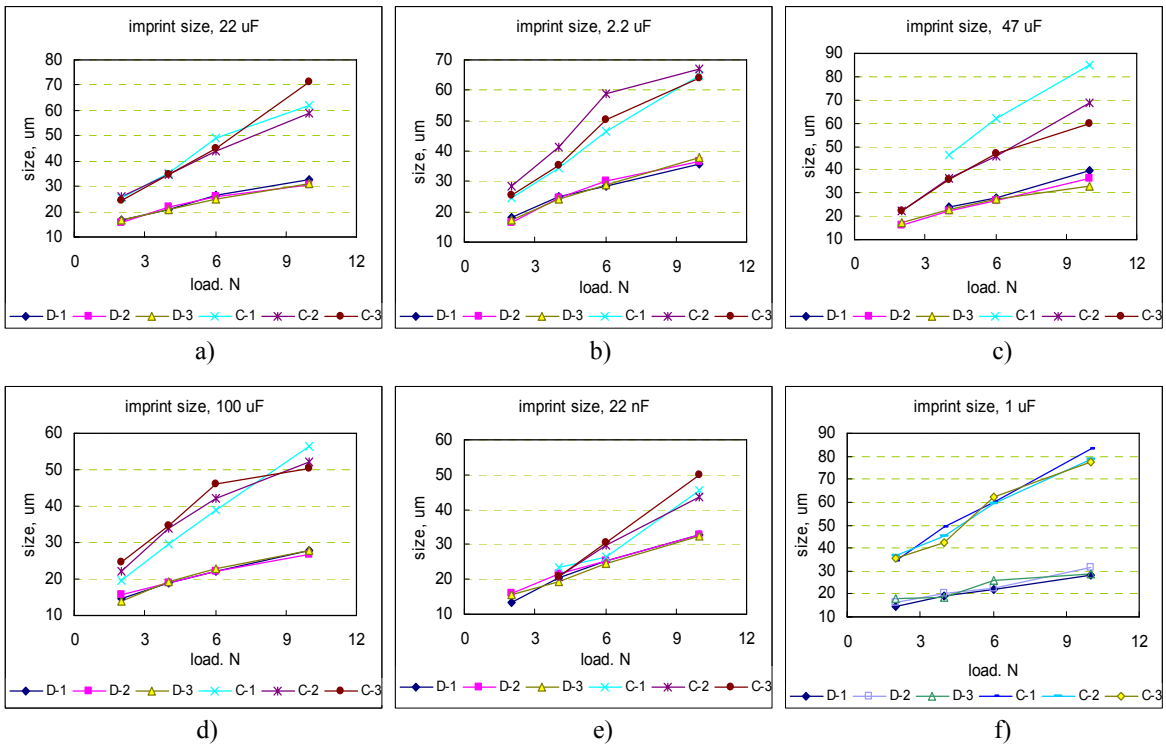


Figure 7. Variations of the size of imprints (D) and the length of radial cracks (C) in different types of capacitors. Each mark corresponds to an average value calculated for five to 12 impressions.

Based on results presented in Figure 7 and using Eq. (1), Vickers hardness was calculated for different load levels. Results of these calculations are presented in Figure 8 and indicate a relatively minor increase of VH with the load. This allowed for characterization of each part type with an average value of hardness. The average values together with the respective standard deviations are displayed in Table 3. Indentation fracture toughness was calculated using Eq. (1) and (2) and is shown in Figure 9. The values of K1C were virtually independent of the load for all part types, thus also allowing characterization of the capacitors with an average fracture toughness and standard deviation (see Table 3).

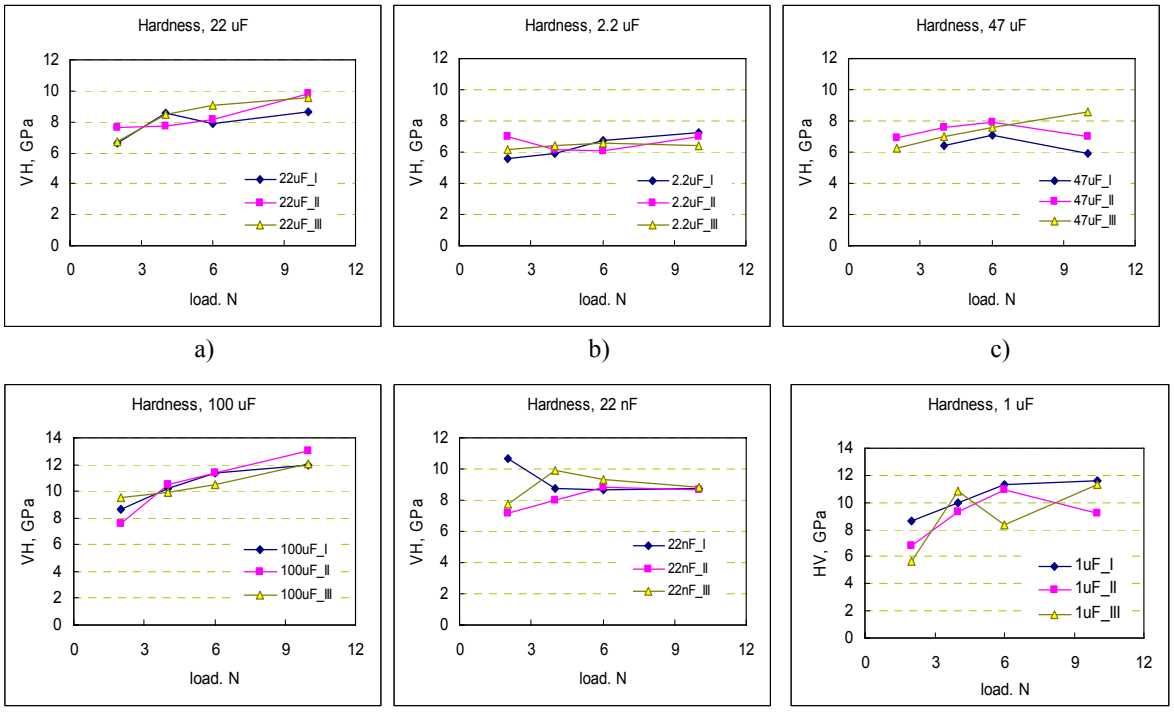


Figure 8. Variations of Vickers hardness with load for six different types of capacitors.

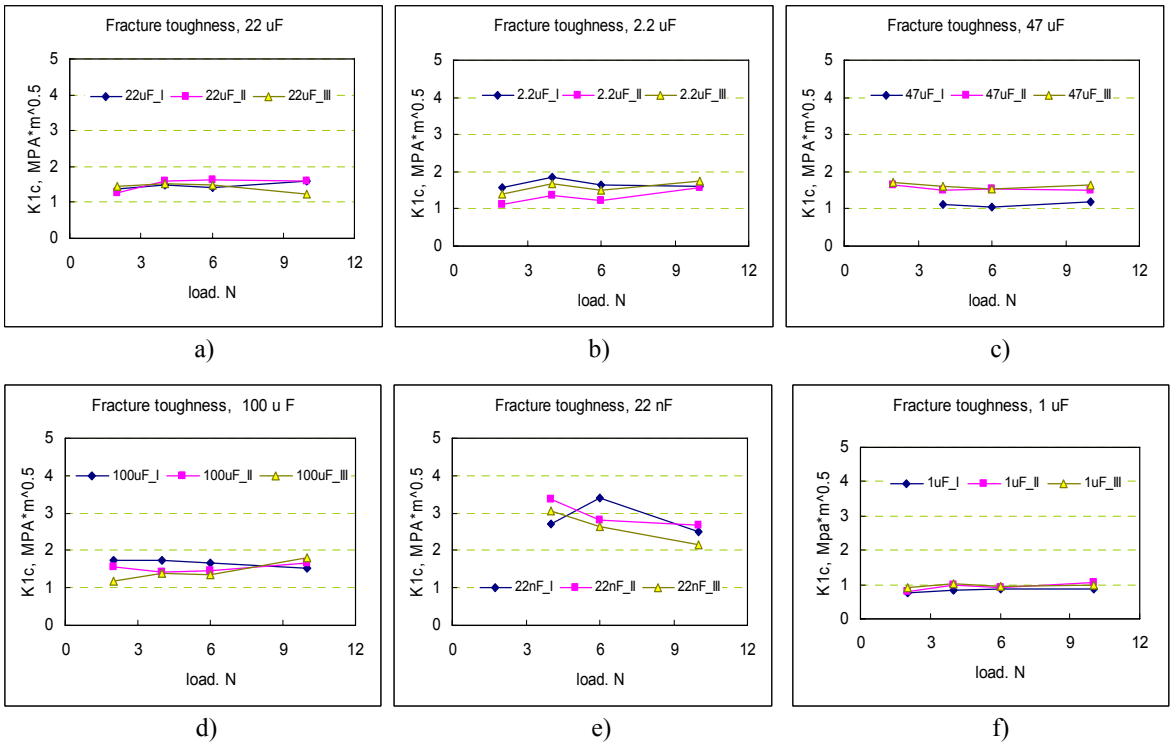


Figure 9. Variations of fracture toughness with load for six different types of capacitors.

Hardness of different capacitors varied in the range from 6.5 GPa to 10.6 GPa and did not depend on the type of materials used. According to Wereszczak et al. [35], the hardness of X7R materials was in a narrow range of 11 GPa to 12 GPa, which is close to our data. The reason for relatively low values obtained for 2.2 µF 50 V and 47 µF 16 V capacitors is not clear. Although VH does not indicate the potential mechanical robustness of MLCCs directly, its value can provide some insight into the effects of porosity and grain size because hardness is typically an inverse function of the amount of porosity [35].

Table 3. Hardness and fracture toughness of ceramic capacitors.

Capacitor	HV, GPa	STD	K1C, MPa-m$^{0.5}$	STD
1.0 µF, 50 V	9.49	1.66	0.91	0.07
100 µF, 6.3 V	10.57	1.57	1.55	0.09
2.2 µF, 50 V	6.45	0.30	1.52	0.14
10 µF, 50 V	10.37	1.03	1.06	0.13
47 µF, 16 V	6.62	1.22	1.37	0.08
22 nF, 50 V	8.78	0.19	2.81	0.32
22 µF, 25 V	8.24	0.97	1.47	0.07

Analysis of results presented in Table 3 shows that for X7R dielectrics the fracture toughness varies from 0.9 to 1.55 MPa-m$^{0.5}$, and it is much higher for the NPO dielectric, 2.8 MPa-m$^{0.5}$. These results are in agreement with the data reported by other authors [5, 35, 38]. Based on statistically significant variations of K1C, capacitors can be arranged in a row with increased fracture toughness: 1 µF 50 V ≈ 10 µF 50 V < 47 µF 16 V < 22 µF 25 V ≈ 2.2 µF 50 V ≈ 100 µF 6 V << 22 nF 50 V. The mechanical stability of the parts was expected to increase in the same sequence.

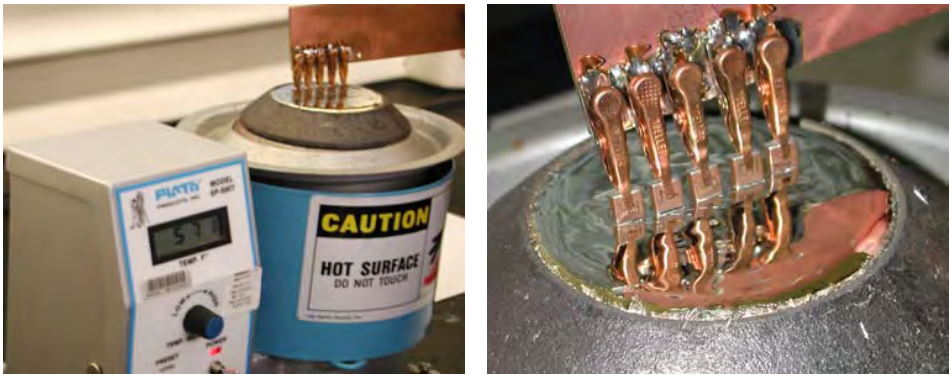
4. Effect of thermal shock.

When temperature at the surface of a ceramic capacitor that is stabilized at temperature T_o suddenly changes to temperature T, the surface areas experience deformation compared to the internal areas of the part that remain at T_o. This causes development of mechanical stresses that depend on the thermal and mechanical characteristics of the ceramic and vary with time due to changes in temperature distribution through the part. The value of temperature difference $\Delta T = T - T_o$, at which cracking is observed, can be used to characterize the thermal shock resistance of the part, ΔT_f.

Experiments for assessment of the robustness of MLCCs to thermal shocks were carried out by preheating the parts to a certain temperature and then quenching them into water at room temperature [38] or at 0 ^oC (ice water) [8, 46]. The value of the thermal shock resistance temperature, ΔT_f, was estimated using measurements of leakage currents of the capacitors after water quenching. Depending on the part type and size of capacitors, experimental values of ΔT_f for X7R materials varied in the range from 120 ^oC to 440 ^oC.

At relatively low ΔT_f temperatures, the probability of cracking is extremely small. The effect of preheating of ceramic capacitors having sizes 1206 and 0805 at temperatures ranging from 155 ^oC to 100 ^oC on results of wave reflow soldering at 235 ^oC did not reveal any thermal cracking or leakage current failures [22].

To simulate the effect of thermal shock conditions that a capacitor might experience during manual soldering, the parts were installed in a fixture as is shown in Figure 10, and their terminals were brought into thermal contact for 5 seconds with molten solder maintained at 300 ^{o}C. After that, the parts were cooled at room temperature for 5 minutes, and the procedure was repeated. Twenty samples of each part type were subjected to this terminal-thermal-shock testing. Considering that in our experiments the temperature during thermal shock increased rapidly by 280 ^{o}C, and the capacitors experienced 100 shocks, it was expected that cracking would appear at least in some lots. However, none of the parts manifested cracking or failures during this testing.



a) b)

Figure 10. Overall (a) and close-up (b) views of the parts during terminal-thermal-shock testing.

Electrical measurements and visual control using an optical microscope were carried out after 10, 30, and 100 thermal shocks. Results of DCL measurements are presented in Figure 11. Note that the DCL levels for 22 nF 50 V NPO capacitors were below 1 nA, which is the sensitivity level for the measurement system used in this study. For this reason, data for the NPO parts are not presented.

No anomalies during I-t measurements or any substantial increase in the leakage currents were detected during the post-cycling current monitoring. No defects were found during multiple optical examinations at 10X magnification. Measurements of AC characteristics (see Figure 12) also did not reveal any anomaly. The vicinal illumination technique [30] used to examine surface areas of the capacitors near terminals at 200X magnification upon test completion failed to reveal any cracks.

The results indicate that manual-soldering-induced thermal shocks do not cause damage to normal-quality large ceramic capacitors. If parts are not susceptible to thermal-shock cracking, multiple-shock stresses likely will not cause formation of defects after up to 100 thermal shocks.

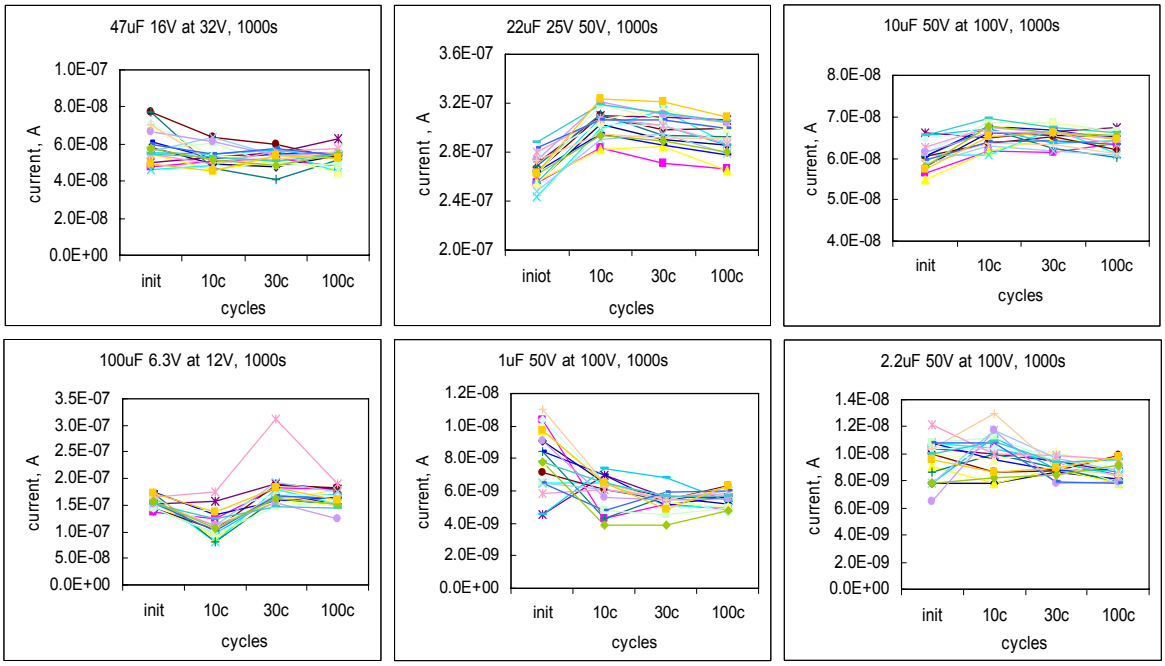
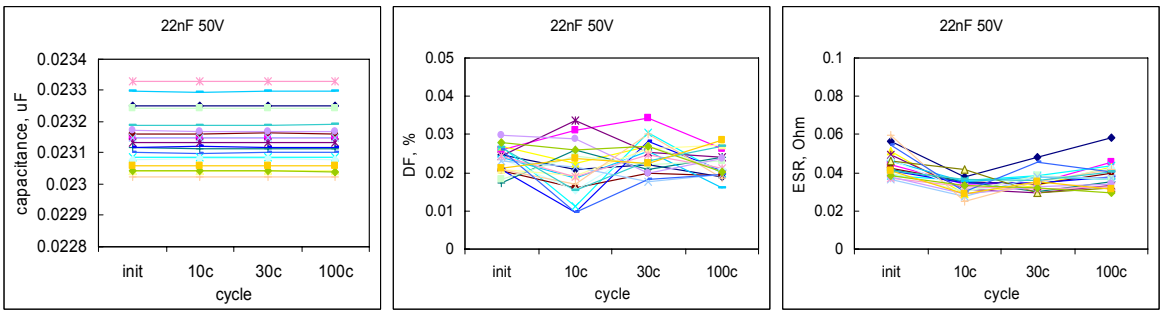


Figure 11. Variations of leakage currents during terminal-thermal-shock cycling for six types of MLCCs. Each chart shows data for 20 samples.



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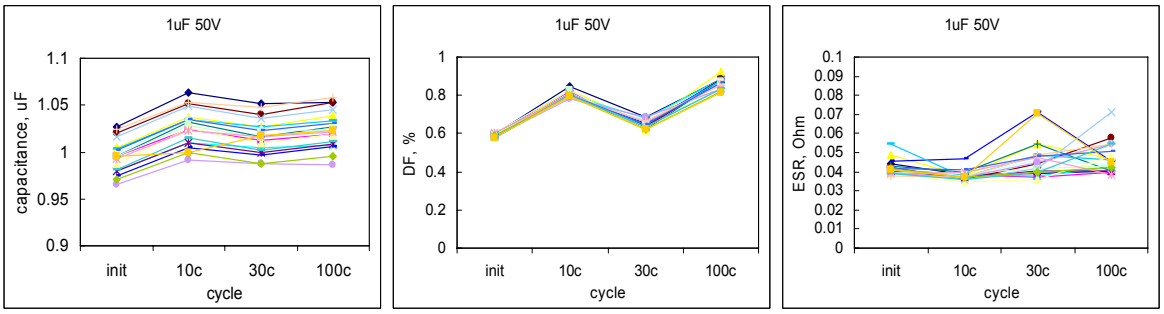
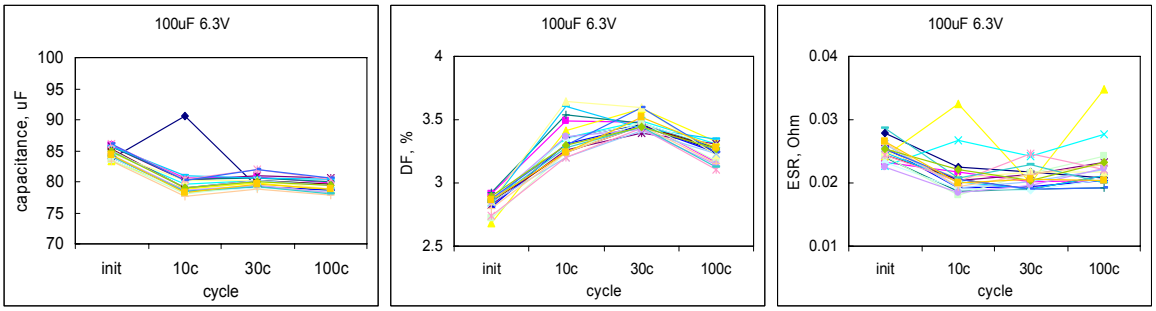


b)

Figure 12.a. Variations of capacitance, dissipation factors, and equivalent series resistances during terminal-thermal-shock cycling for two types of capacitors. Each chart shows data for 20 samples.



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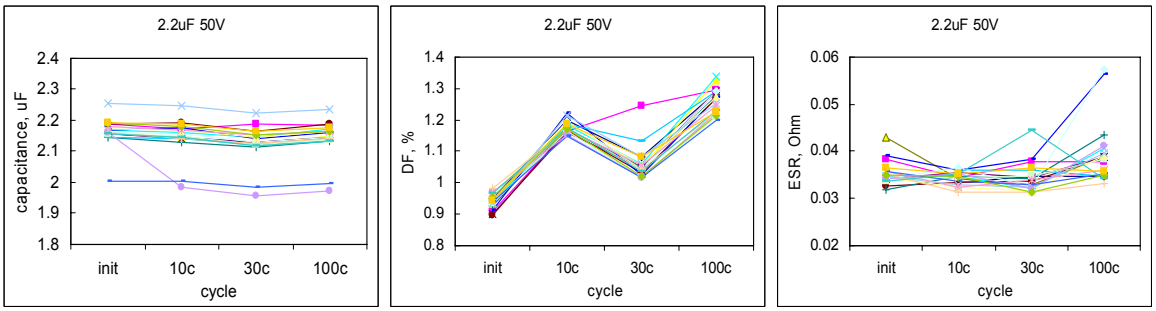

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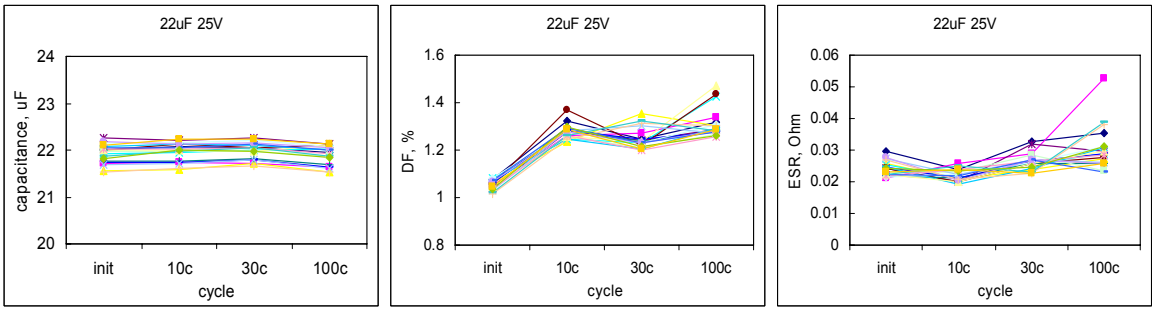
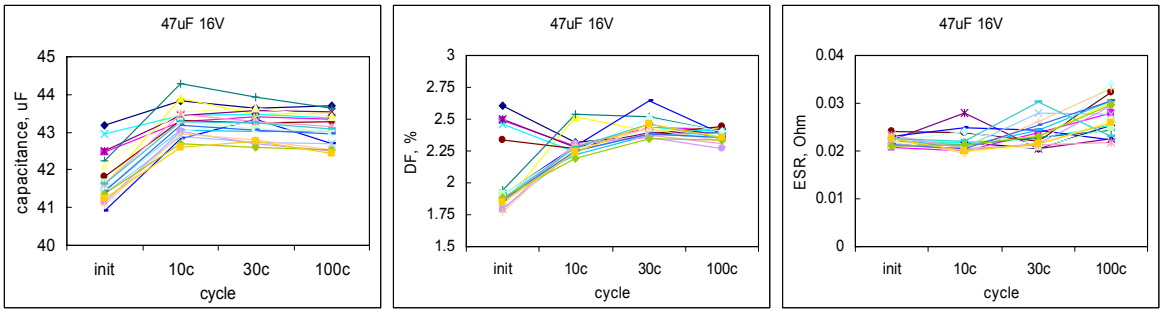


e)

Figure 12.b. Variations of capacitance, dissipation factors, and equivalent series resistances during terminal-thermal-shock cycling for three more types of capacitors. Each chart shows data for 20 samples.



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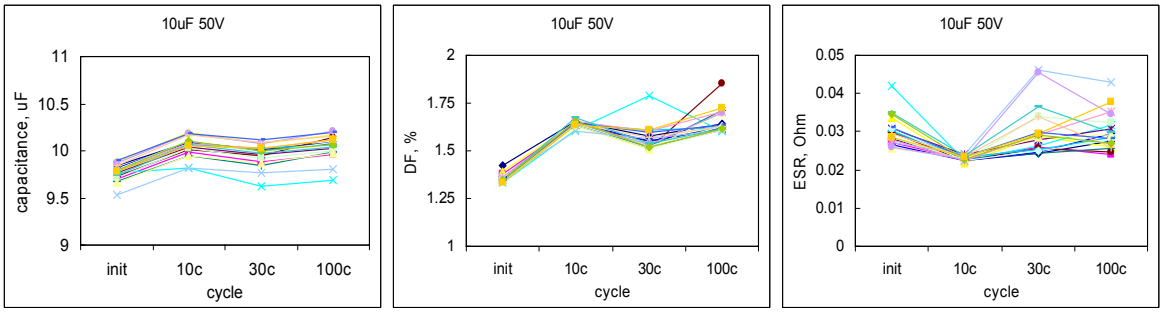


g)

Figure 12.c. Variations of capacitance, dissipation factors, and equivalent series resistances during terminal-thermal-shock cycling for two types of capacitors. Each chart shows data for 20 samples.

5. Effect of excessive solder.

Due to the difference between CTE of solder (~24 ppm/K) and ceramic materials (10 to 14 ppm/K), an excessive amount of solder might create significant compressive stresses at the terminals of capacitors upon cooling to room temperature. As ceramic materials have a very high compressive strength, these stresses likely will not cause cracking. However, relaxation of stresses with time due to solder creeping might result in formation of tensile stresses when the part is heated after some time of being stored at normal conditions. It is also possible that solder-induced compression at the terminals would cause a moment of force and form tensile stresses at the surface of the ceramic near the terminals.

To evaluate the effect of solder-induced stresses, large solder blocks were attached to one of the terminals of each capacitor tested. To form these blocks uniformly, a eutectic solder was molten in a cylindrical depression made in a Teflon plate. One terminal of each of the capacitors was immersed into the solder that was then solidified forming blocks shown in Figure 13. Five samples of each part type were prepared using this technique.

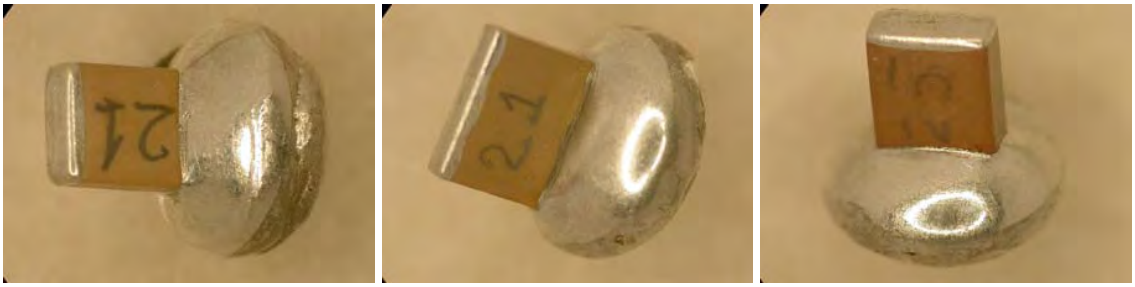


Figure 13. Examples of solder blocks attached to terminals of different types of capacitors to simulate the effect of stresses caused by excessive solder.

Capacitance, dissipation factor, and leakage currents of the parts were measured after various tests shown in Table 4. Methanol testing was used after each of the stress tests to better reveal possible cracks. For this reason DCL measurements were made twice, first right after completion of the stress testing, and second after methanol application.

Table 4. Test flow for capacitors with solder blocks.

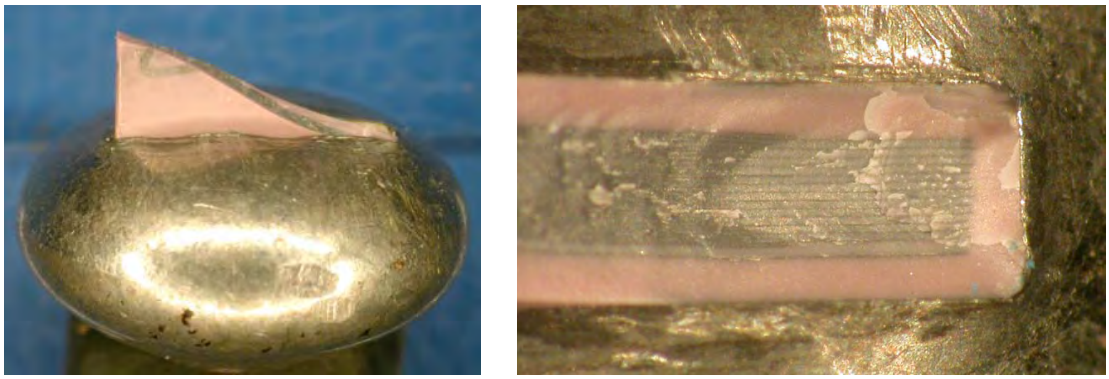
Test Type	Index	Temperature Range, °C	Condition	Number of Cycles
Temp. Cycle	TC1	+25 to +165	Dwell 10 min., ramp 10 min.	20
Temp. Cycle	TC2	+25 to -65	Dwell 10 min., ramp 10 min.	20
Temp. Cycle	TC3	-65 to +150	Dwell 10 min., ramp 10 min.	20
Thermal Shock	TS	-65 to +150	Dwell 10 min., ramp 0.1 min.	20
Immersion into Liquid Nitrogen	LN	+25 to -196	Dwell 1 min., ramp 0.1 min.	1

The parts were subjected to different types of temperature cycles and thermal shocks according to a test flow shown in Table 4. During TC1 test, the parts were subjected to 20 cycles between room temperature and +165 °C to create tensile stresses at high temperatures. During the next test, TC2, the parts were stressed at negative temperatures (to -65 °C) to squeeze the terminals by compressive stresses induced by solder, and possibly create local tensile stresses in ceramic along the edges of the solder chunk. Test TC3 combined the effects of both previous tests.

The thermal shock test, TS, was performed at the same temperature conditions as temperature cycling test TC3, but with the temperature ramp increased by more than 100 times. It is possible that at slow temperature variations the stress relaxation is significant, so the TS test was carried out to reveal the effect of temperature rate on test results. During the last test, LN, the parts were immersed directly into liquid nitrogen at -196 °C to create extreme thermal shock conditions and further increase the level of compressive stresses.

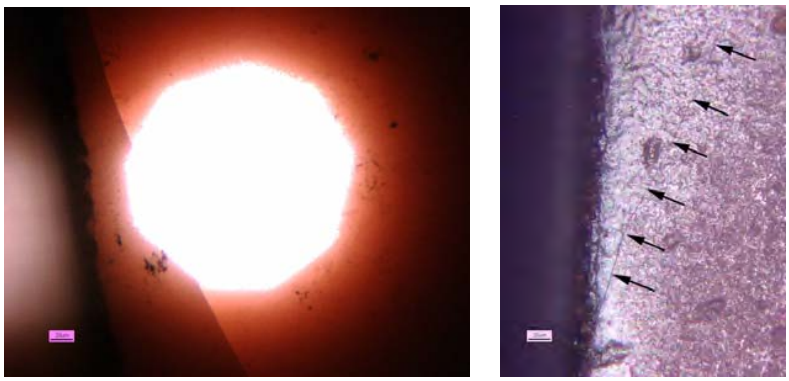
Fractures were observed only in samples of 22 nF 50 V NPO capacitors. One sample, SN 23, fractured after TC2 testing (see Figure 14). Another sample from this lot, SN 22, was found shorting at ~70 kOhm during post-TC2 methanol testing. However, low-power optical microscope examinations did not reveal any anomalies. After testing, all parts were examined using the vicinal illumination technique [30] and cracks originating from the solder edge, similar

to those shown in Figure 15, were revealed in all 22 nF 50 V capacitors. No cracks were found in X7R capacitors even after exposure to the liquid nitrogen temperature.



a) b)

Figure 14. Side (a) and top (b) views of a 22 nF 50 V sample that fractured after TC2. Note that the crack originated from the surface of the capacitor at the edge of solder chunk.



a) b)

Figure 15. A typical crack exposed in 22 nF 50 V capacitors by the vicinal illumination technique (a). Figure b) shows a crack observed at X100 magnification.

Results of electrical testing of the parts are shown in Figures 16 and 17 and can be summarized as follows:

1. Temperature cycling affected the value of capacitance in all parts with X7R dielectrics. Exposure to high temperatures increased C by ~4% to 5%, and exposure to low temperatures decreased capacitance by ~5% to 7%.
2. Dissipation factors increased in X7R parts through the testing by 30% to 50%. The most significant variations happened after TC1, when the parts were exposed to high temperatures only.
3. Leakage currents were stable through the testing in three out of seven of the tested lots: 47 µF 16 V, 100 µF 6 V, and 22 µF 25 V capacitors.

4. Three lots had instances of increased DCL:
   4.1. One sample in the 1 µF 50 V lot of capacitors increased DCL by an order of magnitude after TC3; however, further testing did not confirm the presence of cracking.
   4.2. An increase in DCL of more than an order of magnitude was detected in one of the samples from the 10 µF 50 V lot. However, this increase occurred during the first DCL measurements and was not confirmed by the methanol test.
   4.3. Three out of five samples increased in DCL values by up to two orders of magnitude through the testing after TC2 in a lot of 2.2 µF 50 V capacitors.
5. In a lot of 22 nF 50 V NPO capacitors, one sample fractured and two more showed anomalously high leakages after TC2 cycling. These parts also manifested anomalies during C and DF measurements.

An increase of capacitance upon exposure to high temperatures is a known phenomenon and is related to the aging of MLCCs that results in changes of the domain structure and causes a linear capacitance decrease with the logarithm of time. Annealing of the parts at temperatures exceeding the Curie temperature (de-aging) restores the value of capacitance and explains increase in C after high-temperature cycling, TC1. Most likely the observed increase in dissipation factors after TC1 is also due to the de-aging effect that reverses decrease of dielectric losses with time of aging. Note that the last temperature the parts experienced during TC3 cycling was 150 ^{o}C. For this reason similar values of C were measured after TC1 and TC3. NPO dielectrics do not exhibit this phenomenon. This explains stability of capacitance after TC1 for 22 nF 50 V capacitors.

Possible reasons of decrease of capacitance are less obvious. Most likely this effect is due to stress-induced variations of the dielectric constant in barium titanate ceramics. It is known that mechanical stresses lead to development of 90^{o} domains in $BaTiO_3$ materials that might decrease polarization [47]. Experiments with MLCCs showed that compressive stresses applied perpendicular to electrode plates might significantly decrease dielectric constant of ceramic materials [44, 45, 48]. The decrease of C by 5% to 7% that was observed during experiments might be due to relatively minor stresses in the range from 20 MPa to 40 MPa. It is possible to assume that substantial tensile stresses developed in solder at low temperatures due to CTE mismatch between solder and ceramic cause formation of additional compressive stresses in ceramic when the part is brought back to room temperature. Note that for all part types the values of C after exposure to -65 ^{o}C and to -196 ^{o}C remain the same, thus indicating that the effect does not increase significantly with the temperature swing.

Although temperature conditions for TC3 and TS were similar, capacitance of the parts after TS was lower than after TC1 or TC3. This might be due to more substantial residual compressive stresses created by fast changes of temperature when creeping of the solder does not have time to develop.

Optical examinations revealed cracks on all 22 nF 50 V capacitors; however, two parts did not have any significant degradation of leakage currents. It is possible that cracks in these two parts were shallow and did not cross opposite electrodes.

Five samples in three lots of X7R capacitors had DCL anomalies, but optical examinations revealed no cracks. A failure analysis might be necessary to confirm the presence of cracks in

these parts. However, in the absence of hard shorts, the probability of revealing possible microcracks is not high.

Analysis shows some correlation between the thickness of capacitors and the probability of cracking and/or having a DCL anomaly. The thinnest parts, 22 nF 50 V capacitors with H = 1.05 mm, had the largest proportion of fractures and DCL failures. Multiple DCL anomalies were observed in 2.2 µF 50 V capacitors with H = 1.27 mm. Two part types, 1 µF 50 V and 10 µ /50 V capacitors, had one sample each with increased DCL values; these parts had thicknesses of 1.85 mm and 2.2 mm, respectively. The thickness in the rest of parts that had no anomalies exceeded 2.3 mm.

Interestingly, in several cases application of methanol for parts with excessive DCL values decreased leakage currents, thus casting some doubt on the effectiveness of this test. It is possible that these results are due to preheating at 85 ^{o}C that was used before immersing capacitors into methanol. The purpose of this preheating was to expand the crack and enhance penetration of methanol. However, preheating results also in moisture removal that might have an adverse effect on the leakage currents.

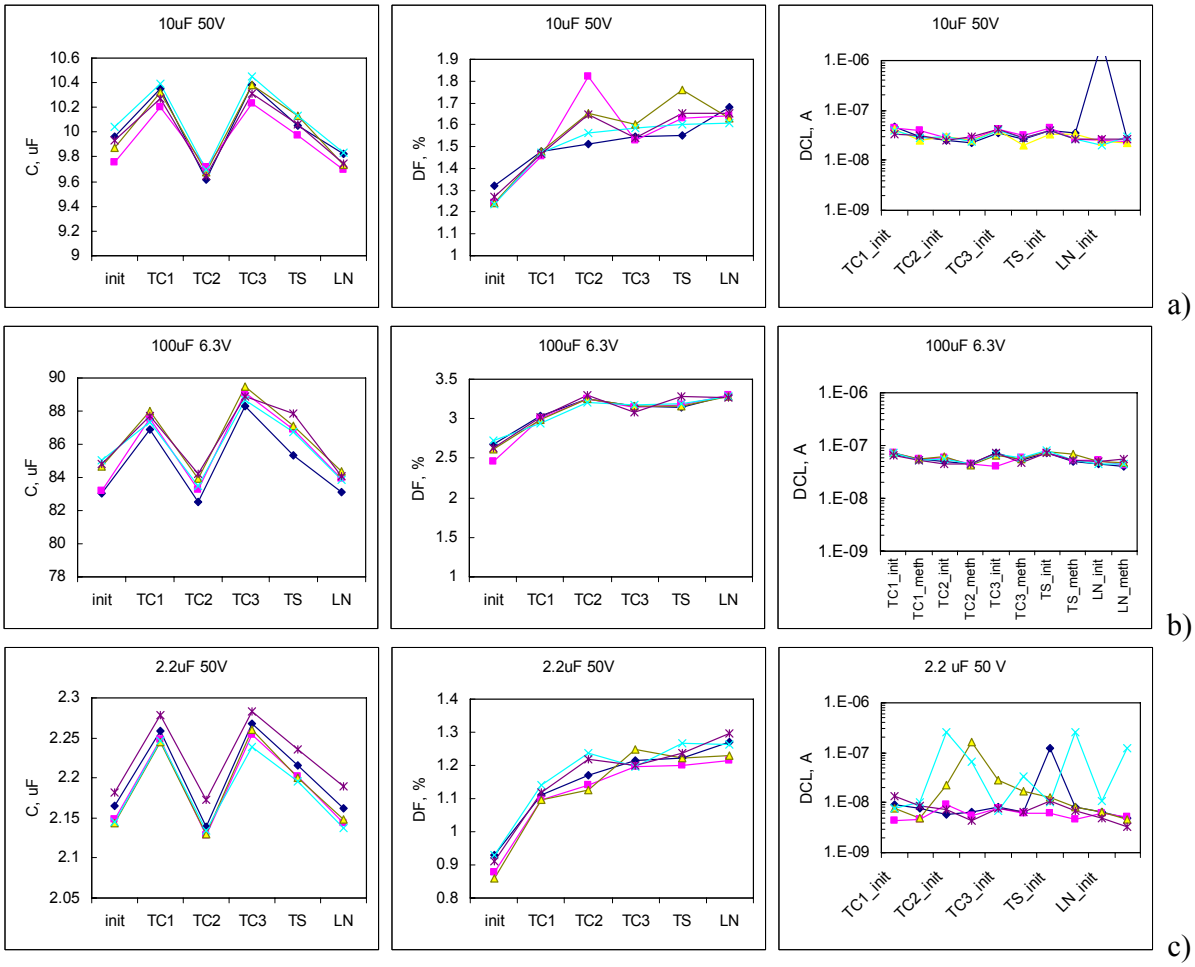
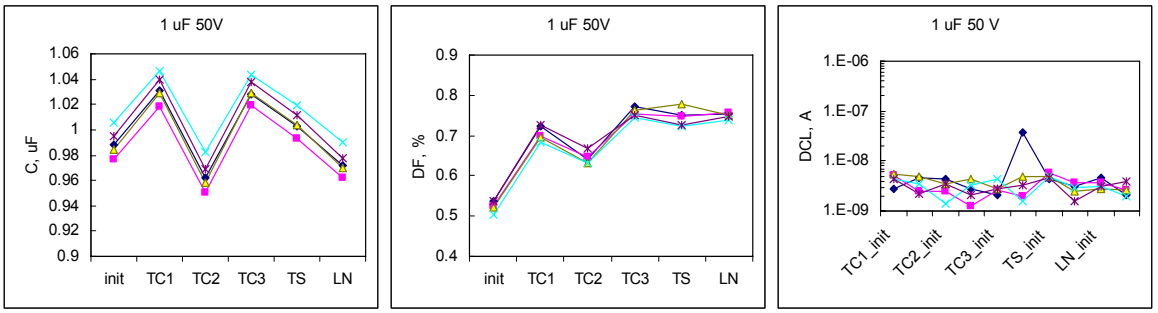
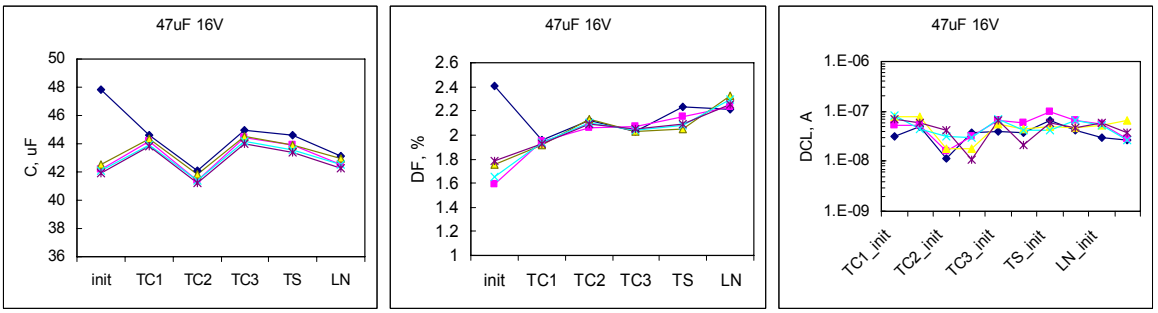


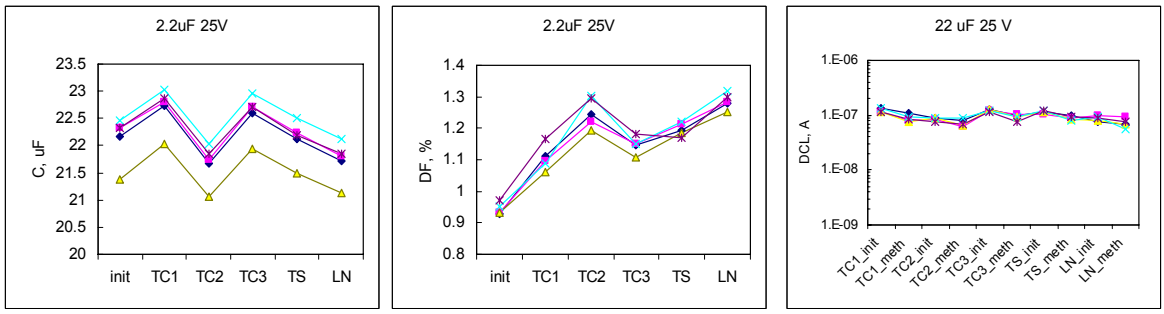
Figure 16. Effect of temperature cycling and thermal shocks for 10 µF 50 V (a), 100 µF 6 V (b), and 22 µF 50 V (c) ceramic capacitors with solder blocks.



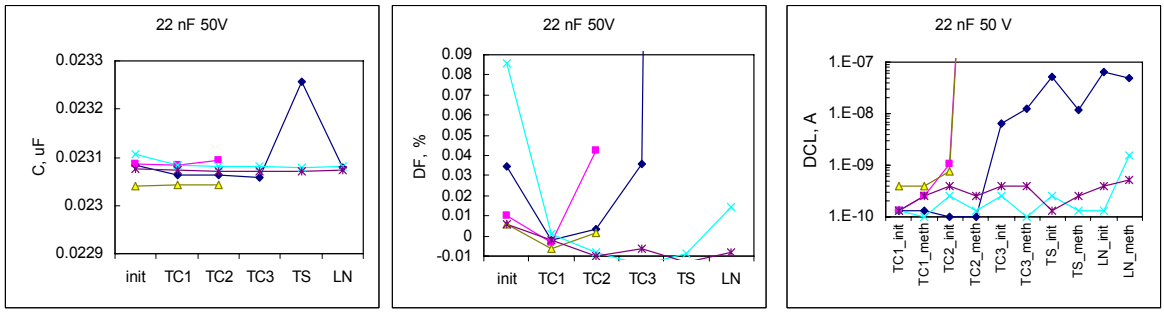
a)



b)



c)



d)

Figure 17. Effect of temperature cycling and thermal shocks for 1 µF 50 V (a), 47 µF 16 V (b), 22 µF 25 V (c), and 22 nF 50 V (d) ceramic capacitors with solder blocks.

6. Effect of TC after soldering onto an FR4 board.

To evaluate the effect of thermomechanical stresses developed in capacitors mounted onto a PWB during temperature excursions on the probability of cracking, 10 samples from four different lots (100 µF 6 V, 22 µF 25 V, 47 µF 16 V, and 10 µF 50 V) were soldered onto a 3.1 mm thick FR4 board and subjected to temperature cycling between -65 ^{o}C and +150 ^{o}C. An overall view of the board is shown in Figure 18. Leakage currents at the twice rated voltages were monitored during 1,000 seconds of electrification. These measurements were carried out on loose capacitors, after soldering, and after 200 and 1,000 thermal cycles. It was expected that by using a relatively thick FR4 board and a wide range of temperature variations, cycling would eventually result in cracking and increase of leakage currents in the parts.

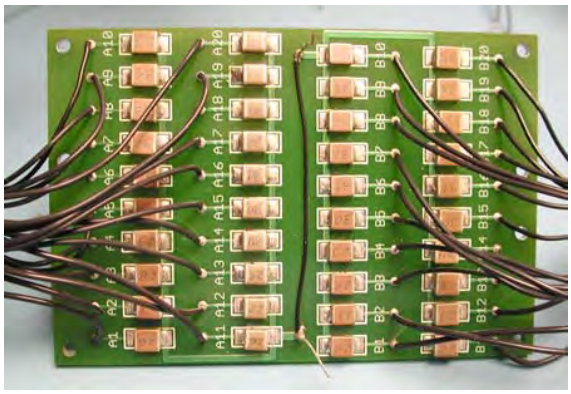


Figure 18. A test board with soldered capacitors.

Results of temperature cycling tests are presented in Figure 19. The leakage currents were stable through the testing in three out of four lots. After 1,000 cycles, one out of 20 samples from a 10 µF 50 V lot had unstable currents indicating intermittency, likely inside the part. This intermittency could be related to microcracking; however, external examinations did not reveal any anomaly. Additional analysis is required to verify this failure.

A high mechanical stability of large MLCCs subjected to temperature cycling is likely due to the fact that ceramic capacitors soldered onto an FR4 board remain under compressive stresses even at temperature extremes. For space projects, temperature extremes during box-level thermal cycling are typically within the range from -40 ^{o}C and +85 ^{o}C. Assuming the exponent in the Coffin-Manson equation for the acceleration factor of temperature cycling test is equal to 3, the 1,000 cycles between -65 ^{o}C and +150 ^{o}C would be equivalent to more than 5,000 box-level cycles. Our results show that at these conditions no wear-out failures in ceramic capacitors would be likely to occur.

These experiments, as well as solder-dip cycling tests, showed that cracking does not occur even after multiple cycles of exposure to extreme temperatures. It is possible that cracking is related to the preexisting flaws. Additional analysis of conditions that possibly might cause cracking during manual soldering of large MLCC is planned for next year's NASA Electronic Parts and Packaging (NEPP) Program task.

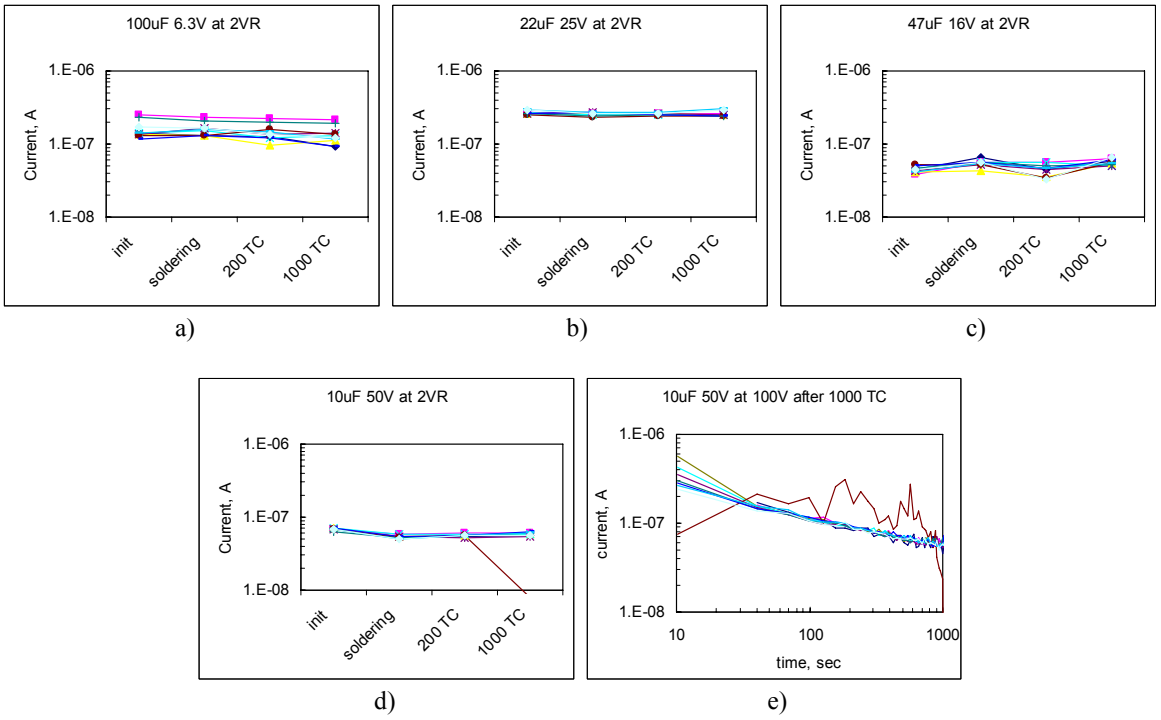


Figure 19. Leakage currents in four part types after soldering them onto an FR4 board and temperature cycling between -65 °C and +150 °C (a-d). Figure e) shows relaxation of leakage currents in 10 µF 50 V capacitors after 1,000 thermal cycles.

7. Summary.

1. Based on literature data, major sources, mechanisms of formation, and techniques for revealing cracking in MLCCs have been analyzed and classified. Possible reasons of manual-soldering-induced cracking have been discussed and areas of investigation have been determined.
2. Coefficients of thermal expansion were measured on six types of capacitors in the range of temperatures from room to 350 °C. All X7R capacitors had extreme temperature dependencies of CTE with the minimal values at Curie temperature. Average CTE values at T > Tc were in the range from 12.1 ppm/K to 14.4 ppm/K for all part types. At T < Tc CTE values were lower, and for different lots varied from 3.1 ppm/K to 9.6 ppm/K. CTE values in X7R capacitors measured perpendicular to the plates were ~10% greater than those measured along the plates. This anisotropy is likely due to built-in compressive stresses that are caused by CTE mismatch between ceramic materials and metal electrode plates, and were formed during sintering of capacitors.
3. Mechanical behavior of the parts was characterized by measurements of Vickers hardness and fracture indention toughness, K1C. Hardness of different types of capacitors varied in the range from 6.5 GPa to 10.6 GPa and did not depend significantly on the type of materials used. Estimations of the fracture toughness showed that X7R dielectrics had K1C values in the range from 0.9 to 1.55 MPa-$m^{0.5}$, whereas capacitors with COG

dielectric had a much larger value, 2.8 MPa-$m^{0.5}$. According to these measurements, the mechanical stability of the parts was expected to increase in the sequence 1 μF 50 V ≈ 10 μF 50 V < 47 μF 16 V < 22 μF 25 V ≈ 2.2 μF 50 V ≈ 100 μF 6 V << 22 nF 50 V.

4. To simulate thermal shock conditions that are specific to manual soldering, 20 samples of each of the seven lots of MLCCs were subjected to the molten solder (300 ^{o}C) terminal dip test. Characteristics of the parts were measured after 10, 30, and 100 solder pot cycles. No cracking or significant parametric variations were observed during this testing. This indicates that for normal-quality parts, thermal shock associated with manual soldering is likely not the major reason for cracking.

5. The effect of mechanical stresses created by excessive solder was investigated using ceramic capacitors with large solder chunks attached to the terminals. The parts were subjected to various temperature cycling and thermal shock tests while their characteristics were measured periodically.
   a. Contrary to what was expected, the worst mechanical stability was observed in 22 nF 50 V NPO capacitors. Note that these parts were relatively thin, H = 1 mm, and it is possible that for solder-induced damage the thickness of the part plays a more important role than the fracture toughness. Cracks at the edges of terminals were revealed using the vicinal illumination technique in all 22 nF 50 V samples, while only three out of five parts had increased leakage currents.
   b. Three lots of X7R capacitors had no anomalies, two lots had one sample each with a one-time instance of DCL increase, and one lot had three out of five samples manifesting unstable leakage currents through the testing. All anomalies were observed after exposure of the parts to low temperatures (-65 ^{o}C), whereas no failures occurred after cycling between room temperature and +165 ^{o}C. Optical examinations revealed no cracks in X7R parts. Analysis showed that all failures occurred in relatively thin capacitors, and that the probability of solder-induced damage increases as the thickness of capacitors diminishes.
   c. TC and TS tests revealed a memory effect in all X7R capacitors with attached solder chunks. The value of C measured at room temperature changed systematically on 4% to 7% depending on the last temperature during the cycling. Capacitance increased after exposure to high temperatures (150 ^{o}C to 165 ^{o}C), and decreased after exposure to negative temperatures (-65 ^{o}C to -196 ^{o}C). The first effect is due to de-aging of MLCCs at T > Tc, and the second is likely related to formation of solder-induced compressive stresses. These stresses are known to decrease dielectric constant in ferroelectric materials. No significant variations of capacitance were observed in 22 nF 50 V parts employing NPO dielectric.

6. To estimate the effect of mechanical stresses related to CTE mismatch between the capacitors and the FR4 board, 40 X7R capacitors from four different lots were subjected to 1,000 temperature cycles between -65 ^{o}C and +150 ^{o}C. All parts passed 200 cycles, and only one part showed erratic leakage currents after 1,000 cycles. These data show that no wear-out failures would likely occur in PWB cards with soldered MLCCs during box-level temperature cycling tests in the range of temperatures from -40 ^{o}C to +85 ^{o}C.

7. The most effective methods for revealing cracks are monitoring of leakage currents at twice rated voltages and vicinal illumination optical microscopy technique. The success of using the methanol test was less than expected.

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Exhibit N

Definition of *stratum* in English:

stratum

Pronunciation /ˈstreɪtəm/ /ˈstrɑːtəm/

NOUN

1 A layer or a series of layers of rock in the ground.
'a stratum of flint'

+ More example sentences + Synonyms

1.1 A thin layer within any structure.
'thin strata of air'

+ More example sentences

2 A level or class to which people are assigned according to their social status, education, or income.
'members of other social strata'

+ More example sentences + Synonyms

2.1 *Statistics* A group into which members of a population are divided in stratified sampling.
'allocation of sample units to strata'

+ More example sentences

Usage

In Latin the word stratum is singular and its plural form is strata. In English this distinction is maintained—it is incorrect to use strata as a singular or to create the form stratas as the plural: a series of overlying strata not a series of overlying stratas, and a new stratum was uncovered not a new strata was uncovered

Origin

Late 16th century (in the sense 'layer or coat of a substance'): modern Latin, from Latin, literally 'something spread or laid down', neuter past participle of sternere 'strew'.

Pronunciation

stratum /ˈstreɪtəm/ /ˈstrɑːtəm/

Exhibit O

Definition of *offset* in English:

offset

NOUN

Pronunciation /ˈɒfsɛt/

1 A consideration or amount that diminishes or balances the effect of an opposite one.
'widow's bereavement allowance is an offset against income'
• More example sentences

2 The amount or distance by which something is out of line.
'these wheels have an offset of four inches'
• More example sentences

2.1 *Surveying* A short distance measured perpendicularly from the main line of measurement.
'if it was a simple curve, he was taught the 'ranging by offsets' technique'
• More example sentences

2.2 *Electronics* A small deviation or bias in a voltage or current.
[as modifier] *'offset adjustment circuits'*
• More example sentences

3 A side shoot from a plant serving for propagation.
'a present of tulip bulbs, offsets, and seeds for his garden'
• More example sentences

3.1 A spur in a mountain range.

4 *Architecture*
A sloping ledge in a wall or other feature where the thickness of the part above is diminished.
• Example sentences

5 A bend in a pipe to carry it past an obstacle.
'allow for any bend you need including offsets for connecting the downpipe'
• More example sentences

6 *[mass noun, often as modifier]* A method of printing in which ink is transferred from a plate or stone to a uniform rubber surface and from that to the paper.
'they produced banknotes by offset'
[as modifier] *'offset printing'*
• More example sentences

VERB

Pronunciation /ˈɒfsɛt/ /ɒfˈsɛt/

1 *[with object]* Counteract (something) by having an equal and opposite force or effect.
'donations to charities can be offset against tax'
'his unfortunate appearance was offset by a compelling personality'
• More example sentences • Synonyms

2 *[with object]* Place out of line.
'several places where the ridge was offset at right angles to its length'
• More example sentences

3 *[no object]* (of ink or a freshly printed page) transfer an impression to the next leaf or sheet.
'there was some offsetting on to text'

Pronunciation

offset NOUN /ˈɒfsɛt/